**Stacked-FET based GaAs
Monolithic Microwave High-Power
Amplifiers for Active Electronically
Scanned Array Radar Front-Ends**

Gijsbert van der Bent

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Gijsbert van der Bent

Voorzitter/secretaris

Universiteit Twente

prof. dr. ir. F.E. van Vliet

Universiteit Twente

dr. ir. W.J.A de Heij

Thales Netherlands

prof. dr. ir. B. Nauta

Universiteit Twente

prof. dr. A.A. Stoorvogel

Universiteit Twente

prof. S. Mahon

Macquarie University

prof. dr. D.M.W. Leenaerts

Technische Universiteit Eindhoven

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Stacked-FET based GaAs Monolithic Microwave High-Power Amplifiers for Active Electronically Scanned Array Radar Front-Ends

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CHAPTER 1

Introduction

1.1 Historical Context

In June 1904, Christian Hülsmeyer demonstrated a system that might be considered the first radar system. Although his invention, the Telemobiloskope, was strictly speaking not able to perform ranging, the concept of detection by means of the reflection of Electro-Magnetic (EM) waves was successfully demonstrated. Figure 1.1 shows a schematic representation of the Telemobiloskope, taken from his patent [1] that was filed in the same year 1904. It basically consisted of three parts: a spark-gap transmitter, an antenna and a coherer receiver.

Figure 1.1: Schematic representation of Hülsmeyer's Telemobiloskope.

The three components of which Hülsmeyer's invention consists are in fact the three basic fields for radar front-end research throughout the years: the generation of Radio Frequency (RF) power, transmission and reception of radio waves and the detection of weak signals. The relevance of these subjects is illustrated in the radar equation [2]:

$$R_{max} = \left[\frac{P_t G_A^2 \lambda^2 \sigma}{S_{min} (4\pi)^3} \right]^{\frac{1}{4}}. \quad (1.1)$$

This equation states that the maximum distance at which an object may be detected has an inverse fourth order dependency to the transmitted power P_t , the radar cross section of the target σ , the square of the antenna gain G_A and wave length λ and the inverse of the minimum detectable signal S_{min} . This implies that to increase the range of view of a radar system, the output power of the radar transmitter should be increased, the receiver noise level should be lowered or the transmission and reception should be more concentrated into the required direction. The latter is one of the aspects on which antenna research basically focuses: the efficient (and broadband) transmission and reception of radio waves in or from a given direction (with a prescribed polarisation). When it comes to receiver sensitivity, the focus is on the reduction of noise figure with non-linearity as a complicating factor. The difference in received power from a target nearby in comparison to the received power from a target far away is very large due the fourth order dependency in Eqn. (1.1) which imposes heavy demands on the dynamic range of the receiver. The RF power generation deals with the amplification of microwave signals, that can be up to the megawatt range.

1.1.1 Active Electronically Scanned Arrays

Early radars consisted of a single transmitter and receiver connected to a movable antenna. As the angular resolution of a radar system depends on the antenna beam width, often a narrow antenna beam is required and therefore the antenna should be large, or consist of an array of smaller antennas. Since these antennas are heavy components, changing direction is a slow process. This drawback is overcome by so called phased array antennas. These antenna systems consist of a large number of small elements, the direction of the beam is controlled by varying the phase relations between the elements. The interference pattern of the radiated waves is hence controlled and when applied properly a steerable wavefront may be obtained. In order to control the phase relations between the elements, the feeding path of each individual antenna element contains a variable phase shifter or time delay. In an Active Electronically Scanned Array (AESA) each antenna channel contains a complete RF front-end including a High Power Amplifier (HPA) and a Low Noise Amplifier (LNA). The advantage over passive phased arrays, where the individual elements do not contain an LNA or HPA,

is that also the gain of each channel is adjustable and can be equalised which results in a higher beam-forming flexibility. It opens the possibility for digital beam-forming which offers even more flexibility, such as forming multiple beams simultaneously. The optimum spacing between the antenna elements of a phased array depends on the wave length λ of the RF signals and is usually equal to or smaller than $\lambda/2$. This puts a practical limit on the size of the RF electronics as well since usually this has to fit within the same space.

1.1.2 Monolithic Microwave Integrated Circuits

In a Monolithic Microwave Integrated Circuit (MMIC), passive and active components are fabricated on a single semiconductor substrate. The first MMIC was published in 1976 [3]. The single stage X-band amplifier, which was developed by The Plessey Company Ltd, UK, was based on a Gallium Arsenide (GaAs) Metal-Semiconductor Field Effect Transistor (MESFET). Increasing the transistor's operating frequency, output power density and efficiency has been a focus of continuous research ever since. Other types of substrate materials such as Gallium Nitride (GaN), Indium Phosphide (InP) and transistor structures such as the High Electron Mobility Transistor (HEMT) and the Heterojunction Bipolar Transistor (HBT) were developed. The small size of MMIC based RF circuits has opened the possibility for large scale development of AESA front-ends containing thousands of RF modules [4].

Receiver evolution has benefited greatly from the advances in Silicon based technologies such as (Bi)CMOS. Although the performance level of III-V technologies are not completely met, the lower cost and increased level of integration are often decisive in the advantage of these technologies.

For the RF power generation, the weakness of Silicon based technologies becomes apparent: due the low breakdown voltages of the transistors, the RF voltage swing and hence the RF power levels are limited. An exception is found in Laterally Diffused Metal Oxide Semiconductor (LDMOS) processes. The maximum operating frequencies of LDMOS, however, is critical for application in S- or X-band radar front-ends although some progress is made in recent years [5]. GaAs based technologies have been the workhorse for power amplifiers for many years. Recently GaN technologies are becoming more popular due to the high breakdown voltage and correspondingly high output power density of these processes, which results in devices with high output power and efficiency.

1.2 Power amplification in AESA radar front-ends

The introduction of AESA front-ends has resulted in the distribution of (power) amplification. As a results the dissipation of power and hence the generation of heat occurs at various places throughout the system.

A conceptual representation of the power section of radar front-end is shown Figure 1.2. Within each channel the RF signal arriving from the exciter is amplified by the combination of a driver amplifier and an HPA. These amplifiers receive their Direct Current (DC) power from a power supply that can be shared by multiple channels. As the amplifiers have a finite efficiency, part of the supplied power will be dissipated and the thermal impedance of the path toward the heat sink will give rise to a temperature increase of the amplifiers. For a given RF output power, this temperature increase can be minimised by improving either the amplifier efficiency or the cooling of the system. The latter depends on the thermal construction of the front-end, but at least contains the thermal impedance from the transistors to the backside of the MMIC.

Figure 1.2: Conceptual power section of radar front-end.

Any resistance in the power lines that carry the supply currents will result in a voltage drop across these lines. The amount of drop is proportional to the supply currents, which in turn depend on the power that needs to be delivered to the amplifiers and the supply voltage of these amplifiers. With a given power delivered to the amplifier, for higher supply voltages these currents and hence the voltage drop will be lower.

Several options exist to increase the amplifier supply voltage. The most straightforward method is the use of a semiconductor technology with a high breakdown voltage. Although GaAs technologies with an increased drain bias voltage have been reported [6–11], in general GaAs based technologies typically operate at drain bias voltages below 12 V. Higher operating voltages are usually achieved by the use of wide band gap materials such as GaN [12]. Due to the higher supply voltage and hence for a given power level, higher voltage to current ratio at the transistors, the impedance levels of the transistors are

higher which results in simpler matching networks showing lower loss and larger bandwidth. GaN technologies, however, are relatively expensive compared to GaAs and the track record of reliability for GaN is still limited.

The integration of a step-down converter in the HPA chip [13] increases the supply of the amplifier on a system level. The complexity of the chip however is drastically increased and the limited possibilities for filtering makes it very difficult to obtain the supply stability that is required for the demanded spurious levels.

An alternative to the use of technologies with high breakdown voltages is the use of stacked transistors, also known as balanced cascodes, which will be further introduced in the next chapter.

1.3 This thesis

The aim of the work presented in this thesis is to obtain the benefits of a high supply voltage without the associated disadvantages of an expensive process with reliability uncertainties. For this purpose a method is investigated to use a conventional MMIC process at an increased supply voltage level, particularly through the use of Stacked-FETs. The theoretical and practical limitations of Stacked-FET amplifiers are systematically investigated and the feasibility is demonstrated by design. The focus of the work is on frequencies from 2 GHz to 4 GHz, commonly denoted as S-band.

Throughout this thesis the mentioned examples as well as the demonstrated Stacked-FETs and amplifiers are based on the PP25-20 GaAs process of WIN Semiconductor [14]. This is a 0.25 μm optical T-gate process targeting X-Ku-band high power applications. The process has been optimised for high breakdown voltage (18 V minimum, 21 V typical), and enables reliable high power operation at a drain bias of 8 V [15]. Further features include:

- 600 pF/mm² high density Metal-Insulator-Metal (MIM) capacitors
- 50 $\Omega/\square$ Tantalum Nitride (TaN) Thin Film Resistors
- 160 $\Omega/\square$ GaAs Epi Resistors
- Through-substrate via process for low inductance grounding
- Optional Benzocyclobutene (BCB) scratch protection layer

Any power amplifier design fundamentally deals with non-linear devices operating at power levels where reliability aspects related to both thermal and voltage or current stresses need careful consideration. For integrated microwave power amplifiers additional challenges arise due to the required accuracy of EM and transistor modelling, in combination with the intrinsically unstable behaviour of the transistors. The use of Stacked-FETs brings additional transistor

modelling complexity due to the fact that not all transistor are operated in the classical common-source configuration. This fact also introduces additional instability modes which, in combination with layout and routing issues that result in additional (biasing) loops, complicates the overall amplifier stability.

In chapter 2 of this thesis the basic concept of a Stacked-FET is introduced. The landscape in which Stacked-FET HPAs are investigated is described and the terminology with respect to power amplifiers is clarified. Details are given regarding typical operating classes and the modelling and simulation of the RF performance is introduced.

A thorough analysis of the operation of Stacked-FETs and the method for optimum dimensioning is given in chapter 3. It is shown how a linearised approached is used for the dimensioning in the large signal regime. A numerical example is given and results of a family of demonstrated Stacked-FETs are presented. The effect of transistor stacking on bandwidth is discussed and the biasing of the Stacked-FET is covered. Load mapping of the transistors in the Stacked-FET is analysed together with the consequences for harmonic termination.

In chapter 4 an advanced transistor modelling approach is introduced, based on the simulation of the extrinsic transistor part in an EM solver. This method provides more flexibility with respect to transistor interconnections which is required for the compact layout of Stacked-FETs.

Chapter 5 focuses specifically on the stability issues within Stacked-FET amplifiers. The stability of the individual transistors, the stability of an entire stack and the stability within a complete amplifier are treated consecutively. A method is defined to include the implications of stability in the Stacked-FET design flow.

In chapter 6 a number of demonstrated examples is presented. It is shown how the designed Stacked-FETs can be used to design state-of-the-art power amplifiers that can compete with both GaAs and GaN based power amplifiers.

In chapter 7 the screening of Stacked-FET amplifiers is discussed, a relevant issue with respect to selection testing which is performed if these kind of amplifiers are to be used during the production of radar front-ends.

Finally the overall conclusions of the work are presented in chapter 8. It is shown that the power amplifiers, designed using the strategies introduced in this thesis, outperform other GaAs based amplifiers and the that results are competitive with the state-of-the-art in integrated GaN power amplifiers.

CHAPTER 2

Power Amplifiers Employing Stacked-FETs

2.1 Introduction

In this chapter the basis for power amplifier design using Stacked-FETs is set out. The technology in which the amplifier is designed is key to the achievable performance of the amplifier, therefore an overview of semiconductor technologies from an RF power perspective is given. General power amplifier terminology is introduced and the state-of-the-art in integrated power amplifiers is discussed. After packaging and application in radar front-ends a brief overview of power amplifier operating classes is given and a representative analysis of voltages and currents on the output of a class-B transistor is presented. The Stacked-FET concept is introduced and an overview of previously published research is given. Modelling and simulation of power amplifiers is treated and finally the design strategy is set out.

2.1.1 Semiconductor Technology Overview

Semiconductor technologies can roughly be divided in two categories: Silicon (Si)-based technologies that are very suitable for low cost, high volume production and III-V technologies, such-as GaAs and GaN technologies, that are optimised mainly for lower volume, high performance devices. The RF power capabilities of various technologies are presented in Figure 2.1. Radio Frequency Complementary Metal Oxide Semiconductor (RF-CMOS) and Si Bipolar technologies cover a wide frequency range, but the output power levels are low. LDMOS and Silicon Carbide (SiC) transistors are able to generate high output power levels but the operation frequency is limited to approximately

3 GHz. GaAs covers a wide frequency range with output power levels in the order of 10 Watt. The operating frequency range for GaN technologies is comparable to that of GaAs, but the output power levels are approximately one order of magnitude higher.

Figure 2.1: Power capabilities for various semiconductor technologies [16].

2.1.2 Radar applications

Radar applications exist at a wide range of frequency bands for various applications. Each application has its own requirements with respect to output power. An overview of power levels and frequency bands for various systems is given in Figure 2.2. The commonly used frequency band denotations are included in the figure. High power S-band radars are often surveillance radars, either for military purposes or for civil applications such as Air Traffic Control. The reported C-band radars are short range search radars. X-band radars exist for many applications including surveillance, navigation, fire control and precipitation detection. The number of front-ends in an AESA system can go up to several thousands which means that the output power requirement for a single front-end is three orders of magnitude lower. For these application output power levels from 10 W to 100 W are required from a single (integrated) amplifier.

Figure 2.2: Power levels for different radar applications and frequencies [17].

2.1.3 Power Amplifier Terminology

Two port representation

Often used terms related to power amplifiers are defined according to definitions shown in Figure 2.3. The power source with impedance Z_s is connected to the input of the two-port, which is loaded with impedance Z_L . The four definitions of reflection coefficient are indicated in the figure.

Figure 2.3: Definitions related to two-port.

Power definitions

The output power P_{out} of an amplifier is defined as the power delivered to the load of that amplifier. The input power P_{in} of an amplifier is defined as the power delivered to the amplifier. The available source power P_{avs} is defined as the maximum power a source can deliver to a load; this occurs when this load is conjugately matched to the power source.

The relation between the input power and the available source power is determined by the input matching Γ_{in} of the amplifier:

$$P_{in} = P_{avs} (1 - |\Gamma_{in}|^2), \quad (2.1)$$

where the factor $(1 - |\Gamma_{in}|^2)$ accounts for the power reflected at the input of the amplifier.

Gain definitions

The Transducer Gain G_T is the ratio between the output power and the available source power:

$$G_T = \frac{P_{out}}{P_{avs}}. \quad (2.2)$$

The transducer gain is used to characterise amplifiers in their environment as it includes actual mismatch losses at the input and the output of the amplifier.

The power gain G_P is the ratio between the output power and the input power:

$$G_P = \frac{P_{out}}{P_{in}}. \quad (2.3)$$

The power gain definition is used to characterise the gain of power transistors which is usually not conjugately matched; it assumes ideal matching at the input and only includes actual mismatch loss at the output.

The Power Gain is related to Transducer gain according to:

$$G_P = \frac{G_T}{1 - |\Gamma_{in}|^2}. \quad (2.4)$$

The Available Gain G_A is the ratio between the available output, defined as the output power delivered to a conjugately matched load, and the available source power:

$$G_A = \frac{P_{out}|_{Z_L=Z_{out}^*}}{P_{avs}}. \quad (2.5)$$

The available gain is only defined for the small signal case, as the available output power under large signal excitation is not necessarily maximal for a conjugately matched load.

Efficiency definitions

Drain efficiency η_d is a measure for how much DC power P_{DC} is converted into RF output power:

$$\eta_d = \frac{P_{out}}{P_{DC}}. \quad (2.6)$$

Drain efficiency does not provide any information on how much RF input power is required to drive the circuit and is therefore an inadequate measure for efficiency. Low gain devices can have a high drain efficiency while a significant part of the output power is not generated by the amplifier but is delivered by the power source that drives the amplifier.

The Power Added Efficiency (PAE) describes the fraction of DC power that results in additional output power:

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} = \eta_d \left(1 - \frac{1}{G_P} \right). \quad (2.7)$$

Eqn. (2.7) shows that for high gain levels the PAE approximates the drain efficiency. This is illustrated in Figure 2.4 where the ratio between PAE and drain efficiency η is shown as function of the power gain of a device. It can be seen that for high gain levels, e.g. higher than 15 dB, the difference is small.

Figure 2.4: Effect of gain on PAE.

Definitions related to matching networks

For a multi-port matching network with inputs 1 to N_{in} , the input reflection coefficient Γ_k^e on port k for even mode excitation on all N_{in} input ports is given by:

$$\Gamma_k^e = \sum_{n=1}^{N_{in}} S_{n,k}. \quad (2.8)$$

The matching Γ_k^m of input k of a network is a measure for the error between the realised and the required input reflection coefficient on that input of the network. It is determined by renormalising even-mode input reflection coefficient Γ_k^e to the required reference reflection coefficient Γ_{ref} :

$$\Gamma_k^m = \frac{\Gamma_k^e - \Gamma_{ref}}{1 - \Gamma_k^e \Gamma_{ref}^*}, \quad (2.9)$$

The ohmic loss L_m of a multi-port, passive matching network is defined as the ratio between the total output power and total input power of the network:

$$L_m = \frac{\sum_{n=1}^{N_{in}} P_{in,n}}{\sum_{m=1}^{N_{out}} P_{out,m}}, \quad (2.10)$$

where N_{in} denotes the number of inputs, $P_{in,n}$ the input power at input port n , N_{out} the number of outputs and $P_{out,m}$ the output power of output port m .

2.1.4 State of the Art in AESA Power Amplifiers

In this section a brief overview of the state-of-the-art in integrated power amplifiers suitable for AESA front-ends for S, C and X-band is given. A distinction is made between amplifiers in GaAs and GaN technologies since the properties of these technologies are significantly different.

GaAs amplifiers

An overview of output power of GaAs power amplifiers is depicted in Figure 2.5 and the associated PAE is given in Figure 2.6. The maximum output power at S-band is approximately 20 W [18]. The MMIC that delivers this power has an associated PAE of 35 % and is designed in a 0.5 μm pHEMT technology. The output stage of this amplifier contains sixteen transistors with 8 gate fingers with a width of 350 μm each. The chip measures 6.3 mm x 5.6 mm. At X-band the highest power level of approximately 16 W is delivered by [19]. The PAE of this MMIC is 28%. It is designed in M/A-COMs Multifunction Self-Aligned Gate (MSAG) process and has sixteen transistors in the output stage. The chip dimensions are 5 mm x 8.15 mm.

Figure 2.5: Overview of state-of-the-art GaAs HPA output power.

Figure 2.6: Overview of state-of-the-art GaAs HPA PAE.

Figure 2.7: Overview of state-of-the-art GaN HPA output power.

Figure 2.8: Overview of state-of-the-art GaN HPA PAE.

GaN amplifiers

The maximum output power of the state-of-the-art GaN amplifiers is summarised in Figure 2.7, the PAE levels of these amplifiers are given in Figure 2.8. At S-band a maximum output power of more than 130 W is achieved [35]. The HPA that delivers this power is designed in a $0.25\ \mu\text{m}$ GaN on SiC process and operates at a drain bias voltage of 40 V. The device uses four transistors in the output stage and has a chip dimension of 6 mm x 5.1 mm. The maximum output power at X-band is approximately 50 W [39] by an MMIC designed in the SELEX Sistemi Integrati $0.5\ \mu\text{m}$ technology. The output stage consists of eight $10\times 100\ \mu\text{m}$ transistors and the chip dimensions are 5 mm x 3.2 mm.

2.1.5 Packaging

In RF radar front-ends, packaged MMICs are often used as this eases the handling during assembly. Low-cost plastic packages have become more popular over more conventional ceramic packages [45], even for high power applications. Where ceramic packages used to be mounted directly on a metal heat sink, standard plastic packages are usually mounted on a Printed Circuit Board (PCB) which means that the maximum heat flux from the package toward the heat sink is smaller. To prevent the transistors in the MMIC from overheating, a higher demand is placed on the both the cooling of the system and the dissipation in the MMIC.

The plastic-moulded Quad-Flat No-Leads (QFN) package [46], as shown in Figure 2.9, is among the most popular package types. This type of package does not contain any leads, the pads to which the wires are bonded are directly soldered to the PCB. This limits the additional inductance and is therefore well suited for high frequency applications. The die is bonded on a copper die paddle which is also directly soldered to the PCB. The package is closed with a plastic mould compound.

Figure 2.9: QFN Package [47].

The effect of the plastic on both the RF performance and the maximum temperature of the chip can usually not be ignored and hence has to be included in the simulations of the packaged MMIC. In chapter 6, which describes the Stacked-FET amplifiers, more details on the thermal analysis are given. The effects of the plastic mould and the bondwires on the RF performance are taken into account by including these in the EM simulations of the matching networks of the amplifiers.

2.2 Power Amplifier Classes

2.2.1 Classification

Power amplifiers are divided into classes based on the operation of the transistors in the amplifier. A first division in operating classes is between either switched-mode or current-mode power amplifiers [48]. In switched-mode amplifier classes the transistor switches between the on-state and the off-state during each RF-cycle while in current-mode classes the transistor output current varies proportionally to the input voltage or current during (part of the) RF-cycle.

The difference between the Class-A, -B and -C amplifier is only the current biasing point and therefore the Current Conduction Angle (CCA), which is the total phase during the RF-cycle that the device is conducting current. For class-A this CCA is 100 %, for class-B this is 50 %. The class-C CCA is below 50 %. Class-D [49] and -S [50] are switch-mode amplifier classes using pulse width modulation which means that the RF output signal should be restored using an output filter. This makes these types of amplifier classes less suitable for high frequency applications. A Class-E amplifier [51] is designed such that the transistor switches at the time instance where the voltage across this transistor is zero. The output capacitance is fundamental to the operation and therefore does not limit the maximum operation frequency. The maximum achievable output power, however, is significantly lower than for other classes. In a Class-F (or class-F⁻¹) amplifier [52] the harmonic environment is designed such that the voltage (or current) is a square wave and does not overlap with the current (or voltage) which results in zero power dissipation. For Class-J and -J* [53], the biasing point is equal to class-B which means that the quiescent current is zero and a half rectified sinusoidal current waveform is obtained. A range of drain voltage waveforms can be constructed with proper combinations of fundamental and second harmonic components that all yield equal RF-performance. In fact class-B is a special case of the Class-J continuum [54]. This concept is later extended into the definition of the continuous class-F [55] and inverse class-F [56]. Recently a further extension is introduced in the class-X amplifier where analysis shows a range of fundamental, second and third harmonic load combinations that yield equal drain efficiency [57].

Table 2.1: Amplifier classes with biasing conditions, harmonic environment and theoretical maximum efficiency.

<i>Class</i>	<i>Mode</i>	<i>Bias</i>	<i>Even harmonics</i>	<i>Odd harmonics</i>	<i>max. η_d</i>
A	Current	$I_{max}/2$	Short	Short	50 %
B	Current	At pinch off	Short	Short	78.5 %
C	Current	Below pinch off	Short	Short	100 % ^a
D ^b	Switched	-	-	-	100 %
E	Switched	-	-	-	100 %
F	Current	At pinch off	Short	Open	100 %
F ⁻¹	Switched	-	Open	Short	100 %
J(*)	Current	At pinch off	Γ_{L,f_0} dependent	Short	78.5 %
S	Switched	-	-	-	100 %

^a The maximum efficiency of a Class-C amplifier is the limiting case. 100 % is achieved for a CCA of zero, which results in zero output power.

^b Two variants of Class-D exist, either voltage or current switching.

For each operating class a specific load line is presented to the transistor. Although these load lines are different for the various classes it is illustrative to explore the load line for one of the classes since this shows how the current and voltage relations determine the operation of the transistor. Class-B operation is chosen since this is representative for the loading of the transistors in a current-mode microwave amplifier and provides most insight through its simplicity.

2.2.2 Class-B Analysis

In this section an analysis is given of the Class-B current and voltage waveforms that determine the optimum transistor loading, output power and drain efficiency. A textbook approach such as given in [48] or [58] is followed. For Class-B operation the quiescent drain current is zero with the transistor biased at the pinch-off point, which yields a half rectified sinusoidal current waveform at the output of the transistor. The drain bias voltage V_{dd} is chosen halfway the knee voltage V_k and the maximum voltage V_{max} . A simplified transistor output-IV plane is used where the knee voltage is determined by the transistor on-resistance $R_{ds_{on}}$ and the maximum current I_{max} :

$$V_k = R_{ds_{on}} \cdot I_{max}. \quad (2.11)$$

Figure 2.10 shows the class-B biasing point in the simplified IV-plane together with the drain voltage and current swing at the edge of compression. The transistor load is selected such that this swing reaches the V_k and I_{max} points

simultaneously. The value of the corresponding load resistance is obtained from the straight line connecting the endpoints of this voltage and current swing.

Figure 2.10: Voltage and current excursions for class-B bias operation.

Figure 2.11: Class-B current and voltage waveforms.

The voltage and current waveforms at the output of the transistor are shown in Figure 2.11. The current waveform $I(\omega t)$ can be described by a real Fourier series [59]:

$$I(\omega t) = I_0 + \sum_{n=1}^{\infty} I_n^a \cos(n\omega t) + \sum_{n=1}^{\infty} I_n^b \sin(n\omega t). \quad (2.12)$$

For the half wave rectified cosine waveform, with $k = n/2$ [60]:

$$I(\omega t) = \frac{I_{max}}{\pi} + \frac{I_{max}}{2} \cos(\omega t) - \frac{2I_{max}}{\pi} \sum_{k=1}^{\infty} \frac{(-1)^k}{4k^2 - 1} \cos(2k\omega t). \quad (2.13)$$

By inspection, the DC component I_0 is:

$$I_0 = \frac{I_{max}}{\pi} \quad (2.14)$$

and the amplitude of the fundamental component I_1 is:

$$I_1 = I_1^a = \frac{I_{max}}{2}, \quad (2.15)$$

as I_1^b evaluates to 0. The voltage waveform $V(\omega t)$ is:

$$V(\omega t) = V_0 - V_1 \cos(\omega t), \quad (2.16)$$

with DC component V_0 :

$$V_0 = V_{dd} \quad (2.17)$$

and amplitude of fundamental component V_1 :

$$V_1 = V_{dd} - V_k. \quad (2.18)$$

The optimum fundamental load resistance R_{opt} is found by division of the fundamental voltage and current amplitudes. Dividing Eqn. (2.18) by Eqn. (2.15) yields:

$$R_{opt} = \frac{V_1}{I_1} = \frac{2(V_{dd} - V_k)}{I_{max}} = 2 \left(\frac{V_{dd}}{I_{max}} - R_{ds_{on}} \right). \quad (2.19)$$

The output power delivered to this optimum load resistance is given by:

$$P_{out} = \frac{I_{max}(V_{dd} - V_k)}{4} = \frac{(V_{dd} - I_{max}R_{ds_{on}})^2}{2R_{opt}}. \quad (2.20)$$

The consumed DC power P_{DC} is obtained from the product of the DC voltage and current components given by Eqn. (2.17) and Eqn. (2.14) respectively:

$$P_{DC} = V_{dd}I_0 = \frac{V_{dd}I_{max}}{\pi}. \quad (2.21)$$

The drain efficiency η_d is defined by:

$$\eta_d = \frac{P_{out}}{P_{DC}}. \quad (2.22)$$

Combined with Eqn. (2.20) and Eqn. (2.21) this yields:

$$\eta_d = \frac{\pi}{4} \cdot \frac{V_{dd} - I_{max}R_{ds_{on}}}{V_{dd}} = \frac{\pi}{4} \cdot \left(1 - \frac{I_{max}R_{ds_{on}}}{V_{dd}}\right) \quad (2.23)$$

2.2.3 Drain Bias Voltage Reduction

The reduction of drain bias voltage is often used as a mechanism to control the output power of a power amplifier. The effect of this drain bias voltage on the transistor performance is analysed in this section, based on the results from section 2.2.2. The analysis is based on idealised class-B operation but is representative for other current-mode classes as well.

The nominal load R_{opt} will be determined at the nominal DC drain voltage $V_{dd_{nom}}$. The case is analysed in which the DC drain voltage is reduced to $V_{dd_{new}}$, while the output voltage swing is reduced by reducing the transistor drive to prevent the voltage from becoming smaller than the (current dependent) knee voltage. In this way $V_{d_{min}} = V_k(I_{peak}) = I_{peak}R_{ds_{on}}$ is maintained, where I_{peak} is the maximum current.

In the idealised class-B case, the voltage waveform contains only a fundamental component, which depends on the load impedance R_{opt} and the fundamental current component. The new DC and fundamental current components are now respectively:

$$I_{0_{new}} = \frac{I_{peak}}{\pi} \quad (2.24)$$

and

$$I_{1_{new}} = \frac{I_{peak}}{2}. \quad (2.25)$$

The new maximum current I_{peak} is obtained by rearranging Eqn. (2.19) with $I_{max} = I_{peak}$ and $V_k = I_{peak}R_{ds_{on}}$:

$$I_{peak} = \frac{V_{dd_{new}}}{R_{ds_{on}} + \frac{R_{opt}}{2}} = I_{max} \frac{V_{dd_{new}}}{V_{dd_{nom}}}. \quad (2.26)$$

It is seen that the maximum current scales linear with the DC drain supply voltage. The new output power is:

$$P_{out_{new}} = \frac{I_{peak}(V_{dd_{new}} - I_{peak}R_{ds_{on}})}{4}. \quad (2.27)$$

The new DC power is :

$$P_{DC_{new}} = \frac{I_{peak}V_{dd_{new}}}{\pi}. \quad (2.28)$$

The new drain efficiency is found by division of Eqn. (2.27) and Eqn. (2.28):

$$\eta_{new} = \frac{\pi}{4} \left(1 - \frac{I_{peak} R_{ds_{on}}}{V_{dd_{new}}} \right), \quad (2.29)$$

which, combined with Eqn (2.26), can be simplified to:

$$\eta_{new} = \frac{\pi}{8} \left(\frac{R_{ds_{on}}}{R_{opt}} + \frac{1}{2} \right)^{-1}. \quad (2.30)$$

Eqn. (2.30) shows that in the idealised case, in contrary to common believe, the drain efficiency has no drain bias voltage dependency and only depends on the on-resistance of the transistor and the loading resistance.

2.3 The Concept of Transistor Stacking

2.3.1 Introduction

As described in Section 1.2, an increased supply voltage of the power amplifier in a radar front-end is beneficial at the system level. This increase in supply voltage can be achieved by sharing the supply by a number of devices in series. These devices can be complete matched amplifiers or individual transistors within an amplifier. An example of the first option, where the total supply is divided over a number of complete power amplifiers, is given in [61]. In these amplifiers the outputs of the individual amplifiers are summed up externally. Basic examples of the second option are given in [62] and [63]. In these amplifier types the bias voltage is supplied to a series of transistors where an RF ground is created for each individual transistor by proper decoupling [62, 63]. Although these two options provide the advantage of the high supply voltage, the impedance levels at the transistors in the amplifier stages are still the same as for classical stages.

In a balanced cascode or stacked transistor amplifier, a number of transistors (N) is stacked in order to increase the total breakdown voltage with the same factor N . The voltage swings of the individual transistors in the stack are summed, resulting in an overall voltage swing on the stack which is N times higher than the voltage swing on a single transistor while all transistors carry an equal DC as well as RF drain current. In the ideal case, which means without losses due to stabilisation and non-perfect voltage and current equalisation, this results in an output power that is also N times larger than for a single transistor.

Stacked transistor circuits exist in many forms and are used for various applications where the bias voltage is too high for a single transistor. In some cases, for example in the logic gates of digital circuits, this excess voltage might cause a high amount of leakage current. In these cases Stacked-FET structures can help to reduce these leakage currents [64–66]. In other cases, for example in TR switches, the RF swing is so high that the transistor is pushed out of its

required biasing regime and starts to conduct where it should isolate, or vice versa. In these cases a Stacked-FET structure helps to limit the RF voltage swing on a single transistor [67,68]. In the majority of cases, however, the voltage limit is due to reliability issues, for example in power supplies where the switched voltage levels can be higher than allowed by the used transistors [69,70], or in (microwave) power amplifiers where the voltage swing can exceed the transistor breakdown voltage.

2.3.2 Stacked-FETs in Microwave PAs

A Stacked-FET stage is shown in Figure 2.12. It consists of a CS Field Effect Transistor (FET) loaded by in this case a series of two FETs with the source and drain terminals as inputs and outputs respectively. These loading transistors are strictly speaking not real Common Gate (CG) stages, as this requires a perfect ground potential at their gates. Hence they are referred to as Degenerated Common Gate (DCG) stages. In a classical cascode, which contains a real CG stage, the voltage swing is not equally divided over the transistors which does not yield the required overall increase of voltage swing. The exact procedure to obtain proper balancing of the Stacked-FET, i.e. to equalise all the voltages and the currents of the individual transistors in the stack, is the subject of the next chapter.

Figure 2.12: Stacked-FET.

The comparison between the load lines of a single FET and a Stacked-FET containing three transistors is depicted in Figure 2.13. The knee voltage but also the voltage head room is increased with a factor equal to the number of FETs

in the stack, in this case three. This increases the voltage swing and hence the optimum load resistance for the complete stack with the same factor.

Figure 2.13: Voltage and current excursions for stack of three FETs, including single FET excursion as a reference.

The thermal properties of a Stacked-FET amplifier and a classical, CS-based amplifier are compared through the thermal analysis of two different four-transistor configurations.

The first case consists of an amplifier stage combining four power transistors in parallel. In the second case, two Stacked-FETs are combined in parallel, while each stack consists of two power transistors.

In both cases the total number of transistors and the dissipated power per transistor are equal. The simulations are performed in COMSOL [71] with the thermal setup that is further described in Chapter 6. The dissipated power per transistor is 1.5 W and the backside temperature is 60 °C. The results of the simulations are shown in Figure 2.14. The maximum temperature is 90.6 °C for the CS stage and 92.4 °C for the Stacked-FET stage. This implies that from a thermal point of view no significant difference is present between the two cases. In the case of a Stacked-FET stage, however, the distance between the stacks in parallel can be increased while still obtaining a chip area that is smaller than for the CS case. This reduced the thermal coupling between the stacks and the maximum channel temperature. Due to the smaller chip space required for a Stacked-FET stage, there is larger degree freedom in comprising between chip area and thermal resistance.

Figure 2.14: Thermal analysis of the amplifier stage with four transistors in (a) CS configuration and (b) Stacked-FET configuration.

2.3.3 Prior Art

Stacked-FET microwave amplifiers are demonstrated in GaAs [63, 72–81], GaN [82, 83] as well as Si based [81, 84–93] technologies.

In [94] a stacked transistor amplifier is described in which the input signal is actively provided to the transistors high in the stack. Patent [95] aims specifically at the biasing of the devices in the stack. In [96] class-E switching using Stacked-FETs is discussed. Several authors have derived equations for optimum stack performance. [97] and [98] give a description assuming that the drain-source capacitance is zero. In [88] and [81] a detailed description is given, however in some parts of the analysis the imaginary part of the optimum load impedance of a single transistor is assumed to be zero or the transistor model is simplified by ignoring the gate-to-drain capacitance C_{gd} .

In [74] and [87] the drain-to-source and drain-to-gate capacitances are ignored. [99] gives an original derivation which is only valid when the drain-to-gate capacitance is ignored. [100] gives an analysis of the stacking limitations, aiming at oscillator applications in the sub THz range. A W-band Stacked-FET amplifier is also described in [101]. In [102] a GaAs Stacked-FET is used as a unit cell for the design of a distributed amplifier. Some authors pay special attention to the harmonic tuning or waveform engineering of Stacked-FET amplifiers [103, 104]. The highest reported output power from a Stacked-FET based GaAs MMIC is approximately 8 W in the high L-band / low S-band [105].

In summary (1) no comprehensive analysis is available that is suitable for microwave Stacked-FET power amplifier design as this includes at least the need for incorporating the transistor's C_{gd} and C_{ds} and the possibility to load the individual transistors in the stack with a complex load admittance and, (2) the

demonstration of these microwave amplifiers is limited to power levels below 10 W and even that only at the very low microwave frequencies. In particular transistor dimensioning, stability trade-offs and simulation methods are absent in literature. The work in this thesis, however, aims at (1) giving a detailed and in-depth treatment on the design of high power Stacked-FET amplifiers and, (2) demonstrating the capabilities of microwave Stacked-FET power amplifiers at power levels above 10 W.

2.4 Modelling and Simulation

Transistor characterisation is based on the measured results on individual (CS) transistor samples. An example of such a sample is shown in Figure 2.15. In this figure the reference planes of the measurements and the model extracted from these measurements are indicated. Usually the transistor samples are on test cells that contain a variety of transistors with different numbers of gate fingers and unit gate finger widths to determine the geometry dependency of the transistor characteristics.

Figure 2.15: Common source FET for characterisation and modelling.

Two types of measurements for the characterisation of transistors can be identified. The first type is the measurement of DC-currents and S-parameters under various biasing conditions. The results of these measurements can be used as input for model extraction or to evaluate the small-signal behaviour (for example stability) over a wide range of operating conditions. The second type of measurements are load-pull measurements in which the transistor performance dependency upon the externally applied load impedance is analysed. The results of these measurements will be used in determining the desired load impedance, trading power, gain and efficiency.

2.4.1 Transistor modelling and characterisation

Transistor models can be classified in three categories. Physics-based models [106] describe the transistor from the properties of the device structure. These kinds of models reflect the internal operating mechanisms of the transistor and are mainly used for device and technology optimisation as they tend to be unnecessarily complex for circuit simulations. Empirical or behavioural models [107] describe the behaviour of the transistor without any link to the physical operation of the device. These black box models can be used for simulations on a specific transistor geometry under specific conditions such as operating frequency, power range and impedance levels. Changes in these conditions and scaling of transistor size significantly reduces the reliability. Compact models [108] are an intermediate category. These models are based on elementary electronic components and their constitutive equations. The model topology can be mapped to the device structure, whilst the parameter values are obtained from measurements and curve-fitting. The work performed in this thesis is based on these compact models.

The topology of the used small signal compact model is given in Figure 2.16 [109]. A distinction can be made between the intrinsic components C_{gs} , C_{gd} , C_{ds} , g_m , τ , R_{ds} , R_{id} and R_{is} describing the active part of the transistor and the extrinsic components L_g , R_g , C_{pg} , L_d , R_d , C_{pd} , L_s , R_s and C_{ps} which describe the remainder of the transistor structure.

Figure 2.16: Small-signal model topology.

In transistor models valid for CS FETs the parasitic source capacitance C_{ps} is often ignored as in CS configuration it is paralleled by the small source inductance. If the source of the transistor is not grounded, as is the case for

DCG stages in a Stacked-FET, this capacitance should be explicitly included in the model.

The extrinsic component values for a measured device are determined from the measured S-parameters at the so called 'Cold-FET' bias point of $V_{ds} = V_{gs} = 0$ V [110]. The measured DC-currents and S-parameters versus all bias points are de-embedded up to the intrinsic transistor plane using these component values. The resulting bias dependent intrinsic model parameters are then fitted with a non-linear model such as the EEHEMT1 [111] or Angelov's [112–114] model. The combination of the intrinsic non-linear model and the extracted extrinsic model forms the overall large signal transistor model.

Load-pull measurements are performed to determine the performance of a transistor over a range of output loads, either at the fundamental frequency only or for combinations of loads at fundamental and higher harmonic frequencies. These load-pull measurements can be carried out with passive tuners, which mechanically adjust the load impedance levels, or by means of active injection where an RF signal is applied to mimic the effect of a reflected signal [115–122]. Both type of load-pull measurements can be performed on multiple harmonic frequencies simultaneously. The advantage of active load-pull is that losses on the output of the Device Under Test (DUT) can be compensated whilst for passive load-pull these losses directly limit the maximum magnitude of the reflection coefficient that can be applied. A combination of passive and active load-pull can also be applied, for example to use the passive tuner as a pre-match and the active sources for fine load adjustment or to tune the load at the fundamental frequency with the passive tuner while the higher harmonic loads are tuned actively.

2.4.2 Simulation Methods

During the HPA design, the first iterations are performed with lumped, idealised models for the passive parts. Small signal and Harmonic Balance simulations are performed to determine the performance as well as the stability of the amplifier. During succeeding iterations, the idealised models are replaced by increasingly realistic models containing more parasitic effects. Then the passive parts are analysed with a 2.5-D EM solver such as Keysight's Advanced Design System (ADS) Momentum [123] or Sonnet Design Suite [124] and finally a single EM simulation is performed for each matching network, including bias lines and other non-RF structures. The effect of packaging on the RF performance can be analysed with 3-D EM solver such as Ansoft's HFSS [125] or Keysight's ADS EMPro [123]. Thermal simulations are performed to analyse the maximum temperature of the active parts in the MMIC as well as the maximum package and PCB temperature. Input for these thermal simulations are the MMIC layout, the dissipation of the active and passive components in the MMIC and the layer stack including package, PCB and cooling structure.

2.4.3 Stability analysis

Among the most challenging parts of power amplifier design is the prevention of oscillations, which requires comprehensive stability analysis techniques. In this section an overview is given of commonly used methods. These methods can be divided in two categories. First there are the two-port techniques, which analyse the stability from the two-port parameters and the external impedances presented to the ports. The second category are the internal stability analysis methods that analyse the stability from the internal nodes. These methods can be applied to structures containing multiple active devices and take the effects of loops into account.

Two-port techniques

The most common approach for stability analysis is based on standard two-port techniques in which the stability circles are analysed either directly or by means of derived parameters such as K [126] or μ [127]. Via these parameters the effect of terminating impedances on the stability is analysed of a device that is stable when both ports are terminated with the impedance levels for which the two-port parameters are given [128, 129]. Although these techniques are strictly speaking only valid for small signal cases, applying these techniques using a linearisation in the large signal operation points extends the range of applicability.

For an intuitive analysis of these two-port techniques, the load and source stability circles are defined. The load stability circle represents the values for Γ_L for which $|\Gamma_{in}|=1$ and is defined by the centre [130]:

$$c_L = \frac{(S_{22} - S_{11}^* \Delta_S)^*}{|S_{22}|^2 - |\Delta_S|^2} \quad (2.31)$$

and the radius

$$r_L = \left| \frac{S_{12} S_{21}}{|S_{22}|^2 - |\Delta_S|^2} \right|. \quad (2.32)$$

where $\Delta_S = S_{11} S_{22} - S_{12} S_{21}$ is the determinant of matrix $\mathbf{S}$.

In a similar way the source stability circle that represents the values for Γ_S for which $|\Gamma_{out}|=1$ is defined by the centre:

$$c_S = \frac{(S_{11} - S_{22}^* \Delta_S)^*}{|S_{11}|^2 - |\Delta_S|^2} \quad (2.33)$$

and the radius

$$r_S = \left| \frac{S_{12} S_{21}}{|S_{11}|^2 - |\Delta_S|^2} \right|. \quad (2.34)$$

The load and source stability circles indicate the boundary between the stable and unstable regions. No knowledge, however, is obtained whether the stable regions are inside or outside of the circles. This knowledge can be derived from

the stability information on a known reflection coefficient either inside or outside the circle. If the device is measured and stable in a $50\ \Omega$ environment, the region that contains this $50\ \Omega$ point is the stable region. If no measurement results are available, the stability for a fixed environment can be obtained from an analysis of the system poles within this environment, using techniques as discussed in the next section.

A device is said to be unconditionally stable if no passive termination exists that results in instability of the device. This means that the unstable regions indicated by the stability circles are entirely outside of the Smith Chart.

A commonly used method to analyse the unconditional stability of a device is by means of Rollett's stability factor K defined by:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |\Delta_S|^2}{2|S_{12}S_{21}|}, \quad (2.35)$$

or in terms of imittance parameters:

$$K = \frac{2\Re(\gamma_{11})\Re(\gamma_{22}) - \Re(\gamma_{12}\gamma_{21})}{|\gamma_{12}\gamma_{21}|}. \quad (2.36)$$

Note that in contrast to the original paper by Rollett, this thesis uses a capital K to avoid confusion with Boltzmann's constant.

This factor indicates whether the stability circles intersect the edge of the Smith Chart [127, 131], which is not the case for $K > 1$. This is, however, not sufficient to prove unconditional stability. To that end, an additional parameter is required to guarantee that the stability circle lies outside of the Smith Chart. Several options exist to express this condition, for example $|\Delta_S| < 1$. If both criteria are met, the device is unconditionally stable under the proviso that stability is proven for any set of passive termination impedances [128, 132, 133].

The requirements $K > 1$ and $|\Delta_S| < 1$ can be captured in a single condition based on parameter μ :

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta_S S_{11}^*| + |S_{12}S_{21}|}. \quad (2.37)$$

Geometrically, μ represents the distance between the centre of the Smith Chart and the nearest point on the load stability circle. Similarly a parameter μ' is defined according to:

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta_S S_{22}^*| + |S_{12}S_{21}|}, \quad (2.38)$$

which corresponds to the distance between the centre of the Smith Chart and the nearest point on the source stability circle. Unconditional stability is guaranteed if $\mu > 1$ or $\mu' > 1$ (note that if $\mu > 1$, then $\mu' > 1$ and vice versa) and the proviso is satisfied.

Initially the analysis of the stability of transistors under large signal conditions is carried out by extracting the large signal equivalent values of the small signal model parameters. These parameter values show a strong dependency on the applied source power. A non-linear simulation is performed in which the transistor is excited with a large signal while applying a small test signal. From the response to this test signal the model parameter values are extracted. The variation in model parameters as a function of operating power causes the two-port stability parameters to vary as well.

Internal stability analysis

Many situations exist where the previously described two-port techniques are insufficient. Examples are multi-port structures, structures for which the Rollett proviso is not guaranteed, or cases where loops are introduced or different modes of instability might occur due the presence of multiple active devices in parallel [134,135]. In these situations the stability of the amplifier should be investigated using system analysis tools.

Throughout this thesis it is assumed that variations of environmental conditions such as temperature and bias voltages, are slow enough for these conditions to be considered constant during the stability analysis. This means that the systems to be analysed can be considered time-invariant and the time-variance of the system [136] can be ignored. In that case, the goal of a system analysis is to find the eigenvalues of the time-invariant component matrix $\mathbf{C}$ in:

$$\Delta \dot{\bar{x}}(t) = \mathbf{C} \cdot \bar{x}(t), \quad (2.39)$$

where $\bar{x}(t)$ is a vector containing the state variables of the system, i.e. the voltages across and the currents through the components defined in $\mathbf{C}$ [137].

Direct analysis of the characteristic system is only possible if the Jacobian matrix of the system can be determined. This is, however, not possible without exact knowledge of the contents of the system and cannot be determined from simulations. A frequency domain analysis can be performed to determine the eigenvalues of $\mathbf{C}$, but generally the required frequency resolution due to the complexity of the system limits the practical value of this direct approach. An indirect method to determine the stability of the linear complex system is by performing a Nyquist analysis of the characteristic determinant [138]. This, however, requires a complete description of the active sources in the system and cannot be based on the stimuli of the system only.

An alternative method is to perform the Nyquist analysis on the Normalised Determinant Function (NDF) [139,140] according to:

$$\text{NDF} = \frac{\Delta}{\Delta_{0N}}, \quad (2.40)$$

where Δ is the determinant of the network parameters and Δ_{0N} is the reduced determinant, the determinant of the passive matrix that results when all dependent sources (active components) are set to zero. Any type of linear network parameters can be used (Z, Y, S, etc.).

The NDF can be constructed by sequentially disabling a single active component. After each step the ratio of determinants with and without the most recently disabled active component is determined and all the results are multiplied:

$$\frac{\Delta}{\Delta_{0N}} = \frac{\Delta}{\Delta_{01}} \cdot \frac{\Delta_{01}}{\Delta_{02}} \dots \frac{\Delta_{0N-1}}{\Delta_{0N}}. \quad (2.41)$$

The ratio of the complete matrix determinant and the determinant of the networks with a single active component disabled is known as the Return Difference (RD). The Return Ratio (RR) [141] is equal to the RD minus 1, so that:

$$\frac{\Delta}{\Delta_{01}} = \text{RR}_1 + 1. \quad (2.42)$$

This implies that the RR can be determined as the gain of a single loop, with the active components of all previously analysed loops disabled. When all RRs are determined the NDF can be obtained using:

$$\text{NDF} = \prod_{n=1}^N (\text{RR}_n + 1). \quad (2.43)$$

Analysis of the individual RRs of which the NDF exists can be performed using the Ohtomo algorithm [142]. If the S-parameters of the active and passive part of the system are known, the effective loop gain G_k of loop k that contributes to the NDF can be determined from:

$$G_k = 1 + \frac{\Delta_{n-k+1}}{\Delta_{n-k}}. \quad (2.44)$$

In this equation n is the number of interconnections between the active and passive part. The reduced determinants are defined as:

$$\Delta_{n-k+1} = \begin{bmatrix} M_{k,k} & M_{k,k+1} & \cdot & M_{k,n} \\ M_{k+1,k} & M_{k+1,k+1} & \cdot & M_{k+1,n} \\ \cdot & \cdot & \cdot & \cdot \\ M_{n,k} & M_{n,k+1} & \cdot & M_{n,n} \end{bmatrix} \quad (2.45)$$

and Δ_{n-k} is the cofactor $(n-k, n-k)$ of $\mathbf{M}_n$.

The matrix $\mathbf{M}_n$ is constructed from the S-parameter of the passive part $\mathbf{S}_{pas}$, the S-parameter of the active part $\mathbf{S}_{act}$ and the identity matrix $\mathbf{I}$ according to:

$$\mathbf{M}_n = \mathbf{S}_{pas} \cdot \mathbf{S}_{act} - \mathbf{I}_n. \quad (2.46)$$

A different approach to judge the stability of the system is from the location of the poles and the zeroes of the system. Pole-zero identification [143] is based on fitting the impedance function at a random node with a quotient of polynomials. The zeroes of the polynomials in the denominator and numerator are the poles and zeroes of the system respectively.

Stability analysis in the non-linear regime is carried out by the superposition of a large signal drive and a small signal test tone. Due to the mixing of these two tones, the system will be excited with the frequencies $n \cdot f_{LS} \pm f_{SS}$, for n is the set of all non-negative integers. This implies that by defining f_{SS} from 0 to $f_{LS}/2$, the entire frequency range is covered.

Power amplifier stability

During the design of a power amplifier, stability is an aspect that needs to be taken into account from the very beginning, starting with the analysis of the stability of the individual transistors. This can usually be performed using the two-port techniques. For a Stacked-FET power amplifier this is followed by the analysis of the stacks, where similar two-port techniques can be applied, although with more care with respect to the Rollett proviso. For the stability analysis of the entire Stacked-FET power amplifier, two port techniques are insufficient. This analysis is therefore performed by means of the internal stability techniques, in particular through pole-zero identification with third-party analysis software. The stability analyses of Stacked-FETs and Stacked-FET amplifier, and more specific the incorporation of these analyses into the design strategy is the subject of chapter 5.

2.5 Conclusion

The output power level of HPA MMICs in III-IV technologies are compatible with the required power levels for AESA front-ends. Often these MMICs are packaged in plastic QFN packages which are well suited for application up to X-band due to absence of leads. Typical sizes of the devices make it possible to design RF front-ends that fit within the available physical space for such front-ends.

The maximum operating frequency and efficiency of a transistor depend on the selected operating class of that transistor. Popular classes for integrated microwave amplifiers are, beside the classical class-A, class-B, class-E and class-F⁽⁻¹⁾. Continuous classes are seldom demonstrated at MMIC level. The stacking of transistors increases the maximum allowed voltage swing on an amplifier stage, which makes it possible to increase the drain supply voltage on the stage. This has the advantage of lower supply currents for a given level of output power. The dimensioning of these Stacked-FETs will be the subject of the next chapter.

CHAPTER 3

Stacked-FET dimensioning

3.1 Introduction

In the previous chapter Stacked-FETs were introduced as building blocks for power amplifiers with a drain supply voltage higher than supported by the individual transistors. In this chapter a procedure is developed to dimension the Stacked-FET in such a way that the voltages and currents are equal and in-phase for all transistors in the Stacked-FET. It is discussed which external balancing components are required for this current and voltage equalisation and how the required values of these components can be determined. A Stacked-FET consisting of N FETs as shown in Figure 3.1 is analysed. The Stacked-FET consists of a single CS transistor followed by M DCG transistors. Both the DC and RF part of the total drain voltage are distributed evenly over the $N = M + 1$ transistors in the Stacked-FET such that the total drain voltage can be equal to N times the maximum drain voltage of a single FET.

Figure 3.1: Stack of $M+1$ FETs without biasing and balancing components.

The Stacked-FET will operate in one of the classes described in the previous chapter. The selected quiescent DC current density determines the required gate-to-source voltages for the transistors in the stack. Details with respect to the possible harmonic terminations of the individual transistors in the the stack are given in section 3.9 .

During the design of the Stacked-FET, the individual stack transistors are treated independently. The first step is the design of the CS transistor. The optimum transistor load for the selected operating class is determined and the stability of the individual transistor is analysed. The remaining transistors of the Stacked-FET, the DCG transistors, are balanced by applying properly dimensioned components external to the transistor. During the procedure to determine the values of these component a requirement is obtained for the optimum loading of the DCG transistor concerned. This balancing of the DCG FET is repeated for each succeeding DCG transistor, the obtained load requirement for the final DCG transistor is the requirement for the load of the entire Stacked-FET. Based on the known transistor characteristics and values for balancing components the stability of the individual transistor is analysed.

Initially the parasitic components of the transistors are ignored and the dimensioning is based on an idealised FET model containing the intrinsic part only. In a later stage the parasitic capacitances are accounted for. The parasitic resistances and inductances are included in the simulations.

3.2 Transistor 1, CS transistor

The first transistor in the Stacked-FET to be considered is the CS transistor. The considerations for this CS transistor are not different than for an ordinary CS based power amplifier. Calculations on the CS transistor are based on the single simplified small-signal CS FET model shown in Figure 3.2.

Figure 3.2: CS simplified small-signal model.

In the first place the optimum loading of the CS FET is determined. After this the voltage relations inside the CS FET are determined. Both this transistor load and the internal voltage relations are to be made equal for all the transistors in the Stacked-FET. This internal relation, as determined on the CS transistors, are translated to the DCG transistors, are therefore used at a later stage during the balancing of the DCG FETs. The goal of the dimensioning of the balancing components of the DCG transistors is to equalise the internal voltages and currents such that the load lines of all transistors in the Stacked-FET are equal.

3.2.1 Optimum load

The first order parameters describing the technology with respect to its power performance are given in Table 3.1. These parameters dominate the output power and efficiency that can be obtained from a single transistor. Further, they also determine the loading conditions for maximum output power.

Table 3.1: Technology parameters.

Parameter	Unit	Description
$R_{ds_{on}}$	$\Omega \cdot \text{mm}$	Transistor on-resistance in linear region
I_{max}	mA/mm	Transistor maximum current
V_{br}	V	Transistor breakdown voltage
C_{gd}	fF/mm	Intrinsic gate-to-drain capacitance
C_{ds}	fF/mm	Intrinsic drain-to-source capacitance

The optimum load of the CS FET can be obtained from:

- The FET output characteristic, according to the Cripps method [53].
- Load pull simulations, which requires an accurate non-linear model.
- Load pull measurements; this is the most accurate method.

The Cripps method provides the best insight in the optimum loading conditions. It states that the real part of the load presented to the transistor must fit the idealised DC-IV curves of the FET and follows from an analysis given in section 2.2.2 for class-B operation. In that case $G_{opt,int} = 0.5I_{max}/(V_{dd} - V_k)$ according to Figure 3.3. The knee voltage V_k is obtained from the on-resistance and the maximum current: $V_k = I_{max}R_{ds_{on}}$. The imaginary part must compensate the reactive elements C_{out} at the transistor output. Based on the model that was given in Figure 3.2, C_{out} is given by:

$$C_{out} = \frac{C_{ds} + C_{gd}}{1 - \frac{j\omega C_{gd}}{g_m}}. \quad (3.1)$$

Since in practise $g_m \gg \omega C_{gd}$, this can be simplified to:

$$C_{out} \approx C_{ds} + C_{gd}. \quad (3.2)$$

The optimum load admittance of the CS transistor is therefore:

$$Y_{L,CS} \approx \frac{I_{max}}{2(V_{dd} - I_{max}R_{ds_{on}})} - j\omega(C_{ds} + C_{gd}). \quad (3.3)$$

Figure 3.3: Optimum load definition according to Cripps method.

3.2.2 Voltage relations

In this section the ratio between the internal gate-to-source voltage v_{gs} and the internal drain-to source voltage v_{ds} are determined. This ratio will be used later during the balancing of the DCG FETs. Admittances Y_{ds} and Y_{gd} are defined according to:

$$Y_{ds} = j\omega C_{ds} + \frac{1}{R_{ds}} \quad (3.4)$$

and:

$$Y_{gd} = j\omega C_{gd}. \quad (3.5)$$

Applying Kirchhoff's Current Law (KCL) to the drain terminal of the FET in Figure 3.2 gives:

$$\begin{aligned} -v_{ds}Y_{L,CS} - v_{ds}Y_{ds} - v_{gs}g_m + v_{gd}Y_{gd} = \\ -v_{ds}Y_{L,CS} - v_{ds}Y_{ds} - v_{gs}g_m + v_{gs}Y_{gd} - v_{ds}Y_{gd} = 0. \end{aligned} \quad (3.6)$$

Eqn. (3.6) can be written as:

$$\frac{v_{gs}}{v_{ds}} = \frac{Y_{L,CS} + Y_{ds} + Y_{gd}}{Y_{gd} - g_m}, \quad (3.7)$$

with which the required voltage ratio is found. This ratio will be used in section 3.3.2 to determine an external gate-side impedance to balance the voltage over successive DCGs after which in section 3.3.3 the currents will be equalised.

3.3 Transistor 2 to N, Degenerated Common Gate transistors

The goal of the DCG balancing is to equalise the internal voltages and currents for all the transistor in the Stacked-FET. Based on the selected loading for the intrinsic transistors the components to balance the DCG transistor are determined. For transistor n in the Stacked-FET, the internal drain current and drain-to-source voltage swings should be equal to and in-phase with the voltage and current of transistor $n - 1$.

3.3.1 DCG excitation

Several options exist to excite the gates of the DCG transistors. Three reported options are illustrated in Figure 3.4. The first one uses transformers to directly drive the gate-to-source junctions of the DCG FETs [76]. Such transformers are bulky components and therefore this option is considered not desirable. In the

second option a resistive feedback ladder is used to generate the required gate voltages from the overall drain voltage of the Stacked-FET [75]. This feedback network provides additional modes for oscillations and reduces the overall efficiency since part of the generated RF power is fed back into the resistive divider. For these reasons this mechanism is not used. The third option derives the required gate voltage from the DCG source voltage by a capacitive division between the intrinsic gate-to-source capacitance and external gate capacitance [74]. This option is considered the most elegant since it locally generates the required gate voltages with an minimum amount of additional components. The exact dimensioning of these capacitances is treated in section 3.3.2.

Figure 3.4: Options for DCG excitation, (a) direct to gate-to-source, (b) resistive feedback and (c) capacitive division via C_{gs} .

The simplified small-signal model of a single DCG transistor used in the analysis is shown in Figure 3.5. This model is obtained from the model in Figure 3.2. The external gate component for the excitation of the DCG gate is represented by Y_{gX} . The load admittance of the DCG transistor in the stack, Y_L , is either the input admittance of the next DCG transistor (if $n < N$), or the external load admittance (if $n = N$).

Figure 3.5: Common gate simplified small-signal model.

3.3.2 Voltage equalisation

In this section the value of Y_{gX} is determined such that the ratio between the gate-to-source voltage and the drain-to-source voltage in the DCG transistor are equal to that in the CS transistor.

The RF drain-to-source voltages of all transistors in the Stacked-FET should be equal. Due to this requirement the drain voltage $v_{d,n}$ of FET n equals:

$$v_{d,n} = n v_{ds} \quad (3.8)$$

and the source voltage $v_{s,n}$ equals:

$$v_{s,n} = v_{d,n-1} = (n-1) v_{ds}. \quad (3.9)$$

Finally the gate voltage $v_{g,n}$ equals:

$$v_{g,n} = v_{s,n} + v_{gs} = (n-1) v_{ds} + v_{gs}. \quad (3.10)$$

An admittance Y_{gs} is defined according to:

$$Y_{gs} = j\omega C_{gs}. \quad (3.11)$$

Applying KCL to the gate terminal (g) yields:

$$-v_{g,n} Y_{gX,n} - (v_{g,n} - v_{s,n}) Y_{gs} - (v_{g,n} - v_{d,n}) Y_{gd} = 0. \quad (3.12)$$

The gate voltage $v_{g,n}$ can now be written as:

$$v_{g,n} = \frac{v_{s,n} Y_{gs} + v_{d,n} Y_{gd}}{Y_{gX,n} + Y_{gs} + Y_{gd}}. \quad (3.13)$$

Substitution of Eqn. (3.8), Eqn. (3.9) and Eqn. (3.10) into Eqn. (3.13) yields:

$$(n-1)v_{ds} + v_{gs} = \frac{(n-1)v_{ds}Y_{gs} + nv_{ds}Y_{gd}}{Y_{gX,n} + Y_{gs} + Y_{gd}}. \quad (3.14)$$

This gives:

$$(n-1) + \frac{v_{gs}}{v_{ds}} = \frac{(n-1)Y_{gs} + nY_{gd}}{Y_{gX,n} + Y_{gs} + Y_{gd}}. \quad (3.15)$$

Substitution of Eqn. (3.7) into Eqn. (3.15) gives:

$$\frac{Y_{L,CS} + Y_{ds} + Y_{gd}}{Y_{gd} - g_m} + (n-1) = \frac{(n-1)Y_{gs} + nY_{gd}}{Y_{gX,n} + Y_{gs} + Y_{gd}}. \quad (3.16)$$

Isolation of Y_{gX} yields:

$$Y_{gX,n} = \frac{((n-1)Y_{gs} + nY_{gd})(Y_{gd} - g_m)}{Y_{L,CS} + Y_{ds} + nY_{gd} - (n-1)g_m} - Y_{gs} - Y_{gd}, \quad (3.17)$$

with which the unknown gate admittance $Y_{gX,n}$ is expressed in terms of known model parameters.

3.3.3 Current equalisation

The loading conditions of each transistor in the stack should be equal. This means that besides the drain-to-source voltages of the transistors, also the drain currents should be equal. In order to properly combine the generated RF-powers of all transistors in the stack, both these voltages and currents of the transistors should be in-phase. Both criteria are achieved by imposing that for each transistor the output current should be equal to the input current:

$$i_{out,n} = i_{in,n} = i_{out,n-1}. \quad (3.18)$$

Due to the shunt current paths through the external gate capacitors some of the input current flows to ground, which means that a correction current i_{cor} needs to be supplied to the input terminal as indicated in Figure 3.6.

3.3. TRANSISTOR 2 TO N, DEGENERATED COMMON GATE TRANSISTORS

Figure 3.6: Correction current supplied to source of DCG transistor for current balancing.

Application of KCL to the input node gives:

$$i_{in,n} + v_{ds}Y_{ds} + g_mv_{gs} + v_{gs}Y_{gs} + i_{cor} = 0. \quad (3.19)$$

Application of KCL to the output node gives:

$$\begin{aligned} i_{out,n} &= v_{ds}Y_{ds} + g_mv_{gs} - v_{gd}Y_{gd} = \\ &v_{ds}Y_{ds} + g_mv_{gs} - (v_{gs} - v_{ds})Y_{gd}. \end{aligned} \quad (3.20)$$

Combining Eqn. (3.18), Eqn. (3.19) and Eqn. (3.20) yields:

$$\begin{aligned} v_{ds}Y_{ds} + g_mv_{gs} + v_{gs}Y_{gs} + i_{cor} &= \\ v_{ds}Y_{ds} + g_mv_{gs} - (v_{gs} - v_{ds})Y_{gd}, \end{aligned} \quad (3.21)$$

which gives for i_{cor} :

$$i_{cor} = -(Y_{gs} + Y_{gd})v_{gs} + Y_{gd}v_{ds}. \quad (3.22)$$

Eqn. (3.22) gives the value of required correction current, which needs to be supplied by a Current Balancing Component (CBC). The three implementations of this CBC, shown in Figure 3.7, are:

- A component to ground; the required correction for transistor n , denoted by $i_{cor_{shunt},n}$, is supplied by component $Y_{sX,n}$.
- A component to the drain of same transistor n ; the required correction for transistor n , denoted by $i_{cor_{ds},n}$, is supplied by the external drain-to-source admittance $Y_{dsX,n}$. This option corresponds to the approach introduced in [98].

- (c) A component to the drain of the top transistor N ; the required correction for transistor n , denoted by $i_{cor_{dN},n}$, is supplied by component $Y_{dNsX,n}$.

Each option is explored in the next section. In section 3.8.1 a preferred option is selected based on fundamental and practical aspects.

Figure 3.7: Options for current equalisation, (a) correction current via component $Y_{sX,n}$ to ground, (b) correction current via component $Y_{dsX,n}$ to the drain of transistors n , (c) correction current via component $Y_{dNsX,n}$ to the drain of transistors N .

Note that in literature two more methods for Stacked-FET balancing are described:

- The first method [81] uses no CBC, instead the values of external gate admittance $C_{gX,n}$ and applied load admittance $Y_{L,n}$ of transistor n are tuned to present the optimum load to transistor $n - 1$. If this transistor is the CS transistor, this optimum load admittance $Y_{L,n-1}$ is equals to the CS admittance $Y_{L,CS}$. If, however, transistor $n - 1$ is a DCG transistor, this optimum load admittance $Y_{L,n-1}$ is in turn dependent on the tuned gate capacitance value $C_{gX,n-1}$. By using this method the individual DCG transistors in the stack are not loaded with the absolute optimum load admittance, which results in gain and output power reduction.
- A second method [88] uses a series inductor to tune the input admittance of transistor n to the required load admittance of transistor $n - 1$. Also for this technique the gate capacitance $C_{gX,n}$ needs to be modified. The RF voltage drop on the series components reduces the total output power capability and hence efficiency of the Stacked-FET.

Component to ground (a)

If the correction current source of transistor n is supplied via a component $Y_{sX,n}$ to ground, the voltage across this component is $(n-1)v_{ds}$ which in combination with Eqn. (3.22) gives:

$$Y_{sX,n} = \frac{i_{cor_{shunt},n}}{(n-1)v_{ds}} = (Y_{gs} + Y_{gd}) \frac{v_{gs}}{(n-1)v_{ds}} - \frac{Y_{gd}}{n-1}. \quad (3.23)$$

Combined with Eqn. (3.7) this gives:

$$Y_{sX,n} = (Y_{gs} + Y_{gd}) \frac{Y_{L,CS} + Y_{ds} + Y_{gd}}{(n-1)(Y_{gd} - g_m)} - \frac{Y_{gd}}{n-1}. \quad (3.24)$$

By using Eqn. 3.24 the required shunt admittance at each DCG source terminal can be determined.

External drain-to-source component (b)

The correction current for any transistor in the Stacked-FET can be obtained from the drain connection of that transistor. In that case the current source is implemented as an external drain-to-source component $Y_{dsX,n}$. For this configuration the correction current for transistor $n-1$ has to be supplied by transistor n which means that for this transistor n the correction current has an additional term $Y_{dsX,n-1}v_{ds}$ besides Eqn. (3.22):

$$i_{cor_{ds},n} = -(Y_{gs} + Y_{gd})v_{gs} + Y_{gd}v_{ds} + Y_{dsX,n-1}v_{ds}. \quad (3.25)$$

The voltage across the component is v_{ds} which in combination with Eqn. (3.25) gives:

$$Y_{dsX,n} = \frac{i_{cor_{ds},n}}{v_{ds}} = -(Y_{gs} + Y_{gd}) \frac{v_{gs}}{v_{ds}} + Y_{gd} + Y_{dsX,n-1}. \quad (3.26)$$

Combined with Eqn. (3.7) this gives:

$$Y_{dsX,n} = -(Y_{gs} + Y_{gd}) \frac{Y_{L,CS} + Y_{ds} + Y_{gd}}{Y_{gd} - g_m} + Y_{gd} + Y_{dsX,n-1}. \quad (3.27)$$

Since for transistor n (the CS transistor) $Y_{dsX,1} = 0$, Eqn. (3.27) shows recursive behaviour and can be written as:

$$Y_{dsX,n} = (n-1) \left[Y_{gd} - (Y_{gs} + Y_{gd}) \frac{Y_{L,CS} + Y_{gd} + Y_{ds}}{Y_{gd} - g_m} \right]. \quad (3.28)$$

Eqn. 3.28 gives the required external drain-to-source admittance to provide the correction current to the source of transistor n .

Component to drain of transistor N (c)

The third option to implement the correction current source for transistor n is with a component $Y_{dNsX,n}$ from the source of the transistor to the drain of transistor N . In this case the voltage across the component is $(N - n + 1)v_{ds}$ which in combination with Eqn. (3.22) gives:

$$Y_{dNsX,n} = \frac{i_{cor_{dNsX,n}}}{(N - n + 1)v_{ds}} = - (Y_{gs} + Y_{gd}) \frac{v_{gs}}{(N - n + 1)v_{ds}} + \frac{Y_{gd}}{N - n + 1}. \quad (3.29)$$

Combined with Eqn. (3.7) this gives:

$$Y_{dNsX,n} = - (Y_{gs} + Y_{gd}) \frac{Y_{L,CS} + Y_{ds} + Y_{gd}}{(N - n + 1)(Y_{gd} - g_m)} + \frac{Y_{gd}}{N - n + 1}, \quad (3.30)$$

which gives the required admittance from the source terminal of transistor n to the drain of transistor N .

3.3.4 Load of transistor N

When the optimum values for the balancing components are known, the optimum load admittance for the Stacked-FET can be defined. As the optimum load depends on the implementation of CBC, each option will be treated individually.

With component to ground (a)

The voltage at the load is $N \cdot v_{ds}$, while the current is equal to $-i_{ds}$. The load admittance is therefore:

$$Y_{L,stack} = Y_{L,N} = \frac{-i_{ds}}{N \cdot v_{ds}} = \frac{Y_{L,CS}}{N}. \quad (3.31)$$

Eqn. (3.31) shows that for this CBC implementation, the optimum load admittance of the stack scales inversely proportional with the number of transistors in the stack.

With external drain-to-source component (b)

In this case the current at the load is equal to $-i_{ds} - i_{dsX,N}$ while the voltage at the load is $N \cdot v_{ds}$. Since the voltage across each compensation element is equal to v_{ds} this gives:

$$Y_{L,stack} = \frac{-i_{ds} - i_{dsX,N}}{N \cdot v_{ds}} = \frac{Y_{L,CS} - Y_{dsX,N}}{N}. \quad (3.32)$$

According to Eqn. (3.32), the optimum load admittance of the stack reduces as the number of stacked transistors increases.

With parallel components to drain N (c)

If the compensation components are all connected to the drain of FET N , the currents through these components are drawn from the load which means the current at the load is $-i_{ds} - \sum_{n=1}^N i_{cor_{d_N sX,n}}$. The voltage across each compensation element is equal to $(N - n + 1)v_{ds}$ which implies the current through these components is $(N - n + 1)v_{ds}Y_{dsX,n}$. Since the voltage at the load is $N \cdot v_{ds}$ this yields a load admittance of:

$$\begin{aligned} Y_{L,stack} &= \frac{-i_{ds} - \sum_{n=2}^N i_{cor_{d_N sX,n}}}{N \cdot v_{ds}} = \\ &= \frac{Y_{L,CS} - \sum_{n=2}^N (N - n + 1) \cdot Y_{d_N sX,n}}{N} = \\ &= \frac{Y_{L,CS} - \sum_{n=2}^N n \cdot Y_{d_N sX,n}}{N}. \end{aligned} \quad (3.33)$$

Also for this CBC option the optimum load admittance of the stack is inversely proportional to the number of transistors in the stack.

3.4 Parasitic capacitances

In Figure 3.8, a Stacked-FET with two transistors is depicted, including the parasitic capacitances C_{pd} , C_{ps} and C_{pg} of the transistors. The corresponding admittances for these capacitances are $Y_{pd} = j\omega C_{pd}$, $Y_{ps} = j\omega C_{ps}$ and $Y_{pg} = j\omega C_{pg}$ respectively. Although the Stacked-FET consists of transistors with equal sizes, some asymmetry arises due to the difference in transistor layout between the DCG and CS FETs. This means the parasitic capacitances, determined by the extrinsic metal in the transistor layout, will be different for the DCG and CS FETs. Furthermore, the voltages across the parasitic capacitances, that are connected to ground, are different for each transistor in the stack. This means that the voltages across these capacitances and hence the current through these capacitances are also different. The effect of these parasitic capacitances is analysed in this section.

The influence of the parasitic inductances and access resistances are initially ignored during the dimensioning of the Stacked-FET.

Figure 3.8: Parasitic capacitors in stack of 2 FETs.

3.4.1 Translation of CS transistor load

One of the goals of the voltage and current balancing is that the intrinsic parts of all transistors in the Stacked-FET are equally loaded. In other words, the intrinsic transistor load of the DCG transistors should be equal to the internal CS transistor load $Y_{L,CS}$. The optimum transistor load obtained during load pull measurements or simulations contains the effect of the parasitic drain capacitance Y_{pd} and is referred to as $Y_{L,CS_{ext}}$. This internal CS transistor load $Y_{L,CS}$ is determined from the known external load $Y_{L,CS_{ext}}$ according to:

$$Y_{L,CS} = Y_{L,CS_{ext}} + Y_{pd}. \quad (3.34)$$

Eqn. (3.34) gives the load to be applied to all intrinsic transistors in the Stacked-FET.

3.4.2 Effect on voltage equalisation

As can be seen from Figure 3.8 the parasitic gate capacitance C_{pg} is parallel to the external gate admittance $Y_{gX,n}$. This means that the effect of C_{pg} can be taken into account by decreasing the obtained $Y_{gX,n}$ from Eqn. (3.17) with a value Y_{pg} :

$$Y_{gX,n} = \frac{((n-1)Y_{gs} + nY_{gd})(Y_{gd} - g_m)}{Y_{L,CS} + Y_{pd} + Y_{ds} + nY_{gd} - (n-1)g_m} - Y_{gs} - Y_{gd} - Y_{pg,n}. \quad (3.35)$$

Eqn. (3.35) implies $Y_{pg,n}$ can be compensated and will have no effect on the stack performance.

3.4.3 Effect on current equalisation

Parallel to the correction current, at the source of transistor n , are the parasitic capacitances $C_{pd,n-1}$ and $C_{ps,n}$. The voltage across these capacitances is $(n-1)v_{ds}$ which means that the term $(n-1)v_{ds}(Y_{ps,n} + Y_{pd,n-1})$ should be added to the correction current:

$$i_{cor} = -(Y_{gs} + Y_{gd})v_{gs} + Y_{gd}v_{ds} + (n-1)v_{ds}(Y_{ps,n} + Y_{pd,n-1}). \quad (3.36)$$

The effect depends on the correction current source implementation that is used. Each variant is discussed in the next sections.

Component to ground (a)

If the correction current at source n is applied via a component $Y_{sX,n}$ to ground, this component is directly parallel to the parasitic capacitances $C_{ps,n}$ and $C_{pd,n-1}$ and needs to be corrected with these values. The required admittance is now given by:

$$Y_{sX} = (Y_{gs} + Y_{gd}) \frac{Y_{L,CS} + Y_{ds} + Y_{gd}}{(n-1)(Y_{gd} - g_m)} - \frac{Y_{gd}}{n-1} - Y_{pd,n-1} - Y_{ps,n}. \quad (3.37)$$

Eqn. 3.37 shows that these parasitic capacitances can be compensated entirely.

External drain-to-source component (b)

In the case of an external drain-to-source component the correction current should be compensated for the parasitic capacitances $C_{ps,n}$ and $C_{pd,n-1}$. This means that the term $Y_{pd,k-1} + Y_{ps,k}$ should be added to $Y_{dsX,n}$ in Eqn. (3.27), which yields:

$$Y_{dsX,n} = (n - 1) \cdot$$

$$\left[Y_{gd} - (Y_{gs} + Y_{gd}) \frac{Y_{L,CS} + Y_{gd} + Y_{ds}}{Y_{gd} - g_m} + Y_{pd,k-1} + Y_{ps,k} \right]. \quad (3.38)$$

Not that in contrast to the CBC implementation with a component to ground, the value of the required admittance is increased.

Component to drain of transistor N (c)

In the case of a parallel component to drain N , the current through the parasitic capacitances $C_{ps,n}$ and $C_{pd,n-1}$ should be provided by this parallel component:

$$Y_{dNsX,n} = -(Y_{gs} + Y_{gd}) \frac{Y_{L,CS} + Y_{ds} + Y_{gd}}{(N - n + 1)(Y_{gd} - g_m)} + \frac{Y_{gd}}{N - n + 1} + (n - 1)(Y_{pd,k-1} + Y_{ps,k}). \quad (3.39)$$

Also here the required admittance value is increased due to the parasitic capacitances.

3.4.4 Stacked-FET load

The parasitic drain capacitance $C_{pd,N}$ of FET N is parallel to the external load and should be compensated for. This means the Stacked-FET load Y_L equals:

$$Y_{L,sX} = \frac{Y_{L,CS}}{N} - Y_{pd,N} \quad (3.40)$$

in the case of component to grounds,

$$Y_{L,dSX} = \frac{Y_{L,CS} - Y_{dsX,N}}{N} - Y_{pd,N} \quad (3.41)$$

in the case of external drain-to-source capacitors and

$$Y_{L,dNsX} = \frac{Y_{L,CS} - \sum_{n=2}^N n \cdot Y_{dNsX,n}}{N} - Y_{pd,N} \quad (3.42)$$

in the case of a parallel components to drain of transistor N . In all cases the parasitic capacitances result in a constant offset in the optimum stack load versus number of transistors in the stack.

3.5 Power dependency of model parameter values

The description of the Stacked-FET operation principle that was given in the previous sections is based on the small-signal models of the CS and DCG FETs. In order to optimise the Stacked-FETs in the large signal regime, the non-linear equivalences of the small-signal parameters should be determined. This will be performed by extracting the linearised values at a large signal operating power. By using these equivalent parameter values the small-signal analysis may still be applied.

Two methods are described to determine the effective model parameter values under large signal operation. The first method is a non-linear simulation from which the 'hot S-parameters' are derived. From these 'hot S-parameters' the effective model parameters are extracted. A drawback of this method is that it depends on the accuracy of the non-linear model that is used for the simulation.

A second method is based on the extraction of the model parameters from the small-signal S-parameters measured over the V_{ds} - V_{gs} bias plane. For this method the transistor load line is estimated, based on the current and voltage waveforms corresponding to the selected operating class. The weighted average of the model parameters along this load line is taken as the effective large signal equivalent.

3.5.1 Effective model parameter values from harmonic balance simulation

The effective model parameters are extracted from the 'hot S-parameters', derived from the non-linear model of the transistor. A non-linear simulation is performed in which the transistor is excited with a large signal at a frequency of 3.1 GHz, while a small test signal is applied simultaneously. From the response to this test signal the model parameter values are extracted [108]. The extracted component values of a 8x350 μm FET at a small signal test frequency of 3 GHz are shown in Figure 3.9 versus applied source power. It is found that the capacitances C_{gd} and C_{ds} have a nearly constant value of 280 fF and 850 fF respectively over the entire power range. The capacitance C_{gs} varies from its small-signal value of approximately 4.5 pF, down to a value of approximately 3 pF in the high power range. The value of the transconductance g_m , which is around 0.75 S in the small signal range, reduces to approximately 0.3 S as the source power increases.

Figure 3.9: Model parameters versus source power of $8 \times 350 \mu\text{m}$ transistor, $f_{LS}=3.1 \text{ GHz}$, $f_{SS}=3.0 \text{ GHz}$.

3.5.2 Effective model parameter values from small-signal measurements

The second method to determine the large signal equivalent model parameter values, is by averaging along the transistor load line. For this method the S-parameters are measured versus V_{ds} and V_{gs} . From these S-parameters the small-signal intrinsic FET-model parameters are determined for all the measured points [144]. Bias combinations of high values for drain and gate voltage that yield a dissipated power above a pre-defined limit are not considered, as they violate the equithermal assumptions. The measurement is performed on a $4 \times 100 \mu\text{m}$ transistor and the extracted values of C_{ds} , C_{gd} , C_{gs} and g_m are linearly scaled to an equivalent value for the $8 \times 350 \mu\text{m}$ transistor. The results are given in Figure 3.10. The S-parameter measurements on which the parameter extraction is based are performed from a drain voltage from 0 V to 15 V and a gate voltage from -5 V to 0 V. For the bias point with high gate voltage and low drain voltage, the device becomes unstable during the measurements. This is typically the case when both $V_{ds} < 3 \text{ V}$ and $V_{gs} > -0.5 \text{ V}$. Therefore no reliable data can be extracted in this region.

3.5. POWER DEPENDENCY OF MODEL PARAMETER VALUES

Figure 3.10: Extracted small-signal model parameters versus bias.

To estimate the large signal equivalent parameter values, the drain and gate voltage waveforms for the transistor should be determined. In the HPA, the drain and gate voltage waveforms for the transistors heavily depend on the class of operation. For class B operation, which was discussed in section 2.2.2, the drain voltage is sinusoidal with a minimum that reaches the knee voltage of the transistor. The gate voltage waveform is defined taking into account the non-linear relation between drain current and gate voltage due to the presence of the gate-to-source diode. This is achieved by defining the gate voltage as the square-root of the drain current. The load line is plotted in the model parameter contours in Figure 3.11.

Figure 3.11: Class-B stimulus line in small-signal model parameter contours.

The drain and gate voltage waveforms together with the model parameters at the corresponding points are given in Figure 3.12. The average values of these parameters are taken as effective values for the given excursion lines. Not all required data points are reliable as the excursion line goes through the region with low V_{ds} and high V_{gs} where the device tends to be unstable. As a result the component values at these instances are absent in the model parameter traces of Figure 3.12.

Figure 3.12: Small-signal model parameters, valid for Class B, non-linear V_{gs} stimulus line.

3.5.3 Comparison of the simulated and extracted model parameters

A comparison between the results from the two methods is given in Table 3.2 and significant differences are found. A possible explanation is in the limited

availability of small signal parameter data in the range of low V_{ds} and high V_{gs} . The data obtained from the simulation is therefore judged as more reliable and this method is used further throughout this thesis. Possible solutions to increase the reliability of the extracted data is by stabilising the S-parameter measurement setup, for example by improved low frequency damping.

Table 3.2: Equivalent model parameters.

Parameter	Unit	From model	From S-parameter measurements
C_{gs}	pF	2.5	2.04
C_{ds}	fF	850	588
C_{gd}	fF	280	312
g_m	S	0.3	0.48

3.6 Numerical example

The process of stack balancing is illustrated through the design of a stack consisting of three $8 \times 350 \mu\text{m}$ transistors. A motivation for the use of transistors with these dimensions will be given in chapter 6. The intrinsic and extrinsic model parameter values that are used to dimension the balancing components of the stack are given in Table 3.3. The frequency dependent CS load, used as a starting point for the stack design, is selected as a compromise between output power and PAE, and modelled as the admittance $Y_{CS,ext} = 0.05 - j\omega \cdot 1.3 \cdot 10^{-12}$.

Table 3.3: Model parameters $8 \times 350 \mu\text{m}$ FET, $f=3 \text{ GHz}$, $V_{ds}=8 \text{ V}$, $V_{gs}=-1.5 \text{ V}$.

Parameter	Unit	Value
C_{ds}	pF	0.85
C_{gs}	pF	2.5
C_{gd}	pF	0.28
g_m	S	0.3
C_{pd}	fF	176
C_{ps}	fF	176
C_{pg}	fF	23.8

3.6.1 Gate admittance for voltage equalisation

The required gate admittance for voltage equalisation Y_{gX} according to Eqn. (3.35) is shown in Figure 3.13. Over the entire frequency range the imaginary parts of the required admittances increase linearly with frequency and can hence be implemented as capacitors. $\Im Y_{gX,2}$ is larger than $\Im Y_{gX,3}$ which means that the largest capacitance is required for the first DCG transistor. The real parts of both

the admittances $Y_{gX,2}$ and $Y_{gX,3}$ are negative. The second plot of the figure gives the ratios between the real and imaginary parts of the required admittance. It can be seen that for low frequency these ratios are small, while they linearly increase with frequency. For frequencies below approximately 5 GHz, these ratios are smaller than 5 % and can be ignored. The implementation of the negative real parts at higher frequencies requires an active network [145] and is not practically feasible due to the expected demands on dynamic range and the implications for stability.

Figure 3.13: Required external gate admittance for voltage equalisation, $C_{ds} = 850$ fF, $C_{gd} = 280$ fF, $C_{gs} = 2.5$ pF and $g_m = 0.3$ S.

3.6.2 Component values for current equalisation

With component to ground (a)

The required shunt admittance for current equalisation Y_{sX} according to Eqn. (3.37) is shown in Figure 3.14. The required imaginary parts decrease linearly with frequency which require non-Foster networks [146], which are not implementable in a passive manner. An active implementation [147–149] is not feasible due to the high voltage swings at the gates. Over a limited frequency band the imaginary part can be approximated by an inductance to ground. The real parts of both the admittances $Y_{gX,2}$ and $Y_{gX,3}$ are negative, but smaller than 5 % of the imaginary part over the entire frequency range.

Figure 3.14: Required drain shunt admittance for current equalisation, with Y_{sX} being the component to ground, $C_{ds} = 850$ fF, $C_{gd} = 280$ fF, $C_{gs} = 2.5$ pF and $g_m = 0.3$ S.

With external drain-to-source component (b)

The external drain-to-source admittance for current equalisation Y_{dsX} according to Eqn. (3.38) is shown in Figure 3.15. Over the entire frequency range the imaginary parts of the required admittances increase linearly with frequency and can hence be implemented as capacitors. The real parts of both the admittances $Y_{dsX,2}$ and $Y_{dsX,3}$ are negative, but smaller than 5 % of the imaginary parts over the entire frequency range.

Figure 3.15: Required external drain-to-source admittance Y_{dsX} for current equalisation, $C_{ds} = 850$ fF, $C_{gd} = 280$ fF, $C_{gs} = 2.5$ pF and $g_m = 0.3$ S.

With component to drain of N (c)

The external admittance from source n to the drain of FET N Y_{dNsXX} according to Eqn. 3.39 is shown in Figure 3.16. Over the entire frequency range the imaginary parts of the required admittances increase linearly with frequency and can hence be implemented as capacitors. The real parts of both the admittances $Y_{dNsXX,2}$ and $Y_{dNsXX,3}$ are negative, however, the ratios between the real and imaginary parts are below 2 % up to a frequency of 14 GHz..

Figure 3.16: Required external admittance Y_{dNsX} to drain of transistor N for current equalisation, $C_{ds} = 850$ fF, $C_{gd} = 280$ fF, $C_{gs} = 2.5$ pF and $g_m = 0.3$ S.

3.6.3 Stacked-FET load

The required Stacked-FET loads for the different compensation methods are given in Figure 3.17. For all compensation methods the load contains a positive real part and negative imaginary part that decreases linearly as a function of frequency. Depending on the implementation of the CBC, the real part shows a frequency dependent behaviour. At the frequency band of interest, however, it may be considered constant. This implies that for each method the required load can be modelled with a parallel RC network. The imaginary part and hence the required capacitance shows a large variation between the CBC options. This capacitive part is the smallest for the shunt implementation and the largest for the implementation with a component to drain of transistor N .

Figure 3.17: Required load admittance for stack of three $8 \times 350 \mu\text{m}$ transistors, $V_{dd}=24 \text{ V}$, $V_{gs}=-1.5 \text{ V}$.

Figure 3.18: Output power versus load mismatch for $3 \times 8 \times 350 \mu\text{m}$ Stacked-FET, $V_{dd}=24 \text{ V}$, $V_{gs}=-1 \text{ V}$, $f=3 \text{ GHz}$.

The sensitivity of the Stacked-FET to load mismatch is simulated with the non-linear model, the result is shown in Figure 3.18. If the calculated load admittance is applied, $|\Gamma_L^m|=0$, the simulated output power is 37.4 dBm. For a small mismatch $|\Gamma_L^m| = -26 \text{ dB}$, the output power varies with the phase of the load over a window of approximately 0.3 dB. Note that for a phase angle around 100° the output power increases, this is due to the fact that the selected internal load admittance of the transistors in the stack is a compromise between output power and PAE. At this specific mismatch the internal load moves toward a load that is optimal for output power. Larger mismatch values result in higher power losses. If a loss of 0.5 dB is defined as acceptable, the maximum allowed mismatch

is -20 dB. This is used a goal throughout the remainder of this chapter. In comparison to the expected behaviour of a single CS transistor [150], no increase of output power dependency to load mismatch is observed.

3.7 Bandwidth of Stacked-FET

3.7.1 Bode-Fano limit

The bandwidth over which a complex impedance with quality factor Q can be matched to a real load with a finite error (represented by the matching level $|\Gamma|$) is obtained from the Bode-Fano limit [141,151]. For a first order load impedance, a general formulation of this limit is:

$$\frac{1}{\omega} \int_0^\infty \ln \left(\frac{1}{|\Gamma|} \right) d\omega \leq \frac{\pi}{Q}. \quad (3.43)$$

More insight is obtained if the required matching level is defined as $|\Gamma_{goal}|$ and the required operating band is between the low frequency limit ω_l and the high frequency limit ω_h . For a rectangular matching profile, with $|\Gamma| = |\Gamma_{goal}|$ for $\omega_l < \omega < \omega_h$ and $|\Gamma| = 0$ elsewhere and a load modelled by a parallel RC section with $Q = \Im Y_L / \Re Y_L = \omega C_L / G_L = \omega R_L C_L$, the relative bandwidth $BW = (\omega_h - \omega_l) / \sqrt{\omega_h \omega_l}$ is given by:

$$\frac{\omega_h - \omega_l}{\sqrt{\omega_h \omega_l}} = \frac{\pi}{Q \ln \left(\frac{1}{|\Gamma_{goal}|} \right)} = \frac{\Re Y_L \pi}{\Im Y_L \ln \left(\frac{1}{|\Gamma_{goal}|} \right)} = \frac{G_L \pi}{\omega C_L \ln \left(\frac{1}{|\Gamma_{goal}|} \right)}, \quad (3.44)$$

For in-band operating frequencies $\omega \approx \sqrt{\omega_h \omega_l}$, from which follows that:

$$\Delta\omega = \omega_h - \omega_l \approx \frac{G_L \pi}{C_L \ln \left(\frac{1}{|\Gamma_{goal}|} \right)}. \quad (3.45)$$

The effect of the number of transistors in a Stacked-FET on bandwidth is analysed for all three CBC options. With $Y_{L,CS} = G_{L,CS} + jB_{L,CS}$ substituted in Eqn. (3.40) to Eqn. (3.42), the optimum Stacked-FET load versus number of transistors in the Stacked-FET can be expressed (the real parts of the balancing components are ignored). In the case of CBCs to ground:

$$Y_{L,sX} = \frac{G_{L,CS} + jB_{L,CS}}{N} - Y_{pd,N}. \quad (3.46)$$

In the case of the CBCs as external drain-to-source capacitors:

$$Y_{L,dsX} = \frac{G_{L,CS} + j(B_{L,CS} - B_{dsX,N})}{N} - Y_{pd,N}, \quad (3.47)$$

with $B_{dsX,N}$ is the susceptance of the external drain-to-source capacitance of the upper FET in the Stacked-FET.

In the case of parallel CBCs to the drain of transistor N :

$$Y_{L,dNsX} = \frac{G_{L,CS} + j\left(B_{L,CS} - \sum_{n=1}^N n \cdot B_{dNsX,n}\right)}{N} - Y_{pd,N}, \quad (3.48)$$

with $B_{dNsX,n}$ is the susceptance of the capacitance between the source of FET n in the Stacked-FET and the drain of transistor N . In all cases both the real and imaginary part of the optimum load admittance decrease with the number FETs. An additional constant part exists due to presence of the parasitic drain capacitance of FET N . For the CBC as a shunt component to ground, the real part $G_{L,CS}$ and imaginary part $B_{L,CS}$ decrease evenly. When the CBC is implemented with an external drain-to-source admittance $B_{dsX,N}$ the presence of this admittance, which increases with stacking height, causes the real part to decrease more rapidly than the imaginary part. In the case of CBCs $B_{dNsX,n}$ to the drain of transistor N , this effect is even larger since the load admittance includes the balancing components for all DCG transistors.

For illustration, the real- and imaginary part of the optimum load of the Stacked-FET of $8 \times 350 \mu\text{m}$ transistors in WIN PP25-20 technology, designed at a frequency of 3 GHz, is given versus stacking height in Figure 3.19. According to Eqn. (3.46) to Eqn. (3.48), the real part of the load is equal for all three CBC options. The imaginary part, however, shows the dependency to the selected CBC option. The load for current balancing with a shunt component shows a decrease in imaginary part, although due to the presence of the parasitic drain capacitance it does not decrease as strong as the real part. The solutions with an external drain-to-source capacitance and with CBCs to the drain of transistor N both show an increase in imaginary part, where the latter shows the largest increase. For a Stacked-FET containing two FETs, these two options are equal.

Figure 3.19: Load admittance versus number of transistors in Stacked-FET. $C_{ds} = 850$ fF, $C_{gd} = 280$ fF, $C_{gs} = 2.5$ pF, $g_m = 0.3$ S and $f = 3$ GHz.

The resulting Q of the optimum load is shown in Figure 3.20. It is seen that for the CBC as a shunt component to ground, Q_{sX} is almost constant versus the number of transistor in the stack. For the other two options the, Q_{dsX} and Q_{dNsX} show an increase as the number of transistors in the stack gets larger.

Figure 3.20: Load admittance and Q versus number of transistors in Stacked-FET. $C_{ds} = 850$ fF, $C_{gd} = 280$ fF, $C_{gs} = 2.5$ pF, $g_m = 0.3$ S and $f = 3$ GHz.

The effect on obtainable absolute bandwidth is shown in Figure 3.21 for a required matching level of -20 dB. The bandwidth with shunt component remains larger than 1.8 GHz for a Stacked-FET with up to five transistors. For the other two options the bandwidth drops below 1 GHz if the Stacked-FET contains more than two transistors.

Figure 3.21: Bandwidth versus number of transistors in the Stacked-FET, $C_{ds} = 850$ fF, $C_{gd} = 280$ fF, $C_{gs} = 2.5$ pF, $g_m = 0.3$ S and $f = 3$ GHz, $|\Gamma_{goal}| = -20$ dB.

3.7.2 Bode-Fano limit in practise

Lopez [152] has solved the equations given by Fano [151] to determine the maximum obtainable bandwidth for a finite number of tuning elements k , where tuning elements are defined as succeeding series and parallel branches, including those of the complex load. In the case of a simple, yet often applied, matching network consisting of m LC-networks, the number of tuning elements equals $k = 2m + 1$. The relation between the number of LC-sections m and the maximum obtainable bandwidth is given by:

$$BW = \frac{1}{Q} \cdot \frac{1}{b_k \sinh \left[\frac{1}{a_k} \ln \left(\frac{1}{|\Gamma_{goal}|} \right) \right] + \frac{1-b_k}{a_k} \ln \left(\frac{1}{|\Gamma_{goal}|} \right)}, \quad (3.49)$$

where the coefficients a_k and b_k depend on the number of tuning elements k corresponding to the number of LC-sections m according to Table 3.4. The last entry, with $k = \infty$ corresponds to the Bode-Fano limit as given in Eqn. (3.45).

Table 3.4: Coefficients a_k and b_k versus the number of tuning elements k .

k	m	a_k	b_k
1	0	1	1
2	-	2	1
3	1	2.413	0.678
4	-	2.628	0.474
5	2	2.755	0.347
6	-	2.838	0.264
7	3	2.896	0.209
8	-	2.937	0.16
∞	∞	π	0

Figure 3.22: Bandwidth versus number of tuning elements for different CBC options, $N=3$, $C_{ds} = 850$ fF, $C_{gd} = 280$ fF, $C_{gs} = 2.5$ pF, $g_m = 0.3$ S and $f = 3$ GHz, $|\Gamma_{goal}| = -20$ dB.

The bandwidth of a Stacked-FET containing three transistors that can be obtained with a finite number of tuning elements is given in Figure 3.22 for the three CBC options. It is seen that with three LC matching sections, the maximum bandwidth with a shunt component is approximately 2.7 GHz. With an external drain-to-source capacitance this maximum bandwidth is approximately 1 GHz while for a CBC to the drain of transistor N , the bandwidth is below 0.7 GHz. Although from this analysis the CBC as a shunt component gives the largest possible bandwidth, it was already mentioned in section 3.6.2 that the implementation of this shunt component yields an intrinsic bandwidth limitation due to the required linearly decreasing, negative susceptance.

It is seen that although the Q-factor of the required load for a Stacked-FET is higher than for a conventional CS transistor, the achievable bandwidth with a practical number of matching elements is still large enough for application at S-band, where the typical absolute bandwidth is below 0.6 GHz.

3.7.3 Influence of matching ratio

In the previous sections it was shown that the real part of the optimum load admittance $Y_{L,stack}$ of a Stacked-FET consisting of N transistors is approximately N times smaller than that of the single transistor in CS configuration. To illustrate the effect of the smaller real part of the load admittance, the effect of the matching ratio on the obtainable bandwidth with a single LC-section is analysed. This analysis is based on the expression of input matching Γ_{in} as a function of matching ratio $r = \Re Y_{in} / \Re Y_{load}$ of the LC-section, angular frequency ω and angular centre frequency ω_c [150]:

$$\Gamma_{in}(\omega) = \frac{r - 1 - \left(\frac{\omega}{\omega_c}\right)^2 \cdot (r - 1)}{r + 1 - \left(\frac{\omega}{\omega_c}\right)^2 \cdot (r - 1) + 2j \cdot \frac{\omega}{\omega_c} \cdot \sqrt{r - 1}}. \quad (3.50)$$

Based on Eqn. 3.50 the obtainable relative bandwidth is plotted for a target matching of -20 dB in Figure 3.23. The figure shows the strong dependency of bandwidth on the matching ratio. The use of a Stacked-FET containing two transistors, which reduces the matching ratio with a factor two, can increase the bandwidth with approximately 100 %. If a Stacked-FET with three transistors is used, the matching ratio reduces with of a factor of three, resulting in an increase of bandwidth with almost 200 %.

Figure 3.23: Relative bandwidth versus matching ratio, $|\Gamma_{goal}| = -20$ dB.

3.8 Demonstration

The procedure of Stacked-FET balancing is verified through the design and test of a range of Stacked-FETs containing two, three and four $8 \times 350 \mu\text{m}$ transistors. In this section the selection of the CBC option and the biasing consideration are described, followed by the results from the designed Stacked-FETs.

3.8.1 Selection of current equalisation option

In section 3.6 the three implementations of the CBC were worked out. It was shown that the shunt admittance implementation requires a negative admittance which decreases linearly over frequency. This can only be implemented over a very small frequency range with an inductor and results in a direct bandwidth limitation. Besides, such an inductor causes a DC connection between the sources of the DCG transistors and ground which means that proper decoupling is necessary. The combination of this inductor and the decoupling requires a large chip area. The CBC option with component to the drain of transistor N requires the load with the largest reactance, with corresponding bandwidth limitation, and besides it introduces multiple RF loops with increases the stability risks while it does not offer significant advantages. For these reasons, from the three presented implementation of the CBC, the option with external drain-to-source capacitors is selected.

3.8.2 Gate biasing of the Stacked-FET

The transistors in the Stacked-FET should be biased according to the selected class of operation. In this case class-B is selected, meaning that the quiescent drain current should be zero and the transistors should be gate-biased at the their pinch-off voltage. To balance all the transistors in the Stacked-FET the individual gate-to-source voltages of each transistor in the Stacked-FET should be equal. This is achieved for every FET n in the stack by defining the gate bias voltage $V_{g,n}$ as:

$$V_{g,n} = (n - 1)V_{ds} + V_{gs} = \frac{n - 1}{N}V_{dd} + V_{gs}. \quad (3.51)$$

The Stacked-FETs discussed in this thesis are designed for pulsed radar applications, meaning that these devices are switched on and off at high pulse rates. During the switching of the bias voltages of the Stacked-FET, care must be taken to simultaneously provide the overall drain voltage as well as the gate voltages of the individual DCG FETs. Switching the DCG gate voltages earlier than drain supply could result in high temporal gate-to-source and gate-to-drain voltages which can damage the transistors in the Stacked-FET. Switching the DCG gate voltages later than the drain supply stresses the gate-to-drain diode

in reverse resulting in breakdown effects, either instantly or in the form of degradation over time. The gate voltages for the DCG FETs are derived from the overall drain voltage, which ensures simultaneous switching if the differences in rise and fall time of the different biasing paths are minimal.

Gate voltage variations

The gate-to-source voltages $V_{gs,n}$ of the transistors in the Stacked-FET depend on the applied gate bias voltages and the source voltages of these transistors. The source voltage of the CS FET is zero which means that for this transistor the gate-to-source voltage equals the externally applied gate voltage. This voltage sets the quiescent current of the CS transistor which will then dictate the current in the entire Stacked-FET. Under small-signal conditions the source voltages of the DCG FETs will be such that the $V_{gs,n}$ values correspond to this DC drain current; these source voltages will depend only on the CS transistor current and the total drain supply voltage of the Stacked-FET.

When the Stacked-FET is driven into compression, the voltage and current swings on the transistors increase and reach the DC limits of the transistor, such as the knee voltage and the maximum current. Since the Stacked-FET is optimised for operation in the non-linear regime, the FETs in the Stacked-FET are not properly balanced under small-signal conditions and the voltage- and current swings of the FETs are not equal. As a consequence not all FETs reach the DC limits simultaneously, which influences the compression behaviour of the Stacked-FET.

If the dynamic load line of the CS FET reaches the $I_{ds} = 0$ limit, even mode harmonics are generated and the DC component of the current signal increases. If the load line of the DCG FETs is such that the $I_{ds} = 0$ limit is not yet reached, this hard clipping does not occur and the increased drain current results in an increase of the gate-to-source voltage of this DCG FET. As the gate voltage is externally supplied and hence constant, the source voltage will decrease. If the DCG FET reaches the $I_{ds} = 0$ limit before the CS transistor reaches this limit, the source voltage will increase.

Via this mechanism the source voltages and hence the drain-to-source voltages of the DCG FET will vary if the Stacked-FET is driven into compression. Furthermore any error in the applied gate voltage to FET n results in a source voltage error of similar magnitude and thus an error in the drain voltage of FET $n - 1$. Since the absolute values of the drain-to-source voltages are much larger than the absolute values of the gate-to-source voltages, performance of the Stacked-FET shows a low sensitivity to variation in gate voltages of the DCG FETs. To illustrate this for the WIN PP25-20 technology: A gate-to-source voltage variation of 10 % corresponds to approximately 0.15 V, which is less than 2 % of the drain-to source voltage of the FET.

Figure 3.24: Supply of gate bias voltages.

The gate bias voltage of the CS FET can be applied via the Input Matching Network (IMN) network connected to the gate of the transistor, as illustrated in Figure 3.24. With a proper decoupling the DC connection can be placed outside of the RF plane which means that the biasing will not influence the RF performance. The gates of the DCG FETs are only connected to the external gate capacitance C_{gX} (optionally via the series stability resistor R_{gX} which will be described in chapter 5). The gate bias voltage has to be supplied to these gates without disturbing the RF loading. A first possibility is to use quarter-lambda or high inductance lines, however the length of these lines makes this option impractical. The option adopted in this work is to use series resistors, as shown in Figure 3.24. From an RF point of view, if the gate supply lines are properly decoupled, these resistors are connected in parallel to the external gate admittance $Y_{gX,n}$. From Figure 3.13 it is seen that the minimum absolute value of this admittance at S-band is approximately 8 mS, corresponding to an absolute impedance value of 125 Ω . For proper decoupling the gate bias resistor should be much larger than this value. On the other hand, if the resistor value is too large, the rise time of the gate voltage on the transistor due to this resistor in combination with the gate capacitance will be too high, resulting in distorted start-up-behaviour. A maximum rise time of 100 ns is assumed. In combination with a total gate capacitance of approximately 10 pF this yields a maximum resistor value of 3333 Ω .

3.8.3 Layout

The layouts of the designed structures are given in Figure 3.25 to Figure 3.27. From these layouts it can be seen that DCG transistors are not connected to the original reference plane of the transistors. For this reason an alternative transistor modelling technique is used. Details on this modelling technique are given in chapter 4. All structures have a parallel RC-section in series with the gate of the CS FET and a resistance in series with the external gate capacitance to enhance the stability. A thorough stability analysis will be given in chapter 5. Besides the RF input and output, DC connections are present for the biasing of the DCG transistors. The Stacked-FET with three transistors has active gate bias circuits to derive these gate bias voltages from the positive supply. These bias circuits are based on the standard CS FET bias circuits as described in [153].

Figure 3.25: Stacked-FET of $2 \times 8 \times 350 \mu\text{m}$.

Figure 3.26: Stacked-FET of $3 \times 8 \times 350 \mu\text{m}$ including active gate-bias network.

Figure 3.27: Stacked-FET of $4 \times 8 \times 350 \mu\text{m}$.

3.8.4 Results

The measurement results from the Stacked-FET structures are given in Figure 3.28 to 3.30 together with the results from a single CS FET. The figures show the measured data from 6 stacks of two FETs ($2 \times 8 \times 350 \mu\text{m}$), 6 stacks of three FETs ($3 \times 8 \times 350 \mu\text{m}$), 4 stacks of four FETs ($4 \times 8 \times 350 \mu\text{m}$) and 1 single CS FETs ($3 \times 8 \times 350 \mu\text{m}$). In Figure 3.28 it is seen that the output power increases with the number of FETs in the stack, not only in the compression or saturation regime but also in the small signal range. This implies that, as expected, besides the output power, also the gain increases with the number of FETs in the stack.

Figure 3.28: Output power of (Stacked-)FET, $f=3$ GHz, $V_{ds}=8$ V, $V_{gs}=-1$ V, $T_a=25$ °C.

Figure 3.29 shows the output power densities for all three structures. The output power density of the Stacked-FETs saturates earlier than the output power density of the single transistor and decreases with the number of FETs in the stack. This is the penalty for stabilisation of the stack, which will be treated in more detail in chapter 5.

Figure 3.29: Output power density of (Stacked-)FETs, $f=3$ GHz, $V_{ds}=8$ V, $V_{gs}=-1$ V, $T_a=25$ °C.

In Figure 3.30 the PAE for all three structures is shown. The PAE reduction of the Stacked-FET structures is in line with the measured reduction in output power density.

Figure 3.30: PAE of (Stacked-)FET, $f=3$ GHz, $V_{ds}=8$ V, $V_{gs}=-1$ V, $T_a=25$ °C.

3.9 Load mapping of DCG transistors

The calculated values for the balancing components C_{gX} and C_{dsX} of the DCG transistors only result in proper load translation in combination with the unique load admittance for which the values were determined. The load admittance out of the operation band will be different, therefore load equalisation is not obtained within these frequency ranges. This complicates harmonic tuning of transistors in the Stacked-FET and complicates the stabilisation of the DCG transistors.

3.9.1 Out-of-band termination

To analyse of the effects of out-of-band terminations of a Stacked-FET the load-to-source mapping of a DCG transistor is investigated. This is carried out based on the simplified small-signal model that was shown in Figure 3.5.

For the gate node (g) holds:

$$v_g = \frac{v_s Y_{gs} + v_d Y_{gd}}{Y_{gX} + Y_{gs} + Y_{gd}} = \frac{v_s Y_{gs} + v_d Y_{gd}}{Y_f}, \quad (3.52)$$

where $Y_f = Y_{gX} + Y_{gs} + Y_{gd}$. For the drain node (d) holds:

$$v_d = \frac{v_g Y_{gd} - g_m v_g + g_m v_s + v_s Y_{ds}}{Y_{gd} + Y_{ds} + Y_L} = \frac{v_g Y_{gd} - g_m v_g + g_m v_s + v_s Y_{ds}}{Y_h}, \quad (3.53)$$

where $Y_h = Y_{gd} + Y_{ds} + Y_L$.

Substitution of Eqn. (3.52) into Eqn. (3.53) gives:

$$\frac{v_d}{v_s} = \frac{Y_{gs} Y_{gd} - g_m Y_{gs} + Y_f g_m + Y_f Y_{ds}}{Y_f Y_h - Y_{gd}^2 - g_m Y_{gd}}. \quad (3.54)$$

The input admittance Y_{in} is given by:

$$Y_{in} = \frac{i_{in}}{v_s} = \frac{(v_g - v_s) Y_{gs} + g_m (v_g - v_s) + (v_d - v_s) Y_{ds}}{-v_s}. \quad (3.55)$$

Substitution of Eqn. (3.52) into Eqn. (3.55) gives:

$$-Y_{in} = \left(\frac{Y_{gs} + \frac{v_d}{v_s} Y_{gd}}{Y_f} - 1 \right) \cdot (Y_{gs} + g_m) + \left(\frac{v_d}{v_s} - 1 \right) Y_{ds}. \quad (3.56)$$

Substitution of Eqn. (3.54) into Eqn. (3.56) results in:

$$Y_{in} = \frac{A + B + C}{Y_f Y_h + g_m Y_{gd} - Y_{gd}^2}, \quad (3.57)$$

where:

$$A = g_m (-Y_{gs} Y_{gd} - Y_{gs} Y_L + Y_{gd} Y_f + Y_L Y_f - Y_{gd}^2),$$

$$B = -Y_{gs}^2 Y_h - 2Y_{gs} Y_{ds} Y_{gd} - Y_{gd}^2 Y_{gs} - Y_{ds} Y_{gd}^2$$

and

$$C = Y_f (Y_{gs} Y_h + Y_{gd} Y_{ds} + Y_L Y_{ds}).$$

Using Eqn. 3.57 it is now possible to determine the DCG input admittance as function its load admittance. This load mapping gives insight into the internal stability of Stacked-FET, as will be discussed in detail in chapter 5. Furthermore, the mapping of the loads at the harmonic frequencies can be analysed, which is the subject of the next section.

3.9.2 Effect on harmonic load

Due the impact on voltage and current waveforms, the applied transistor loads at the harmonics frequencies can have a major impact on RF performance as well as reliability [154]. In order to stress all the transistors in the Stacked-FET in a similar manner, the harmonic load applied to drain of each transistor in the Stacked-FET should be equal. For the DCG FET this means that the harmonic load reflection coefficient should be found which is mapped to the same reflection coefficient at the input, i.e. the load for which the DCG is transparent. The analysis of the harmonic loads is limited to the second harmonic load $\Gamma_L^{2f_0}$ and the third harmonic load $\Gamma_L^{3f_0}$ as these are the only two components that have significant impact on the transistor performance. At higher frequencies the parasitic output capacitance of the transistor dominates the loading of the intrinsic transistor. The second harmonic load $\Gamma_L^{2f_0}$ causes even-mode distortion of the waveforms resulting in asymmetry between the positive and negative peaks of the waveforms. The third harmonic load $\Gamma_L^{3f_0}$ causes odd-mode distortion of the waveforms which has the same effect on both the positive and negative peaks of the waveforms.

The mapping of the second harmonic load to the DCG input according to Eqn. (3.57) is illustrated in Figure 3.31 based on the characteristics of a $8 \times 350 \mu\text{m}$ transistor. The DCG transistor is designed at a frequency of 3 GHz and the mapping is given for the $2f_0$ frequency of 6 GHz. The load reflection coefficients indicated on the right side yield the input reflection coefficient given on the left. It can be seen that the Smith chart region, i.e. load reflection coefficients with a maximum magnitude of 1, can translate to input reflection coefficients with a magnitude much larger than 1, which means that a passive termination may result in an input impedance with a real part much smaller than zero. The same effect is observed for other (non harmonically related) frequencies.

Figure 3.31: Mapping of second harmonic load (right) to input (left) for DCG $8 \times 350 \mu\text{m}$ FET, with $g_m=0.8 \text{ S}$, $C_{gs}=5 \text{ pF}$, $C_{gd}=200 \text{ fF}$, $C_{ds}=800 \text{ fF}$, $C_{gx}=0.8 \text{ pF}$, $C_{dsx}=1.2 \text{ pF}$, $2f_0=6 \text{ GHz}$.

To find which load is transparent from the DCG output to the input, (3.57) is solved for $Y_{in} = Y_{load}$. This yields:

$$Y_L = \frac{-B_1 \pm \sqrt{B_1^2 - 4Y_f C_1}}{2Y_f} \quad (3.58)$$

with

$$B_1 = Y_f Y_{gd} + g_m Y_{gd} - Y_{gd}^2 + g_m Y_{gs} - g_m Y_f + Y_{gs}^2 - Y_f Y_{gs}$$

and

$$C_1 = g_m Y_{gs} Y_{gd} - g_m Y_{gd} Y_f + g_m Y_{gd}^2 + Y_{gs}^2 Y_{gd} + Y_{gs}^2 Y_{dsT} + 2Y_{gs} Y_{dsT} Y_{gd} \\ + Y_{gd}^2 Y_{gs} + Y_{dsT} Y_{gd}^2 - Y_f Y_{gd} Y_{gs} - Y_f Y_{gs} Y_{dsT} - Y_f Y_{gd} Y_{dsT}.$$

The two solutions of Eqn. (3.58) are plotted in Figure 3.32 versus frequency. The loads at the harmonic frequencies of 6 GHz and 9 GHz are indicated in the figure. The properties of the solutions are investigated in more detail.

Figure 3.32: Transparent loads from drain to source of DCG FET with $g_m=0.8$, $C_{gs}=5$ pF, $C_{gd}=200$ fF, $C_{ds}=800$ fF, $C_{gX}=0.8$ pF, $C_{dsX}=1.2$ pF.

A vector field indicating the strength and direction of the translation from load to input reflection coefficient of the DCG transistor as described by $f(\Gamma_L) = \Gamma_L(\Gamma_{in}) - \Gamma_{in}$ is shown in Figure 3.33 for all possible second harmonic load reflection coefficients. Figure 3.36a gives the results for load reflections with a magnitude smaller than unity and Figure 3.36b gives the results for load reflections with a magnitude larger than unity.

The two solutions found from Eqn. (3.58) at a frequency of 6 GHz, which were indicated in Figure 3.32, can be identified as the point with a vector magnitude of zero, i.e. the poles of the function. This implies that a load reflection coefficient with one of these two values will result in an equal input reflection coefficient. For a Stacked-FET containing this DCG transistor this means that the load reflection coefficient at the drain of the preceding transistor is equal to the load reflection coefficient at the drain of this stage. It is however seen that one of the poles in Figure 3.33 is a sink, while the other is a source. Although both poles are theoretically transparent points, any perturbation around the source will result in a shift away from that source. Effectively after multiple transistors, all the reflection coefficients will be attracted toward the sink. This is illustrated in Figure 3.34 which shows the translation of reflection coefficients through a cascade of DCG transistors. The loads for $n=0$ at the output of the DCG transistor is defined to cover the entire Smith chart region. At $n=1$, after a single DCG stage these loads are spread out over a reflection coefficient region including areas

where $|\Gamma| \gg 1$. The same holds after two DCG stages ($n=2$), although the region in that case is more compact. Here it is already seen that the loads concentrate around the location of the sink in Figure 3.33. After five transistors all the loads remain within the Smith Chart region and for a larger number of stage all loads are mapped to a very compact region close to the sink. It is found that the only reflection coefficient that remains constant after each successive DCG stage is the load at the sink.

Figure 3.33: Vector field indicating load translation $f(\Gamma_L) = \Gamma_L(\Gamma_{in}) - \Gamma_{in}$ from load to input of DCG FET with $g_m=0.8$ S, $C_{gs}=5$ pF, $C_{gd}=200$ fF, $C_{ds}=800$ fF, $C_{gx}=0.8$ pF, $C_{dsx}=1.2$ pF, $f=6$ GHz. (a): Standard Smith chart for reflection coefficients with magnitude smaller than 1, (b): Negative Smith chart for reflection coefficients with magnitude larger than 1.

Figure 3.34: Load mapping through DCG FET cascade with $g_m=0.8$, $C_{gs}=5$ pF, $C_{gd}=200$ fF, $C_{ds}=800$ fF, $C_{gx}=0.8$ pF, $C_{dsx}=1.2$ pF, $f=6$ GHz.

The mapping of four specific load reflection coefficients ($1, j, -1$ and $-j$) to the DCG input is illustrated in Figure 3.35 as a function of frequency. The diamonds indicate the lowest frequency of 0.1 GHz and the squares indicate the highest frequency of 30 GHz. It is seen that at the highest frequency all four load reflection coefficients are mapped close to a short at the input. The mapping of the open circuit spreads out over the entire bottom edge of the Smith Chart, while the mapping of $+j$ point shows a large loop outside the Smith Chart region. The mapping of the short and the $-j$ point are more located within a concentrated region.

Figure 3.35: Mapping of load to input for DCG FET with $g_m=0.8$, $C_{gs}=5$ pF, $C_{gd}=200$ fF, $C_{ds}=800$ fF, $C_{gX}=0.8$ pF, $C_{dsX}=1.2$ pF, $f=0.1$ to 30 GHz.

The vector field of the translation from load to input reflection coefficient at the $3f_0$ frequency of 9 GHz is given in Figure 3.36. Also here the points that were indicated in Figure 3.32 are recognised as the poles. All conclusions drawn for the second harmonic load are also valid for this third harmonic load.

Figure 3.36: Vector field indicating load translation $f(\Gamma_L) = \Gamma_L(\Gamma_{in}) - \Gamma_{in}$ from load to input of DCG FET with $g_m=0.8$, $C_{gs}=5$ pF, $C_{gd}=200$ fF, $C_{ds}=800$ fF, $C_{gX}=0.8$ pF, $C_{dsX}=1.2$ pF, $f=9$ GHz. (a): Standard Smith chart for reflection coefficients with magnitude smaller than 1, (b): Negative Smith chart for reflection coefficients with magnitude larger than 1.

3.10 Conclusion

In this chapter equations are derived for the balancing of the DCG transistors in a Stacked-FET. The optimum loading of the intrinsic part of the (CS) FET is used as a starting point of the design. Based on the large signal equivalent parameter values of the DCG FET, the optimum values for the balancing components are determined. For the voltage balance this component is an external gate capacitor, for current balance three options are analysed and an external drain-to-source capacitance is preferred.

The total procedure to design and dimension the Stacked-FET, taking the parasitic capacitances into account, is:

- Select optimum external transistor load based on knowledge from CS FET.
- Find extrinsic and intrinsic transistor model parameters.
- Translate optimum external transistor load to loading of intrinsic transistor.
- Select implementation for CBC.
- Calculate values for voltage balancing and CBC, starting at the lower DCG transistor.
- Repeat this for each DCG transistor in the Stacked-FET, working to the uppermost DCG transistor.
- Determine optimum load admittance of complete Stacked-FET.

This flow is illustrated in the flow chart in Figure 3.37.

For the CBC option with a shunt component the bandwidth limit arises from the implementation of this negative susceptance with an inductor. For the other two options the bandwidth is Fano limited. The addition of an external drain-to-source component is the preferred implementation for the CBC since this has the smallest impact on bandwidth, is better implementable from a layout point of view without any decoupling requirements and does not introduce additional RF loops that might degrade the overall amplifier stability.

During the design of the last DCG transistor the optimum loading for the entire Stacked-FET is obtained. Two methods were discussed to determine the large signal equivalent components parameter values. It is shown that the options for optimisation of harmonic terminations are limited due to the output-to-input mapping of the DCG transistors. As the DCG transistor is only (close to) transparent for a short, this is the obvious choice for the harmonic loads. From Table 2.1 it can be seen the only current-mode classes for which these harmonic loads are valid, are the classes A, B and C. A numerical example of the dimension of Stacked-FET is given for illustration and the effect of transistor stacking on maximum obtainable bandwidth is discussed.

Figure 3.37: Flow chart for Stacked-FET balancing.

CHAPTER 4

Custom-Transistor Modelling

4.1 Introduction

During the design of any amplifier, high quality transistor models are required to perform reliable simulations. The accuracy of such a model is maximal if it is based on measurements on that same type of transistor. Scaling rules can be identified in order to fit the model parameters over a range of transistor geometries, but the use of any dimension outside of this range, or any other type of modification that is not explicitly addressed in the model equations, reduces the accuracy of the model. Once a modified transistor structure is available for testing, a dedicated model can be generated based on measured results on this structure. As this is often not the case from the beginning of the design process, an alternative model needs to be generated that represents the behaviour of the structure as accurately as possible.

In the previous chapter several examples of Stacked-FETs were given. The layouts of these Stacked-FETs were shown in Figure 3.25 to Figure 3.27. A detailed view of one of the DCG stages from the Stacked-FET containing four transistors is shown in Figure 4.1. From this layout it can be seen that the gate, source and drain reference planes are distinctly different from those of a common CS transistor, as was illustrated in Figure 2.15 in section 2.4 and on which the compact transistor model is based. This implies that modifications to this transistor model are required or a completely new model needs to be created.

Figure 4.1: DCG stage from Stacked-FET with four transistors.

In this chapter a transistor model is developed which is divided into a compact model part for each single intrinsic gate finger and a part describing the extrinsic passive structure that connects these intrinsic gate fingers. The model extraction is based on the measured two-port parameters of a small, two finger transistor. The choice of the transistor will be discussed later in the chapter. The extrinsic parasitics of this transistor are obtained through simulation, using an EM solver. The result of this simulation is used to de-embed the intrinsic gate finger parameters from the transistor measurements. Once the model of the intrinsic gate finger is available, alternative geometries can be defined of which the modified extrinsic part is again analysed in the EM solver. The new EM results are combined with the intrinsic gate model(s) to represent the modified alternative transistor geometries. This method yields several advantages:

- A high level of flexibility with respect the transistor layout and reference planes is obtained. Any modifications in the extrinsic transistor part are accounted for in the EM-analysis.
- The phase relations between the individual gate fingers and the phase relations within a single finger are taken into account. This extends the scaling range for this model when compared to a compact model of the complete transistor, which are usually verified over a given range of transistor sizes. Extrapolation outside of this range is usually limited to several tens of percents, whilst the technique described here has been demonstrated with a scaling factor of 30 [155].
- Additional layers can be included in the layer stack of the EM simulation, for example to include the effect of protective layers that cover the MMIC.

Any mistake in the parameter extraction will be amplified and visible at the end results. For this reason, particularly the care with which the parameters of the extrinsic transistor part is determined, is essential to the success of the approach. Correct calibration of the internal ports in the EM simulation is crucial.

4.2 Modelling methodology

This section describes the method to determine the parameter values of the model that describes the individual intrinsic gate finger. The adopted method is based on the work published by Mahon *et al.* [156,157]. The Y-parameters of the single intrinsic gate finger, Y_{SGF} , can be extracted from the measurement results of a two-finger transistor. Due to the symmetry of such a two-finger transistor, the system of equations that describe the extrinsic parasitics can be simplified such that this system can be solved; in this way, Y_{SGF} will be obtained later in this section.

Figure 4.2: Separation of intrinsic gate fingers and extrinsic parasitics of two-finger transistor. Note the symmetry about the horizontal axis; this symmetry reflects the symmetry in the transistor layout.

The topology of the model of the two-finger transistor is given in Figure 4.2. The external ports ① and ② are referring to ground while the internal ports ③, ④, ⑤ and ⑥ use the internal gate connections as a reference. The extrinsic parasitic part is mathematically removed from the measurement data using the results of an EM simulation.

The setup of the EM simulation on the extrinsic part is given in Figure 4.3. The port numbering corresponds to the definitions in Figure 4.2.

Figure 4.3: Port definitions of EM simulation.

The entire model containing the two intrinsic gate fingers and the extrinsic parasitic parts can be described in terms of the Y-matrix $\mathbf{Y}^{\text{EM}}$ of the six-port EM result in combination with the voltages and currents on the ports:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \end{bmatrix} = [\mathbf{Y}^{\text{EM}}] \cdot \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \end{bmatrix}. \quad (4.1)$$

Due to the symmetry about the horizontal axis of the two-finger device, the internal currents $i_5 = i_3$ and $i_6 = i_4$ while the internal voltages $v_5 = v_3$ and $v_6 = v_4$. Furthermore:

$$Y_{15}^{EM} = Y_{13}^{EM},$$

$$Y_{16}^{EM} = Y_{14}^{EM},$$

$$Y_{25}^{EM} = Y_{23}^{EM}$$

and

$$Y_{26}^{EM} = Y_{24}^{EM}.$$

Applying these equalities to Eqn. (4.1) yields:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & y_{13} & y_{14} & y_{13} & y_{14} \\ y_{21} & y_{22} & y_{23} & y_{24} & y_{23} & y_{24} \\ y_{31} & y_{32} & y_{33} & y_{34} & y_{35} & y_{36} \\ y_{41} & y_{42} & y_{43} & y_{44} & y_{45} & y_{46} \\ y_{31} & y_{32} & y_{33} & y_{34} & y_{35} & y_{36} \\ y_{41} & y_{42} & y_{43} & y_{44} & y_{45} & y_{46} \end{bmatrix} \cdot \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_3 \\ v_4 \end{bmatrix}. \quad (4.2)$$

Factorisation of Eqn. (4.2) and removing redundancy yields:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & 2y_{13} & 2y_{14} \\ y_{21} & y_{22} & 2y_{23} & 2y_{24} \\ y_{31} & y_{32} & y_{33} + y_{35} & y_{34} + y_{36} \\ y_{41} & y_{42} & y_{43} + y_{45} & y_{44} + y_{46} \end{bmatrix} \cdot \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix}, \quad (4.3)$$

The external and internal current and voltage vectors are defined as:

$$\mathbf{I}_e = \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}, \quad (4.4)$$

$$\mathbf{I}_i = \begin{bmatrix} i_3 \\ i_4 \end{bmatrix}, \quad (4.5)$$

$$\mathbf{V}_e = \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (4.6)$$

and:

$$\mathbf{V}_i = \begin{bmatrix} v_3 \\ v_4 \end{bmatrix}, \quad (4.7)$$

with which Eqn. (4.3) can be written as:

$$\begin{bmatrix} \mathbf{I}_e \\ \mathbf{I}_i \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_{ee} & \mathbf{Y}_{ei} \\ \mathbf{Y}_{ie} & \mathbf{Y}_{ii} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{V}_e \\ \mathbf{V}_i \end{bmatrix}, \quad (4.8)$$

with

$$\mathbf{Y}_{ee} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}, \quad (4.9)$$

$$\mathbf{Y}_{ei} = 2 \begin{bmatrix} y_{13} & y_{14} \\ y_{23} & y_{24} \end{bmatrix}, \quad (4.10)$$

$$\mathbf{Y}_{ie} = \begin{bmatrix} y_{31} & y_{32} \\ y_{41} & y_{42} \end{bmatrix} \quad (4.11)$$

and:

$$\mathbf{Y}_{ii} = \begin{bmatrix} y_{33} + y_{35} & y_{34} + y_{36} \\ y_{43} + y_{45} & y_{44} + y_{46} \end{bmatrix}. \quad (4.12)$$

The external currents and voltages are related to the Y-matrix $\mathbf{Y}_{\text{meas}}$ that is obtained from the measurement of the transistor according to:

$$\mathbf{I}_e = \mathbf{Y}_{\text{meas}} \cdot \mathbf{V}_e \quad (4.13)$$

The Y-matrix $\mathbf{Y}_{\text{SGF}}$ of a single gate finger is related to the internal currents and voltages at the interface between the intrinsic and extrinsic parts according to:

$$-\mathbf{I}_i = \mathbf{Y}_{\text{SGF}} \cdot \mathbf{V}_i \quad (4.14)$$

By combining Eqn. (4.8), Eqn. (4.13) and Eqn. (4.14), $\mathbf{Y}_{\text{SGF}}$ can be solved:

$$\mathbf{Y}_{\text{SGF}} = -\mathbf{Y}_{ie} (\mathbf{Y}_{\text{meas}} - \mathbf{Y}_{ee})^{-1} \mathbf{Y}_{ei} - \mathbf{Y}_{ii}. \quad (4.15)$$

The reactances of the extrinsic transistor part, i.e. the inductances and capacitances, mainly depend on the geometry of the metal and the thickness of the semiconductor substrate. These parameters are well known from the transistor layout and the process description. The access resistance values R_d and R_s are determined by the transistor geometry in combination with the thickness and resistivity of the active transistor region close to the intrinsic finger and the contact resistance between the metal and the active transistor part while the value of R_g depends on the resistivity and the exact shape of the gate metal. These aspects are usually not known to the designer, for this reason the access resistances are not included in the EM analysis. Instead an additional layer in between the intrinsic parts and the extrinsic metal is introduced [158, 159] which contains the access resistances, the values of which are extracted from the measurement data at the cold-FET bias point [110] after subtraction of the EM results.

For the extraction of the access resistances, the method defined in [160] is adopted. After the removal of the reactances, the access resistance values can be obtained from the measurements at the cold-FET bias point according to [160]:

$$R_s = \frac{d \left(\omega \frac{\Re Z_{1,2}}{\Im Z_{2,2}} \right)}{d \left(\omega \frac{1}{\Im Z_{2,2}} \right)}, \quad (4.16)$$

$$R_g + R_s = \frac{d \left(\omega \frac{\Im Z_{1,2}}{\Im Z_{2,2}} \right)}{d \left(\omega \frac{1}{\Im Z_{2,2}} \right)}, \quad (4.17)$$

and

$$R_d + R_s = \frac{d \left(\omega \frac{\Re Z_{2,2}}{\Im Z_{2,2}} \right)}{d \left(\omega \frac{1}{\Im Z_{2,2}} \right)}. \quad (4.18)$$

The entire model consisting of the EM part, the access resistances and intrinsic gate model is illustrated in Figure 4.4.

Figure 4.4: FET model construction.

4.3 Gate-Finger Model Extraction

The intrinsic gate finger model is extracted from the measurements and simulation of a $2 \times 67 \mu\text{m}$ transistors. The S-parameters of this transistor are measured at a nominal bias point and the cold-FET bias point of $V_{ds}=V_{gs}=0 \text{ V}$.

4.3.1 Simulation of extrinsic reactances

The reactive part of the extrinsic parasitics are simulated in an EM solver. The setup for the EM analysis on the $2 \times 67 \mu\text{m}$ FET is shown in Figure 4.5. As the access resistances are determined separately, all the metal layers are defined as lossless. The gate metal is mapped to a layer directly above the substrate. At the connection points for the intrinsic gate finger model the gate metal is cut and four ports are defined at the two gate connections, the drain connection and

the source connection [161, 162]. For the two-finger device this yields a ten-port EM simulation. The distances between the ports that connect to a single gate finger are small, which means that parasitic coupling effects might be present in the simulation results. To obviate these artefacts, Sonnet [124] has been used as an EM solver, since this offers the possibility to create co-calibrated port groups [163]. All four internal ports of a single gate finger connection are defined as part of a calibration group which means that they share a common, local ground and are calibrated simultaneously to remove all cross-coupling between these ports. The meshing in the y-direction should be fine enough to correctly model the width of the gate metal as well as the distances between the gate metal and the drain and source regions. In this case the mesh grid in this direction is chosen equal to the gate length of $0.25 \mu\text{m}$. In the x-direction a coarser mesh is allowed.

After the simulation the resulting ten-port matrix is converted to the required six-port matrix with the internal gate connections as reference nodes for the internal drain and source connections. Internal gate ports ④ and ⑥ are mathematically connected and ports ③ and ⑤ are defined with this joint port ④ and port ⑥ node as ground reference. The same is done for the equivalent port at the second finger. This yields the required configuration as was defined in Figure 4.3.

Figure 4.5: Sonnet setup $2 \times 67 \mu\text{m}$ transistor.

A 3D view of the EM-simulation setup is shown in Figure 4.6.

Figure 4.6: 3D view of Sonnet setup for 2x67 μm transistor simulation.

4.3.2 Access resistances

The result of the extraction of the access resistances from two different devices are given in Figure 4.7. The variation between the results from the different samples is small. It is assumed that the resistances R_d and R_s are inversely proportional to the gate width while the resistance R_g is assumed to scale linearly with the gate width. The normalised component values are listed in Table 4.1.

Figure 4.7: Extracted access resistance values of single 67 μm gate finger.

Table 4.1: Normalised access resistance values for single 67 μm gate finger.

Parameter	Unit	Value
R_g	Ω/mm	328.4
R_d	$\Omega\cdot\text{mm}$	0.71
R_s	$\Omega\cdot\text{mm}$	0.61

4.3.3 Intrinsic parameters extraction

Figure 4.8 shows the small-signal model used to describe the intrinsic gate finger [109]. After subtraction of the EM results and the access resistances, the intrinsic model parameters of a single gate finger are extracted from the remaining two port data [108].

Figure 4.8: Intrinsic FET model.

The model parameter values extracted from the two devices are given in Figure 4.9. The parameters τ , R_{id} and R_{is} show difficulties in extraction at low frequencies. For this reason all parameter values are extracted using the average values between 4 GHz and 6 GHz. The obtained values for R_{id} and R_{is} are small or negative, therefore these parameters are set to zero. An overview of used values is given in Table 4.2.

4.3. GATE-FINGER MODEL EXTRACTION

Figure 4.9: Small signal model parameters extracted from two 2x67 μm devices.

Table 4.2: Small signal model parameter values of intrinsic gate finger.

Parameter	Unit	Value
C_{gd}	fF/mm	20.4
C_{gs}	pF/mm	1.53
C_{ds}	fF/mm	147
G_{ds}	mS/mm	9.9
g_m	mS/mm	279
τ	ps	2.77
R_{id}	$\Omega \cdot \text{mm}$	0
R_{is}	$\Omega \cdot \text{mm}$	0

4.4 Custom-transistor model construction

The overall transistor model is constructed by embedding the intrinsic gate finger model and the access resistances into the EM simulation result. A comparison between the S-parameters simulated with the constructed model and the measured S-parameters of the two $2 \times 67 \mu\text{m}$ transistors are shown in Figure 4.10. An excellent match is observed over the entire frequency band from 1 GHz to 15 GHz.

The EM-based model is used to simulate the Stacked-FET containing the $3 \times 8 \times 350 \mu\text{m}$ transistors. A Sonnet simulation is performed on the metal parts including the balancing components of this Stacked-FET, where each gate finger is divided in t parts with a unit-cell gate finger width of $350/t \mu\text{m}$ each. The access resistances and the intrinsic model are linearly scaled to this unit-cell width. The simulated S-parameters at the S-band frequency of 3 GHz and the $3f_0$ frequency of 9 GHz are shown in 4.11. From these results it can be found that at both frequencies the S-parameters show slight variations versus the number of sections per gate finger and, as expected, the variation is larger at the highest frequency. For t larger than 4, the variation becomes very small which means that the number of sections per gate finger should be higher than four.

Figure 4.10: Simulated and measured S-parameters of 2x67 μm transistor.

Figure 4.11: Simulated S-parameters of 3x8x350 μ m Stacked-FET versus number of sections per gate t .

Further verification of the simulation results is performed for $t=6$. This yields a 580-port EM simulation, as shown in Figure 4.12. A 3D view of this setup is shown in Figure 4.13. A comparison between the S-parameters simulated with the constructed model and the measured S-parameters of six $3 \times 8 \times 350 \mu\text{m}$ Stacked-FETs are shown in Figure 4.14. The main error is in the magnitude of S_{21} which is approximately 2 dB higher than in the measurements. For most other parameters a good match is observed over the entire frequency band from 1 GHz to 15 GHz.

Figure 4.12: Sonnet setup $3 \times 8 \times 350 \mu\text{m}$ Stacked-FET.

Figure 4.13: 3D view of Sonnet $3 \times 8 \times 350 \mu\text{m}$ Stacked-FET.

Figure 4.14: Simulated and measured S-parameters of 3x8x350 μm Stacked-FET.

4.5 Conclusion

The EM-based single gate finger model described in this chapter provides several degrees of freedom with respect to transistor layout, layer stack and scaling of unit gate finger width and number of gate-fingers. Besides the possibilities to correctly model very large transistor layouts, additional customisation of these layouts are supported. An example is the increase of the gate-to-gate spacing for the reduction of the thermal resistance.

The ability to create layouts significantly different than the standard CS layout on which standard compact models are usually based, suits very well with the requirements for the design of DCG transistors in the Stacked-FET. Additional degrees of freedom, for example to modify the drain-to-gate or drain-to-source spacing, require the correct inclusion of the access resistances in the EM simulation. Input for this could be obtained from a device simulator.

In this chapter the successful extraction of the intrinsic gate finger model parameters based on measurement on a $2 \times 67 \mu\text{m}$ transistor is presented. This model is used to simulate the S-parameters of the $3 \times 8 \times 350 \mu\text{m}$ Stacked-FET that was presented in chapter 3.

The current implementation only supports linear simulations of the transistor. It is expected that the extension to a non-linear model is well feasible. One of the drawbacks of the current implementation, however, is that no thermal coupling between the individual gate fingers is present. This effect will have a higher significance if the transistor is operated in its non-linear power range. To provide the required accuracy also at higher power levels, this thermal coupling needs to be implemented in the model.

CHAPTER 5

Stability analysis

5.1 Introduction

Stability is a major area of concern for any microwave amplifier design, due to the inherent relation between the stability of a transistor and its RF performance. For any type of RF circuit, instabilities result in degradation of RF performance or an increase of consumed DC power. For a power amplifier, additional effects are present. Instabilities might lead to instant destruction of the device which means that no measurement can be performed on the amplifier in its unstable state. Any analysis of the unstable behaviour is therefore only possible by means of simulations. At the same time, power amplifiers have many unstable modes due the parallel operation of a large amount of non-linear devices. The transistors in the amplifier can be stable under small-signal conditions but unstable in the non-linear power range or vice versa. Bias voltages, device temperature, process variations and ageing can all influence the stability of the amplifier. Instabilities can be present in the even mode, which is the normal mode of operation of the amplifier, but can also appear for any odd-mode combination of the parallel transistors. Within a Stacked-FET amplifier additional unstable modes are present due to the observed load mapping of the DCG transistor, as discusses in section 3.9, and the increased number of (bias) loops. The importance of a stable design is illustrated in Figure 5.1 which shows a power amplifier that failed during measurements due to oscillations.

Figure 5.1: Power amplifier failure due to instability.

Stability analyses are performed on three hierarchical levels for linear as well as non-linear operation:

1. The individual transistors in the stacks are analysed; this is the subject of section 5.2.
2. The full stacks are investigated; this is discussed in section 5.3.
3. The stability of the entire amplifier is investigated; details on this investigation are given in section 5.4.

Unless noted otherwise, the numerical examples given in this chapter are based on the characteristics of an $8 \times 350 \mu\text{m}$ transistor from the PP25-20 $0.25 \mu\text{m}$ GaAs process of WIN Semiconductors. The effective component values at a frequency of 3 GHz are determined from simulations using the EEHEMT1 model of this transistor at an operating power level that yields the maximum PAE: $C_{gs}=3 \text{ pF}$, $C_{ds}=850 \text{ fF}$, $C_{gd}=280 \text{ fF}$ and $g_m=0.3 \text{ S}$. In the DCG configuration, the balancing components $C_{gX}=1428 \text{ fF}$, and $C_{dsX}=994 \text{ fF}$ are included.

5.2 Stability of constitutive transistors

Stability analyses are first performed on the individual CS and DCG-FETs within the frequency range from zero to f_{max} of the transistors by means of the Rollett stability factor K .

Unconditional stability is not a strict requirement for the individual transistors, however, it reduces the risk of stability related problems within the Stacked-FET and is therefore preferred. For this reason the feasibility of unconditionally stable operation is investigated.

The stability of a two-port can be improved by adding a resistance at or between any of the ports. The effect of the different options on Rollett's stability factor- K is investigated based on the configurations shown in Figure 5.2.

(a) Shunt admittance G_{sh} at the terminals.

(b) Feedback admittance G_b between the terminals.

(c) Series Resistance R_s at the terminals.

(d) Feedback resistance R_a in the common path.

Figure 5.2: Resistors for stability improvement.

Rollett's stability factor K of the two-port with shunt admittance G_{sh1} and G_{sh2} between the terminals is given by:

$$K_{G_{sh}} = \frac{2\Re(y_{11} + G_{sh1})\Re(y_{22} + G_{sh2}) - \Re(y_{12}y_{21})}{|y_{12}y_{21}|}. \quad (5.1)$$

A similar equation is found for the two-port with series resistors R_{s1} and R_{s2} in series with the terminals:

$$K_{R_s} = \frac{2\Re(z_{11} + R_{s1})\Re(z_{22} + R_{s2}) - \Re(z_{12}z_{21})}{|z_{12}z_{21}|}. \quad (5.2)$$

Rollett's stability factor K of the two-port with feedback admittance G_b is given by:

$$K_{G_b} = \frac{2\Re(y_{11} + G_b)\Re(y_{22} + G_b) - \Re((y_{12} + G_b)(y_{21} + G_b))}{|(y_{12} + G_b)(y_{21} + G_b)|}. \quad (5.3)$$

Likewise for the two-port with feedback resistance R_a :

$$K_{R_a} = \frac{2\Re(z_{11} + R_a)\Re(z_{22} + R_a) - \Re((z_{12} + R_a)(z_{21} + R_a))}{|(z_{12} + R_a)(z_{21} + R_a)|}. \quad (5.4)$$

In the next sections the implications for the CS and DCG transistors are analysed.

5.2.1 CS-FET

Internal stability check

The internal stability of the $8 \times 350 \mu\text{m}$ CS-FET has been verified by measurements, as it was available as a test-structure. In a 50Ω environment, no instabilities have been observed. This satisfies the condition that was formulated by Rollett in his proviso [132, 133] and hence, stability can be further analysed externally.

External stability check

The single CS transistor very often shows a stability factor K lower than unity, especially for low frequencies, indicating the device is not unconditionally stable in this frequency range. Figure 5.3 shows the K -factor of the $8 \times 350 \mu\text{m}$ CS-FET. It can be seen that the device is not unconditionally stable for frequencies below 3.8 GHz.

Figure 5.3: K -factor of $8 \times 350 \mu\text{m}$ CS-FET.

CS stabilisation

An often used method to enhance the stability margin of the CS-transistor is by applying a suitable value of resistance at the gate of the transistor [37].

From Eqn. (5.2) it can be seen that any increase in R_{s1} directly results in an increased K . Based on the Z-parameters of the transistors, Eqn. (5.2) can be rewritten in order to determine the required resistance R_{s1} to obtain a target value for the stability factor K_{goal} :

$$R_{stab} = \frac{K_{goal}|Z_{12}Z_{21}| + \Re(Z_{12}Z_{21})}{2\Re(Z_{22})} - \Re Z_{11}. \quad (5.5)$$

Due to the frequency dependency of the Z-parameters, the required resistance is frequency dependent. In order to create some margin toward the conditional stable operation, a goal of $K=1.2$ is defined. The K -factor of the CS-FET without stability resistor, together with the resistance values required to obtain $K=1.2$ are shown in Figure 5.4. The required resistance value can be implemented with a parallel RC circuit directly connected to the gate of the transistor. The capacitance in the operating frequency band introduced by this RC network increases the Q-factor of the effective transistor input impedance and reduces the Bode-Fano [151] limit for the input matching, according to the mechanism that was described in section 3.7. For this reason this capacitance value should be as low as possible.

Since the RC network is applied at the gate of the CS-FET it affects the gain of the device and has only a secondary effect on the PAE. The output power delivered by the device is not altered. For this reason the CS-FET in the stack is designed unconditionally stable: it relaxes the requirements for the remaining DCG transistor(s), where stabilisation will have effect on output power and therefore also has a larger impact on the PAE.

Figure 5.4: K -factor of $8 \times 350 \mu\text{m}$ CS-FET and required value of R_{stab} to obtain $K=1.2$.

5.2.2 DCG-FET

Internal stability check

The transistor measurements for characterisation or modelling are usually performed on CS devices. This implies that no a priori knowledge regarding the stability of the single FETs in DCG configuration is available. For this reason extra care should be taken to verify Rollett's proviso. Before any two-port analysis on the DCG-FET is performed, the internal stability of the DCG-FET is verified. This verification is performed by means of an Ohtomo analysis [142] in combination with the intrinsic gate finger parameter extraction, that was the basis for the modelling technique described in the chapter 4. This is a good working combination, since the Ohtomo analysis technique is based on separate descriptions of the passive and active parts. The passive part consists of the metal parts of the DCG-FET and is simulated in Sonnet. To reduce complexity of the matrix manipulations, the access resistances are included in the active part which is further described by the Y-parameters of the intrinsic gate fingers. The Sonnet simulations on the metal parts are performed according to the approach described in section 4.4 for the entire stack: each gate finger is divided in six parts with a unit cell gate finger width of $\sim 58 \mu\text{m}$. The access resistances and the

Y-parameters that were extracted from the two finger device are linearly scaled to this unit cell gate finger width. Both the passive matrix $\mathbf{Y}_{EM}$ that is obtained from the Sonnet simulation and the active matrix representing the gate fingers have to be converted into a format suitable for the Ohtomo test. This means that the passive matrix should only contain ports that connect to the intrinsic transistor part.

Passive matrix

From the passive matrix $\mathbf{Y}_{EM}$ the external ports are removed and replaced by 50Ω terminations. The removal of a single port ① from an $N \times N$ matrix while adding admittance Y_{p1} is performed by applying:

$$\mathbf{Y} = \begin{vmatrix} Y_{EM_{22}} & \dots & Y_{EM_{2N}} \\ \vdots & \ddots & \vdots \\ Y_{EM_{N2}} & \dots & Y_{EM_{NN}} \end{vmatrix} - \begin{vmatrix} Y_{EM_{21}} \\ \vdots \\ Y_{EM_{N1}} \end{vmatrix} \cdot \frac{1}{Y_{EM_{11}} + Y_{p1}} \cdot |Y_{EM_{12}} \dots Y_{EM_{1N}}| \quad (5.6)$$

This is performed twice, resulting in $M \times M$ matrix where $M=N-2$. The two gate connections per gate finger in the resulting matrix are connected mathematically:

$$Y'_{4r-2,4p-2} = Y_{4r-2,4p-2} + Y_{4r,4p}, \quad (5.7)$$

for even rows and columns and

$$Y'_{2r-1,2p-1} = Y_{2r-1,2p-1} \quad (5.8)$$

for odd rows and columns, with r and p are positive integers.

This results in a 144-port passive matrix with three ports per unit intrinsic gate finger.

Active matrix

The extraction of the two-port Y-matrix $\mathbf{Y}_{UGF}$ that describes a single intrinsic gate finger was performed on a transistor with a unit gate width of $67 \mu\text{m}$, while the required unit cell gate width is $58 \mu\text{m}$. The two-port matrix is therefore scaled using a factor $s_{UGW}=58/67$. The scaled Y-matrix is then converted into a Z-matrix and the resistance values, scaled with the same factor s_{UGW} , are added to the individual elements to obtain the required Single Gate Finger (SGF) matrix $\mathbf{Y}_{SGF}$:

$$\mathbf{Y}_{SGF} = \left(\frac{1}{s_{UGW} \cdot \mathbf{Y}_{UGF}} + \begin{vmatrix} \frac{R_s}{s_{UGW}} + s_{UGW} \cdot R_g & \frac{R_s}{s_{UGW}} \\ \frac{R_s}{s_{UGW}} & \frac{R_d + R_s}{s_{UGW}} \end{vmatrix} \right)^{-1} \quad (5.9)$$

The SGF matrix is converted into a three-port equivalent matrix $\mathbf{Y}'_{SGF}$, to provide access to the source node. At the same time the ports are reordered to match the port numbers of the passive part (①=source, ②=gate, ③=drain):

$$\mathbf{Y}'_{SGF} = \begin{vmatrix} Y_{SGF_{11}} + Y_{SGF_{12}} + Y_{SGF_{21}} + Y_{SGF_{22}} & -Y_{SGF_{11}} - Y_{SGF_{21}} & -Y_{SGF_{22}} - Y_{SGF_{12}} \\ -Y_{SGF_{11}} - Y_{SGF_{22}} & Y_{SGF_{11}} & Y_{SGF_{12}} \\ -Y_{SGF_{22}} - Y_{SGF_{21}} & Y_{SGF_{21}} & Y_{SGF_{22}} \end{vmatrix} \quad (5.10)$$

The 3x3 matrix is duplicated 48 times to construct an overall 144 port matrix required for the Ohtomo analysis:

$$\mathbf{Y}_{act} = \begin{vmatrix} \mathbf{Y}'_{SGF} & 0 & \dots & 0 \\ 0 & \mathbf{Y}'_{SGF} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & \mathbf{Y}'_{SGF} \end{vmatrix} \quad (5.11)$$

The dimensions of this active matrix now equal the size of the passive matrix.

Analysis and interpretation of results

The passive and active Y-matrices are converted to S-parameter matrices $\mathbf{S}_{pas}$ and $\mathbf{S}_{act}$ respectively to construct the 144-port matrix $\mathbf{M}_{144}$ required for the Ohtomo analysis, as described in section 2.4.3:

$$\mathbf{M}_{144} = \mathbf{S}_{pas} \cdot \mathbf{S}_{act} - \mathbf{I}_{144}. \quad (5.12)$$

After calculating all the loops, instabilities are automatically extracted based on the Nyquist criteria for oscillation. With loop gain values $G(f_x)$ and $G(f_{x-1})$ calculated at discrete, consecutive frequency points f_x and f_{x-1} , the Nyquist criteria for oscillation is met if $\angle G(f_x) > n \cdot 2\pi$ and $\angle G(f_{x-1}) < n \cdot 2\pi$ while $|G(f_x)| > 1$ or $|G(f_{x-1})| > 1$.

The results from the analysis are given in Figure 5.5. At each analysed bias point, an indication is given whether the transistor is stable (green) or unstable (red). It is observed that the device is potentially unstable for a window of relatively low drain-to-source voltages and relatively high gate-to-source voltages, which corresponds to the findings in section 3.5.2. Under nominal operating voltages the device is found to be stable.

Figure 5.5: Indication of stability for 8x350 μm DCG-FET, green: stable, red: unstable.

External stability check

The stability of the DCG-FET is initially analysed without any additional stabilising components. For this analysis the three port FET Y-matrix $\mathbf{Y}_F$ is combined with the external balancing admittances Y_{gX} and Y_{dsX} . The three port Y-matrix of a small signal equivalent intrinsic FET model (①=source, ②=drain, ③=gate) is given by :

$$\mathbf{Y}_F = \begin{pmatrix} Y_{gs} + Y_{dsT} + g_m & -Y_{dsT} & -Y_{gs} - g_m \\ -Y_{dsT} - g_m & Y_{dsT} + Y_{gd} & -Y_{gd} + g_m \\ -Y_{gs} & -Y_{gd} & Y_{gs} + Y_{gd} \end{pmatrix}, \quad (5.13)$$

with $Y_{dsT} = Y_{ds} + Y_{dsX}$. The external gate admittance is included by adding Y_{gX} to $Y_{DCG_{33}}$. The resulting three port matrix is reduced according to:

$$\mathbf{Y}_{\text{DCG}} = \begin{pmatrix} Y_{DCG_{11}} & Y_{DCG_{12}} \\ Y_{DCG_{12}} & Y_{DCG_{22}} \end{pmatrix} - \begin{pmatrix} Y_{DCG_{13}} \\ Y_{DCG_{23}} \end{pmatrix} \cdot \frac{1}{Y_{DCG_{33}} + Y_{gX}} \cdot \begin{pmatrix} Y_{DCG_{31}} & Y_{DCG_{32}} \end{pmatrix}, \quad (5.14)$$

which results in:

$$\mathbf{Y}_{\text{DCG}} = \begin{pmatrix} Y_{DCG_{11}} - \frac{Y_{DCG_{13}}Y_{DCG_{31}}}{Y_{DCG_{33}} + Y_{gX}} & Y_{DCG_{12}} - \frac{Y_{DCG_{13}}Y_{DCG_{32}}}{Y_{DCG_{33}} + Y_{gX}} \\ Y_{DCG_{21}} - \frac{Y_{DCG_{23}}Y_{DCG_{31}}}{Y_{DCG_{33}} + Y_{gX}} & Y_{DCG_{22}} - \frac{Y_{DCG_{23}}Y_{DCG_{32}}}{Y_{DCG_{33}} + Y_{gX}} \end{pmatrix}. \quad (5.15)$$

By substitution of (5.13) and (5.14) into (5.15) equation (5.16) is obtained:

$$\mathbf{Y}_{\text{DCG}} = \begin{pmatrix} \frac{j\omega C_{gs}(-j\omega C_{gs} - g_m)}{j\omega(C_{gs} + C_{gd} + C_{gX})} + j\omega(C_{gs} + C_{dsT}) + g_m & \frac{j\omega C_{gd}(-j\omega C_{gs} - g_m)}{j\omega(C_{gs} + C_{gd} + C_{gX})} - j\omega C_{dsT} \\ \frac{j\omega C_{gs}(g_m - j\omega C_{gd})}{j\omega(C_{gs} + C_{gd} + C_{gX})} - j\omega C_{dsT} - g_m & \frac{j\omega C_{gd}(g_m - j\omega C_{gd})}{j\omega(C_{gs} + C_{gd} + C_{gX})} + j\omega(C_{gd} + C_{dsT}) \end{pmatrix}. \quad (5.16)$$

By substitution of Eqn. (5.16) into Eqn. (2.36), the stability factor K for the DCG-FET can be written as:

$$K = 2\Re \left(\frac{jC_{gd}\omega(g_m - jC_{gd}\omega)}{j\omega(C_{gs} + C_{gd} + C_{gX})} + j\omega(C_{gd} + C_{dsT}) \right) \cdot \frac{\Re \left(\frac{j\omega C_{gs}(-j\omega C_{gs} - g_m)}{j\omega(C_{gs} + C_{gd} + C_{gX})} + j\omega(C_{gs} + C_{dsT}) + g_m \right)}{\left| \frac{j\omega C_{gs}(g_m - j\omega C_{gd})}{j\omega(C_{gs} + C_{gd} + C_{gX})} - jC_{dsT}\omega - g_m \right| \left| \frac{j\omega C_{gd}(-j\omega C_{gs} - g_m)}{j\omega(C_{gs} + C_{gd} + C_{gX})} - jC_{dsT}\omega \right|} \cdot \frac{\Re \left(\left(\frac{j\omega C_{gs}(g_m - j\omega C_{gd})}{j\omega(C_{gs} + C_{gd} + C_{gX})} - j\omega C_{dsT} - g_m \right) \left(\frac{j\omega C_{gd}(-j\omega C_{gs} - g_m)}{j\omega(C_{gs} + C_{gd} + C_{gX})} - j\omega C_{dsT} \right) \right)}{\left| \frac{j\omega C_{gs}(g_m - j\omega C_{gd})}{j\omega(C_{gs} + C_{gd} + C_{gX})} - j\omega C_{dsT} - g_m \right| \left| \frac{j\omega C_{gd}(-j\omega C_{gs} - g_m)}{j\omega(C_{gs} + C_{gd} + C_{gX})} - j\omega C_{dsT} \right|}. \quad (5.17)$$

Eqn. (5.17) can be simplified to:

$$K = \frac{(C_{gd}C_{gs} + C_{dsT}C_{gs} + C_{dsT}C_{gd} + C_{gX}C_{dsT})^2 \omega^2 + C_{gd}^2 g_m^2 + C_{gX}C_{gd}g_m^2}{\sqrt{(C_{gd}C_{gs} + C_{dsT}C_{gs} + C_{dsT}C_{gd} + C_{gX}C_{dsT})^2 \omega^2 + C_{gd}^2 g_m^2}} \cdot \frac{1}{\sqrt{(C_{gd}C_{gs} + C_{dsT}C_{gs} + C_{dsT}C_{gd} + C_{gX}C_{dsT})^2 \omega^2 + (C_{gd}g_m + C_{gX}g_m)^2}}. \quad (5.18)$$

If $C_{gX} = 0$, Eqn. (5.18) evaluates to $K = 1$, which can be explained by the fact that when the gate of the DCG-FET is left open, the device has no gain and therefore cannot oscillate. For higher values of C_{gX} the value of K reduces. As C_{gX} is smaller for FETs higher in the stack, as was found in section 3.6.1, the stability is most critical for the first DCG transistor in the stack.

DCG stabilisation

The effect of the four configurations of stability resistors, described in Figure 5.2, on the K -factor of the DCG-FET was analysed and it was found that only the series resistance R_{s1} at the input, the series resistance R_{s2} at the output and the feedback resistance R_a at the common path yield a significant stability improvement. Both series resistances R_{s1} and R_{s2} are in the high (RF) current path which means that even for low resistance values, a significant voltage drop is obtained that results in a degradation of RF performance. For this reason the feedback resistance R_a was selected as a preferred solution. This feedback resistance is in series with the voltage balancing capacitance C_{gX} , as indicated in Figure 5.6.

Figure 5.6: Stability resistor R_a for DCG transistor.

The value of R_a for a target stability factor value K_{goal} can be found by solving Eqn. (5.4) for $K_{R_a}^2 = K_{goal}^2$, although this also provides solutions for $K_{R_a} = -K_{goal}$. To obtain some margin toward the point of conditional stability, a target stability factor of $K_{goal}=1.2$ is selected. The obtained four possible solutions for a value of $K_{R_a}^2 = 1.2^2$ are given in the left column of Figure 5.7. As the obtained results are complex they are denoted as Z_a . The second column of the figure gives the original K -factor together with the resulting K -factor when either the obtained complex value of Z_a or only the real part of Z_a are applied. From the resulting K -factor when the complex Z_a is applied, it can be found if this solution yields the required $K = 1.2$ or the undesirable solution $K = -1.2$.

The solutions Z_{a1} and Z_{a2} yield the required results for frequencies higher than approximately 5.5 GHz. For these solutions, the imaginary part equals zero for frequencies higher than 9 GHz. Applying an impedance that consists of just the real part of Z_{a1} or Z_{a2} improves the K -factor for frequencies above 3 GHz. The solution Z_{a3} and Z_{a4} yield unconditionally stable results for frequencies below 12.5 GHz, however, the real part of the required impedances is negative.

It is concluded that the DCG-FET cannot be made unconditionally stable by using a single resistor in series with the external gate capacitance alone. A complex impedance is required, however this disturbs the operation of the stack as it effectively changes the balancing reactance at the gate. Stability using multiple stability resistances is further analysed for the entire Stacked-FET, where the interaction between the transistors in the stack can be taken into account.

Figure 5.7: The four solutions of $K^2(Z_a) = 1.2^2$ and the corresponding effect on Rollett's stability factor K .

5.3 Stability of Stacked-FET

The Stacked-FETs that are described in this thesis are designed to be unconditionally stable, without the requirement of unconditional stability for the transistors in the stack. This implies that stability needs to be investigated for the entire Stacked-FET, which is the subject of this section. The analysis of the stability of a Stacked-FET can only be performed after the balancing of the stack, i.e. if all the external components are known.

5.3.1 Conditional stability evaluation in transistor stacks

Stability analysis based on stability factors K or μ is of limited value for the design of the DCG transistors. The impedance mapping function of these DCG transistors are such that the circle of unit magnitude reflection coefficient on the drain side can be mapped to a region including parts outside of the Smith chart, as was shown in section 3.9. In other words, a purely passive termination of the DCG transistor can result in an input impedance with a negative real part. Furthermore, for a Stacked-FET containing more than two transistors, internal oscillations might be present that are not observable on the external ports.

Figure 5.8: Stability verification by means of load mapping and stability circles.

For the mentioned reasons an alternative method is applied which uses the drain-to-source mapping function of the DCG transistor(s). The mapping of the load regions of the DCG transistor are compared to the load stability circles, as defined by Eqn. (2.31) and Eqn. (2.32), of the preceding transistor(s). This is indicated in Figure 5.8 (a) for comparison at the source of the upper DCG transistor and in Figure 5.8 (b) for comparison at the source of the lower DCG transistor. If the mapping area from the load to the comparison point is entirely inside the stable region of the preceding transistor(s), no passive external impedance exists that causes an instability, i.e. the combination of transistors is unconditionally stable. This analysis should be repeated at the source node of each DCG transistor.

The eight options for stability circle and mapping region combinations are indicated in Figure 5.9, where the load stability circle is defined by c_L and r_L while the mapping circle is defined by c_{map} and r_{map} . In Figure 5.9 (a) and (b) the mapping circle is entirely outside of the stability circle. For case (a) where the stable region is outside, this means that the combination is unconditionally stable while for case (b) where the stable region is inside, the combination is entirely unstable. In Figure 5.9 (c) and (d) the mapping circle intersects the stability circle which means that regardless of the location of the stable region, none of the two cases is unconditionally stable. In Figure 5.9 (e) and (f) the mapping circle is entirely inside the stability circle which means that the combination is unconditionally stable if the stable region is inside as in situation (e). Otherwise as in the situation (f), the combination is entirely unstable. In Figure 5.9 (g) and (h) the mapping circles encloses the stability circle. Regardless of the location of the stable region these combinations are not unconditionally stable.

Figure 5.9: All combinations of stability and mapping circles, grey indicates the stable areas.

To discriminate between the different combinations, the following parameters are introduced:

$$m1 = |c_L - c_{map}| - (r_L + r_{map}) \quad (5.19)$$

and

$$m2 = |c_L - c_{map}| - (r_L - r_{map}). \quad (5.20)$$

If $m1 > 0$, the mapping circle and stability circle are entirely separated which results in unconditional stability only if the stable region is outside. $m2 < 0$ indicates that the mapping circle is located entirely inside the stability circle which results in unconditional stability only if the stability region is inside. To include the conditions of the location of the stable region the parameters $M1$ and $M2$ are defined as:

$$M1 = \begin{cases} m1 & \text{if stability region is outside,} \\ -m1 & \text{if stability region is inside} \end{cases} \quad (5.21)$$

and equivalently:

$$M2 = \begin{cases} m2 & \text{if stability region is outside,} \\ -m2 & \text{if stability region is inside.} \end{cases} \quad (5.22)$$

Table 5.1 give the signs of the parameters $M1$ and $M2$ for the eight cases and indicates whether a situation yields unconditional stability. For unconditional stability, both $M1$ and $M2$ should be positive.

Table 5.1: Stability options.

Case	Region	$M1$	$M2$	Unconditionally stable
(a)	Outside	> 0	> 0	Yes
(b)	Inside	< 0	< 0	No
(c)	Outside	< 0	> 0	No
(d)	Inside	> 0	< 0	No
(e)	Outside	< 0	< 0	No
(f)	Inside	> 0	> 0	Yes
(g)	Outside	< 0	> 0	No
(h)	Inside	> 0	< 0	No

5.3.2 Implications for Stacked-FET design

The effect of the stability considerations on Stacked-FET performance and design are illustrated by analysing a stack of three transistors. As multiple options to stabilise the stack may exist, a procedure should be defined to find the solutions which yields the best RF performance while keeping the stack stable. A brute-force method is used in which a predefined range of possible options is analysed and the best option is chosen based on simulated RF output power and PAE. The variations applied for stability improvement are the external gate resistances $R_{gX,n}$, the external drain-to-source resistances $R_{dsX,n}$ and the single transistor load $Y_{L,fet}$ as indicated in Figure 5.10. The single transistor load $Y_{L,fet}$ used during the design of the stack determines the external balancing components and hence the mapping function of the DCG transistors, which has a large effect on the overall stability. As mentioned in section 5.2.2, the use of series resistors at the drain and source terminals of the DCG transistors are avoided because of the large (RF) currents at these nodes.

Figure 5.10: Stabilised stack of 3 FETs.

The flow graph for the brute-force stabilisation is depicted in Figure 5.11. During each trial a set of transistor loads and stabilisation resistors is generated and the Stacked-FET is optimised for this combination of parameter values. Then the stability of the current solution is analysed and if the stack is found to be unconditionally stable, i.e. the parameter $M1$ and $M2$ are larger than zero for all frequencies, the RF performance is determined using a Harmonic Balance (HB) simulator and stored.

Figure 5.11: Flow graph for brute-force Stacked-FET stabilisation.

5.4 Amplifier stability

Within a Stacked-FET HPA generally a number of stacks is placed in parallel to contribute to the total output power of the amplifier. After the analysis and stabilisation of the individual stacks, the stability of the combination of these stacks should be investigated. The stability of the entire amplifier is verified via an internal stability analysis using either pole-zero identification or Ohtomo tests under small signal and large signal conditions. Besides the extensively discussed two-port and loop instabilities, additional mechanisms are the odd-mode oscillation [134,164] where two groups of transistor oscillate in phase opposition, and parametric oscillations [165–168] appearing at sub-harmonics frequencies due to the non-linearities of the intrinsic capacitances of the transistors.

5.4.1 Stability analysis on amplifier

The large signal stability analysis is performed for various power levels from the small signal regime into deep saturation. As explained in section 2.4.3, the HPA is excited with a drive signal at frequency f_{LS} while a small test tone with a frequency from 0 to $f_{LS}/2$ is applied to the testing node. If the amplifier is found to be stable under the nominal load conditions, the unconditional stability is checked. For the small signal case this check can be performed with two-port techniques. The effect of load and source impedance on stability under large signal conditions is analysed by either applying the two-port techniques to a set of linearised HPA characteristics or by the performance of an internal analyses for various loading conditions. Neither of the two methods, however, is comprehensive. Linearisation of the non-linear HPA characteristics are an approximation only valid at a single power level, while the internal analyses can only be performed for a finite set of source and load impedance values. The two methods are therefore complementary, but care should be taken to cover all relevant conditions which follow from either the specifications or the environmental conditions in which the amplifier operates.

The entire stability analysis of the amplifier is carried out for various supply voltage levels, and temperatures. For both the voltage and temperature ranges the nominal and worst case operating conditions as well as the start-up conditions have to be considered. During start-up the bias voltages vary from zero to the nominal values, while the temperature can be as low as the minimum storage temperature. Stability needs to be ensured under all these conditions. Finally an Monte Carlo (MC) stability test is performed to guarantee stable operation for all possible combinations of components parameters.

5.4.2 Biasing of DCG gates

The gate of each individual DCG-FET needs to be supplied with a gate voltage. Direct combination of all these gates yields a large number of (RF) loops which results in many options for oscillations. RF isolation between the individual gate connections can be obtained by supplying each single gate from an individual active gate bias circuit as was introduced in section 3.8.3, which provide the optimum gate voltages with varying supply voltage and threshold voltage variation. A drawback is that additional circuitry is required which increases the chip size. An alternative option is to place large resistors directly in series with the individual gates. Although the level of isolation is lower for this option, the damping within the RF loops can be sufficient to resolve occurrence of loop oscillations.

5.5 Conclusion

In this chapter the stability aspects contained in the design of a Stacked-FET are addressed. Initially stability considerations are given based on the two-port characteristics of the individual transistors. Later the interaction between the transistors is analysed and the stability of the entire Stacked-FET is investigated.

The enhancement of the stability margin starts at the CS transistor. The CS transistor is made unconditionally stable since this relaxes the DCG stability requirements while the penalty in RF performance of the Stacked-FET is smaller. A stability network containing a resistor and a capacitor in parallel is placed in series with the gate. The real part of the series impedance that is introduced by this RC-network shows a frequency dependency such that the required resistance to reach predefined target value of K is obtained or exceeded.

The required external gate admittance for a target K -factor above 1 is analytically determined. It is found that no real external gate admittance exists to stabilise the DCG-FET. Applying a complex admittance disturbs the voltage balancing of the DCG transistor and therefore degrades the RF performance of the Stacked-FET. The DCG transistors are not necessarily unconditionally stable, instead the interaction between the transistors in the Stacked-FET is analysed. This is done by comparing the mapping functions from the external load to any of the sources of the transistors in the Stacked-FET with the load stability circles from the gate of the CS FET to that same source. A brute-force method is described to integrate the stability analysis in the optimisation and balancing of a Stacked-FET. Within this algorithm multiple balancing and stability components are varied and the effect on both stability and RF-performance is analysed.

After design of a stable Stacked-FET, the stability of an amplifier containing this Stacked-FET needs to be analysed. Stability between the RF ports as well as via the bias connections is investigated, both under small signal and large signal circumstances, for all expected values of bias voltage, RF frequency, input power, temperature and processing conditions. Besides stability for the nominal (even) mode of operation, odd-mode stability as well as the absence of parametric oscillations should be verified.

CHAPTER 6

Stacked-FET Power Amplifiers

6.1 Introduction

In the previous chapters the design and analysis of individual Stacked-FETs was discussed. The techniques that were developed in these chapters are applied to the design of Stacked-FETs that are used as building blocks for two power amplifiers. In this chapter the design procedure and results of these amplifiers is described. The Stacked-FETs of the first HPA are designed according to the procedure given in chapter 3. After the dimensioning of the stacks the stability was verified and stability measures were taken in order to obtain a stable design. During the design of the second amplifier the stability considerations were included as an integral part of the stack design using the procedure described in chapter 5. This amplifier is designed for packaging in a QFN type package. A test board is designed in order to measure the performance of these packaged amplifiers. This test board is shown in Figure 6.1.

The target specifications for the designed amplifiers are given in Table 6.1. The amplifiers are single-ended microstrip devices with an input and output impedance of $50\ \Omega$.

Recently the use of Ruthroff [169] and trifilar [170] transformers have been demonstrated to be beneficial for wide-band amplifiers that are not internally matched to $50\ \Omega$ [171, 172]. This technique is applied to amplifiers using the Non-Uniform Distributed Power Amplifier (NDPA) topology, where the bandwidth is not Fano-limited. For the amplifiers described in this chapter, one of the goals is the reduction of chip-size. The voltage-summation based combining of power from the transistor in the stacks supports this goal as it reduces the

amount of passive power combiners at the output. The use of transformers at the input or output of the amplifiers, however, is in contradiction to the goal of chip area reduction. In chapter 3 it was shown that no practical bandwidth limitations are expected for the Stacked-FETs under consideration, therefore the amplifiers described in this chapter are directly matched to the required output impedance of $50\ \Omega$.

Table 6.1: Target specifications for HPA demonstrators.

	Operating frequency (GHz)	Output power (W)	PAE (%)	Gain (dB)
HPA1	2.9 to 3.4	20	40	15
HPA2	2.9 to 3.4	30	40	25

Figure 6.1: Test-board for measurements on packaged devices.

6.2 Amplifier design

In this section the design of the Stacked-FET HPAs is described. In the first part an overview of the different design steps is given, the remaining parts give further details on several of these steps.

6.2.1 Design procedure

In Figure 6.2 the flow chart of a typical HPA design procedure is given. The first step in this procedure is the considerations of the target specifications. During this step it is verified whether the set of specified parameters are consistent and contain no internal contradictions. Besides the RF-performance, these specifications can also contain environmental conditions, packaging or cost price requirements. The target specifications for the HPAs to be designed were given in the previous section.

If the set of specifications is found to be consistent, a suitable technology is chosen, based on the relevant figures of the active devices in that technology; in particular the output power, efficiency and gain of the available transistors. If in some case no suitable technology is found for the set of target specifications, a reconsideration of these target specifications might be required. For the current development the WIN PP25-20 technology was selected.

During the definition of the amplifier architecture the number of stages, number of stacks per stage, the number of transistors per stack and the transistor sizes are defined and an estimation of the RF-performance is made. If no suitable architecture is found, the specifications are to be reconsidered or an alternative technology should be selected.

After the definition of the architecture, the stacks are designed according to the procedure that was described in chapter 3 and chapter 5. The stability of the transistors and the stacks is verified during this stage. Once the design of the stacks is finished, the assumptions on stack performance that were made during the architecture definition can be verified. If the obtained performance is worse than assumed, the architecture should be modified. In some cases it might even be necessary to go back to the technology selection or specification considerations.

When the HPA architecture is defined and the stacks are designed, the impedance levels at the input and output of the amplifier stages are known. At this point the matching networks are designed. These matching networks should provide the required impedance levels to the input and output of the amplifier stages while supporting the biasing requirements such as the DC supply to the transistors in the stages and DC blocking in-between the stages. At this point in the design also the gate biasing of the amplifier is implemented.

After the composition of the total amplifier, the overall performance is analysed and the stability of the amplifier is verified for all expected values of biasing voltage, temperature, output and input load, RF excitation, etc. Analysis of the RF-characteristics is performed by HB techniques using non-linear transistor models and includes a thermal analysis on the amplifier layout. At this point the amplifier design is finished if all target specifications are complied to, the amplifier is stable under all possible conditions and the highest level of modelling accuracy is reached. If the latter is not the case, the modelling accuracy of the matching networks is improved and the amplifier performance is reanalysed. This loop comprises the transition from the simplest form of modelling, ideal lumped components, to the most complete form, performing an EM analysis on the entire passive network.

Figure 6.2: HPA design procedure.

6.2.2 Power stages

In general, the design of the power amplifier starts with the definition of the power stages, starting at the output stage. The total gate width of the HPA stages is determined by the output power required from these stages, in combination with the power density that can be obtained from the transistors. For a Stacked-FET stage that contains stacks of N transistors, the number of devices in parallel is a factor N smaller in comparison to a classical CS stage. This is illustrated in Figure 6.3, where two options for an amplifier stage containing six transistors are shown. The first option contains CS transistors only and the second options contains stacks of three transistors. If T is the required number of transistors in the stage and N is the number of FETs per stack, the number of stacks in parallel equals T/N .

Figure 6.3: Power stages containing six transistors, (a) with CS transistors and (b) with two stacks of three FETs.

The optimum load impedance $Z_{L,tot}^{CS}$ of the power stage containing only CS transistors equals the optimum load impedance of a single CS transistor $Z_{L,CS}$ divided by the number of transistors T :

$$Z_{L,tot}^{CS} = \frac{Z_{L,CS}}{T}. \quad (6.1)$$

In section 3.4.4 it was shown that the required load impedance of a Stacked-FET containing N transistors is approximately N times higher than the optimum load impedance of a single CS transistor $Z_{L,CS}$. This means that for a Stacked-FET power stage, the required total load impedance $Z_{L,tot}^{stack}$ of the stage equals:

$$Z_{L,tot}^{stack} \approx \frac{N}{T} \cdot N \cdot Z_{L,CS} = \frac{N^2 \cdot Z_{L,CS}}{T}. \quad (6.2)$$

From the ratio between Eqn. (6.1) and Eqn. (6.2) it can be found that the required

load impedance of a Stacked-FET power stage is approximately N^2 times the optimum load impedance of a CS power stage.

The input impedance of the option with six CS transistors equals the impedance of a single CS transistor $Z_{in,CS}$ divided by six. The input impedance of the option with two Stacked-FETs, however, equals the impedance of a single CS transistor divided by two. In general it can be concluded that the ratio between the input impedance Z_{in}^{CS} of a CS-only stage and the input impedance Z_{in}^{stack} of a Stacked-FET stage containing stacks of N transistors is:

$$\frac{Z_{in}^{stack}}{Z_{in}^{CS}} = \frac{T}{N \cdot Z_{in,CS}} \cdot \frac{Z_{in,CS}}{T} = N. \quad (6.3)$$

6.2.3 HPA topology

In section 3.8.4 it was shown that in comparison to a CS stage, not only the output power of Stacked-FET is higher, but the gain increases as well. This increase in gain is equal to the increase in output power and means that, theoretically, the PAE of a Stacked-FET can be higher than for a CS stage, since the PAE is closer to the drain efficiency. Due to the increased gain, the number of stages in a Stacked-FET HPA is not expected to be larger than two since an amplifier with a (small-signal) gain higher than 40 dB is often not required and can, especially for a packaged device, be a cause of stability problems related to output-to-input coupling.

A general topology of a two-stage Stacked-FET HPA is given in Figure 6.4. Such a two-stage amplifier is the simplest form of an amplifier that includes all possible parts an HPA can contain, such as amplifier stages, an IMN, Output Matching Network (OMN) and an Inter Stage Matching Network (ISMN). Stage 2, the output stage, delivers the total output power of the amplifier. Stage 1, the input stage, serves as a driver stage to increase to total gain of the HPA. Each stage x consists of S_x stacks in parallel with a number of N_x FETs per stack. Preferably the number of FETs per stack is equal for both stages as this removes the requirement for multiple drain supply voltages. Due to the high gain of the stacks, the required output power from the input stage (and hence the number of stacks) in the input stage stage is usually low. Often the input stage consists of just a single stack. If the given, general topology is used to describe a single stage amplifier, the input stage and IMN are defined to have zero gain and no power limitations and consumption such that these do not have an effect on the amplifier performance.

The OMN transforms the external 50Ω impedance to a required load impedance of the stacks in the output stage. In the previous section it was shown that the real part of this load impedance is approximately N^2 times larger than that of a comparable CS stage, which results in a lower matching ratio. As

discussed in section 3.7.3, this results in a higher obtainable bandwidth for this matching network.

The IMN transforms the input impedance of the CS transistors in the stack to the required external impedance of $50\ \Omega$. As the real part of this input impedance is N times larger than for a CS stage, also for this matching network the matching ratio is lower, though not as low as for the OMN.

The ISMN matches the (CS) input impedance of the output stage to the required load impedance of the input stage. The real part of the input impedance of the transistors in the output stage is often low. The required load impedance of the Stacked-FET input stage has a real part that is larger than for a standard CS stage, which means that the matching ratio for the interstage matching is significantly higher than for a CS amplifier. For this reason, the ISMN is expected to be the limiting factor with respect to obtainable bandwidth.

Figure 6.4: General topology of a two-stage Stacked-FET HPA.

The actual amplifier design starts with the definition of the amplifier architecture. The architecture of the amplifier is based on several key parameters, such as:

- Selected technology
- Output power
- Operating frequency band
- Supply voltage
- Thermal behaviour and limitations
- Maximum chip size

The performance of the power amplifier is dominated by the transistor performance, which in turn is determined by the transistor geometry in relation to operating frequency, the loading and biasing conditions and thermal effects. Besides the thermal effects on RF-performance, the thermal limitations with respect to reliability need to be considered. The maximum chip size in both x and y direction can have consequences for the number of transistors in a stack and the

number of stacks that can be placed in parallel. In order to make an appropriate choice, an estimation of amplifier performance should be made based on basic transistor parameters such as output power density, efficiency and gain. This is the subject of the next section.

6.2.4 A priori amplifier performance estimation

An iterative procedure for the estimation of the performance is illustrated in Figure 6.5. The electrical performance of a single transistor is determined from measurements or simulations, as was extensively described in chapter 3. To include the temperature and supply voltage dependency, the coefficients for output power density, drain current and gain are obtained from measurements or simulation data at different temperatures or drain voltages. The thermal model is obtained from closed form analyses [173,174] or numerical simulations. Packaging and dynamic aspects (operation pulse width and duty cycle) are included in the thermal model.

Figure 6.5: Estimation of amplifier architecture performance.

The estimation procedure starts at the output stage of the HPA. The estimated performance of the output stage is obtained from the total gate width in combination with the output power density for the stage at a predefined optimum operating point. This can be defined as the power level where the PAE is maximal, a certain gate current limit is exceeded or the maximum allowed compression level is achieved. In order to meet the required total gate width the degrees of freedom are:

- Number of Gate Fingers (NGF) per transistor
- Unit Gate Width (UGW)

- Number of transistors in stack (N)
- Number of stacks in parallel (S)

The total output power of the output stage P_{out_2} is determined by the gate width dependent output power density at the optimum operating point $P_{dens_2}(W_u)$, the number of transistors per Stacked-FET in the output stage N_2 , the number of gate fingers and gate width of the transistors in the output stage, N_{gf_2} and W_{u_2} respectively, the number of paralleled Stacked-FETs in the output stage S_2 and the stacking loss $L_{stacking}$ which is a measure for loss due to imperfect balancing and stabilisation of the stack:

$$P_{out_2} = S_2 \cdot N_2 \cdot N_{gf_2} \cdot W_{u_2} \cdot P_{dens_2}(W_u) \cdot L_{stacking}. \quad (6.4)$$

The total output power of the HPA $P_{out_{HPA}}$ is calculated using the loss of the OMN L_{OMN} , defined as the reciprocal of the power gain of that matching network, according to:

$$P_{out_{HPA}} = \frac{P_{out_2}}{L_{OMN}}. \quad (6.5)$$

The input power of the output stage P_{in_2} depends on the gain G_{P_2} of that stage:

$$P_{in_2} = \frac{P_{out_2}}{G_{P_2}}. \quad (6.6)$$

The required output power $P_{out_{FET1}}$ of a single transistor within the Stacked-FET in the input stage is obtained from the loss of the ISMN L_{ISMN} , the number of transistors per Stacked-FET in the input stage N_1 (which usually equals N_2) and the number of paralleled Stacked-FETs in the input stage S_1 :

$$P_{out_{FET1}} = \frac{P_{in_2} \cdot L_{ISMN}}{N_1 \cdot S_1}. \quad (6.7)$$

The input stage is normally operated under back-off. The extra power margin of the input stage ensures the capability to drive the output stage into compression, even if the gain of the output stage is lower than expected due to process or temperature variations. This means that the key parameters of the transistors in the input stage should be determined for a compression level lower than present in the output stage. This is done by fitting the output power density P_{dens} , drain current I_d and power gain G_P , against the Normalised output Power Density (NPD), which is defined unity at the power density at the optimum operating point P_{dens_2} :

$$NPD = \frac{P_{dens}}{P_{dens_2}}. \quad (6.8)$$

The effective gain and drain current of the first stage transistors can now be determined and all other HPA parameters can be derived. This includes

an updated estimation of dissipation and channel temperature. This data is fed back to the thermal model calculation and transistor parameter estimation respectively. An new iteration is started and the performance calculation is updated. After convergence of this iterative loop, the estimated HPA characteristics are available.

Based on the estimated maximum channel temperature and the reliability data of the process the amplifier Mean Time To Failure (MTTF) [175] can be determined. This MTTF shows a very strong dependency on transistor temperature which is described by the Arrhenius relation [176]:

$$\text{MTTF}|_{T_{ch}} = \text{MTTF}|_{T_{ref}} e^{\frac{E_a}{k} \left(\frac{1}{T_{ch}} - \frac{1}{T_{ref}} \right)}, \quad (6.9)$$

where $\text{MTTF}|_{T_{ch}}$ is the MTTF at channel temperature T_{ch} , $\text{MTTF}|_{T_{ref}}$ is the MTTF at reference temperature T_{ref} , k is the Boltzmann constant and E_a is a process dependent activation energy.

This equation shows the strong life time degradation due to temperature increase. An increase in transistor channel temperature of 25 °C can reduce the life time by an order of magnitude [177]. Therefore a good estimation of amplifier performance cannot be performed without reliable calculations of transistor temperatures. For this a proper thermal model is a necessity.

6.2.5 Interpretation of WIN reliability data

In the reliability report of the PP25-20 process, WIN provides the obtained life times of three test transistor of $2 \times 75 \mu\text{m}$ for specified backside temperatures T_{back} [178], see Table 6.2. These backside temperatures are translated to channel temperatures T_{ch} by using the results of thermal simulations performed in COMSOL [71]. According to the reliability reports, the lifetime tests were carried out at a drain voltage of 8 V and a drain current of 26 mA, resulting in a dissipation of 208 mW. In the COMSOL simulation, each channel is defined as a volume of $75 \times 0.5 \times 0.25 \mu\text{m}^3$ ($W \times L \times H$) = $9.375 \mu\text{m}^3$ which yields a power density of $11.09 \text{ mW}/\mu\text{m}^3$ or $11.09 \text{e}15 \text{ W}/\text{m}^3$. Note that the defined channel length of $0.5 \mu\text{m}$ is twice the transistor gate length of $0.25 \mu\text{m}$, due fact that the active channel spreads out toward the drain side.

Table 6.2: Time of first failure from WIN PP25-20 reliability data.

T_{back}	T_{ch} (COMSOL)	Lot 1	Lot 2	Lot 3
150 °C	265 °C	239 h	278 h	156 h
165 °C	285 °C	69 h	119 h	85 h
180 °C	305 °C	47 h	39 h	26 h

The activation energies are determined from the test results according to:

$$E_a = \frac{k \cdot \ln(AF)}{T_1^{-1} - T_2^{-1}}, \quad (6.10)$$

where T_1 and T_2 are two of the obtained temperature points and the acceleration factor $AF = \text{MTTF}|_{T_1} / \text{MTTF}|_{T_2}$ is the corresponding acceleration factor determined from the fitting, see Figure 6.6 . The extracted activation energy $E_a = 1.19$ eV.

Figure 6.6: Extrapolation of WIN reliability data.

6.2.6 Thermal model

The thermal model used in this work is divided into several parts, see Figure 6.7. The first two parts, represented by the series connection of R_{th1} and R_{th2} , cover the thermal path from the base i.e. the thermal reference to the backside of the MMIC. These parts can contain packaging, PCB, die attach, etc. and is usually constant versus temperature. The upper elements, $R_{th,x}$, cover the thermal path from the transistor channels to the backside of the MMIC. Each amplifier stage is treated individually, which results in the thermal resistance values $R_{th3,1}$ to $R_{th3,n}$, where n is the number of stages. Each thermal resistance $R_{th,x}$ represents the weighted average of the thermal resistances of the individual transistors in the stage. In the model thermal coupling between the stages exists via the substrate on which the MMIC is mounted, i.e. the stages are thermally isolated if the MMIC backside temperature is uniform. As the thermal properties of semiconductor materials such as GaAs, GaN and Silicon Germanium (SiGe) are temperature dependent, the values for $R_{th3,x}$ are temperature dependent as well. In literature

several models for thermal conductivity κ of GaAs versus temperature can be found. For the fitting of the thermal conductivity for temperatures in the range from 300 to 400 K the following equation is often used:

$$\kappa(T) = aT^b, \quad (6.11)$$

where T is the temperature in Kelvin. A commonly used sets of fitting parameters as found in literature [173] are $a=56873$ and $b=-1.23$. These parameter values are used in the remainder of this chapter.

Figure 6.7: Thermal model.

The thermal resistance of the path from transistor channel to MMIC backside can be estimated based on an analytical method proposed by Darwish et.al. [173]. With this method the thermal resistance of an infinite array of gate fingers is calculated based on unit gate width, gate length, gate-to-gate spacing and substrate height. A more detailed and accurate estimation is obtained by using a thermal FEM solver [71]. The drawback is the significantly larger simulation time which limits the feasibility for this method to be performed inside an iterative loop.

6.2.7 Practical gate biasing

In section 3.8.2, general requirements for the gate bias voltages of the transistors in the stack are discussed. In the HPA these bias voltages need to be supplied to each transistor. Figure 6.8 illustrates how the supply of gate bias voltages is implemented for a single Stacked-FET stage containing S stacks. The gate bias voltages for the CS transistors are obtained from a single active gate bias circuit GB1 that compensates for threshold voltage and supply voltage variations [153]. The DCG transistors in the stacks 1 to S all have an individual gate bias

circuit GB2.1 to GB2.S and GB3.1 to GB3.S. This separates the gates of these DCG transistors, thereby reducing the number of RF loops and hence the number of possible instabilities.

Figure 6.8: Gate biasing of transistors in Stacked-FET stage.

Figure 6.9: Gate bias circuit for DCG transistors.

The bias circuits of the DCG gates are supplied with the drain supply voltage V_{dd} of the amplifier, see Figure 6.9. As a result the gate bias voltages are directly related to the stack supply voltage which prevents the DCG FETs from being exposed to positive gate-to-drain voltages during start-up. The start-up behaviour is analysed through a transient simulation with the gates of the DCG stages in the HPA connected to the DCG gate bias circuit. The simulated output voltages of the DCG gate bias circuit are shown in Figure 6.10. The supply voltage V_{dd} ramps from 0 V to 24 V in 100 ns, starting at $t=0$ ns. The output voltages follow with a delay of approximately 20 ns.

Figure 6.10: Start-up of DCG gate bias circuit.

The voltages on the DCG FETs in the stack, observed in the simulation, are given in Figure 6.11. It can be seen that the gate-to-source voltages settle after 30 ns and remain stable during the remainder of the start-up. The drain-to-gate voltage never exceeds the critical value of in this case approximately 20 V.

Figure 6.11: Voltages on transistors during start-up of DCG gate bias circuit.

6.3 HPA 1: 20 W, Single-stage amplifier

The first amplifier is a single stage amplifier with an output power level of approximately 20 W. Due to its relatively simple topology, it gives a large amount of insight in a Stacked-FET HPA that delivers state-of-the-art output power.

6.3.1 CS transistor performance

To determine the architecture of the first amplifier, a number of load-pull measurements is performed on CS transistors with different sizes. Based on the measured characteristics an estimation of the performance of several HPA architectures is carried out. One optimum architecture is selected, implemented and measured.

The load-pull measurements are performed on transistors with various values for NGF and UGW. A summary of the results from these measurements is listed in Table 6.3. Per transistor geometry the average results from the measurements on three samples are given. The output power density as a function of the total gate width shows a decreasing trend that can be approximated with a linear fit, see Figure 6.12.

Table 6.3: CS transistor performance from load-pull measurement at $I_g=0.1$ mA/finger, $f=3$ GHz, $V_d=8$ V, $I_{dq}=114$ mA/mm, $\delta=10$ %, $PW=50$ μ s, $T=25$ °C.

NGF	UGW μ m	P_{out} (dBm)	P_{dens} (W/mm)	P_{diss} (W/mm)	G_P (dB)	I_d (mA)
8	150	29.94	0.82	0,534	23.5	203
8	300	32.57	0.75	0,533	24.9	384
10	300	32.99	0.66	0,513	26.8	430
12	300	33.49	0.62	0,398	27.5	457
8	500	33.78	0.60	0,400	23.8	497
12	500	35.07	0.54	0,321	23.7	641

Figure 6.12: Measured output power density of single CS transistors versus total gate width at $I_g=0.1$ mA/finger, $f=3$ GHz, $V_d=8$ V, $I_{dq}=114$ mA/mm, $\delta=10$ %, $PW=50$ μ s, $T=25$ $^{\circ}$ C.

The maximum finger width is determined by the operating frequency [150]. The unit gate width mainly affects the transistor gain due to attenuation and phase shift in the gate line. Therefore a larger gate width will reduce the amplifier gain and PAE. This mechanism also holds for the number of gate fingers. The latter, in combination with the channel-to-channel pitch, determines the physical size of a single transistor. The minimum channel-to-channel pitch is limited by the maximum temperature, as the thermal coupling and therefore the temperature increases with reduced distance. The predicted effect of gate pitch is analysed in a COMSOL analysis on a 8×350 μ m transistor. The simulations are performed for a dissipation of 0.6 W/mm or 1.7 W per transistor which is just above the absolute maximum dissipation according to load-pull measurements, see Figure 6.13.

According to Eqn. (6.9), the maximum channel temperature for an often required MTTF of 10 years is 162° C. This mean that the minimum channel spacing is approximately 20 μ m.

Figure 6.13: Simulated maximum channel temperature of a single transistor versus channel spacing for dissipation of 1.7 W, $T_{back} = 80^{\circ}\text{C}$.

6.3.2 Single-stage amplifier architecture

The HPA output power for different combinations of Stacked-FETs is calculated based on the measured output power densities in Figure 6.12. For this estimation an output matching loss of 0.6 dB is assumed.

The result for Stacked-FETs containing three transistors per stack is shown in Figure 6.14 and the output power for different combinations of Stacked-FETs containing four transistors is shown in Figure 6.15.

The target output power specification of 20 W is met with any of the following combinations of Stacked-FETs in parallel:

- Four stacks of $3 \times 8 \times 350 \mu\text{m}$
- Eight stacks of $3 \times 8 \times 150 \mu\text{m}$
- Four stacks of $4 \times 8 \times 250 \mu\text{m}$
- Eight stacks of $4 \times 8 \times 110 \mu\text{m}$

For solutions with either three or four transistors in the Stacked-FET, the required output power level can be achieved with four stacks in parallel, which is preferred over solutions with eight stacks due the smaller chip size. The choice for a stack of three transistor is made since the estimated stacking losses will be lower, resulting in a higher PAE, as was shown in section 3.8.4. This mean that the selected architecture of the HPA uses four Stacked-FETs of three $8 \times 350 \mu\text{m}$ transistors each. Details on the design of this stack can be found in section 3.6. In the next section the stabilisation of this stack is described.

Figure 6.14: Estimated output power versus UGW for parallel connection of two, four and eight stacks of *three* transistors with eight gate fingers, $f=3$ GHz, $I_g=0.1$ mA/finger, $V_d=8$ V.

Figure 6.15: Estimated output power versus UGW for parallel connection of two, four and eight stacks of *four* transistors with eight gate fingers, $f=3$ GHz, $I_g=0.1$ mA/finger, $V_d=8$ V.

6.3.3 Stability of the Stacked-FET

The stability of the $3 \times 8 \times 350 \mu\text{m}$ Stacked-FET is analysed after the design of the stack and the constitutive transistors are stabilised by the use of stabilisation resistors. Unconditional stability of the CS-transistor is obtained by the use of a parallel RC-network in series with the gate, as described in section 5.2.1. For the stabilisation of each DCG transistor, the effect of resistance R_a in series with the external voltage balancing capacitor C_{gX} (see Figure 5.6) on the stability parameter μ is analysed.

Figure 6.16 shows the stability parameter μ of the lowest DCG transistor the stack as a function of frequency and resistor value R_a . As argued in chapter 5, this lowest DCG is the most critical transistor with respect to stability. The cutting plane $\mu = 1$ is included, this plane defines the required resistor value for unconditional stability versus frequency which is given in Figure 6.17.

Figure 6.16: Stability parameter μ of lowest DCG transistor versus frequency and stability resistance R_a .

From the results it is found that the required value for R_a increases for low frequencies and unconditional stability of the stack over the entire frequency range down to DC cannot be obtained with this method. To choose a proper value for R_a the RF output power and PAE of the total stack are given in Figure 6.18 versus the stability resistance values in the DCG transistors. For resistance values above 10Ω the reduction in output power and PAE starts to increase. For this reason the resistance value is limited to 10Ω , which means that unconditional stability is only obtained for frequencies above 20 GHz . For lower frequencies,

stability is verified in the overall HPA analysis and for the analysed cases, no instabilities were found.

Figure 6.17: Required R_a for $\mu=1$ of first DCG transistor.

Figure 6.18: RF-performance $3 \times 8 \times 350 \mu\text{m}$ stack as a function of DCG stability resistance R_a , $f=3 \text{ GHz}$, $V_{dd}=24 \text{ V}$, $V_{gs}=-1 \text{ V}$.

6.3.4 Thermal analysis

A COMSOL [71] simulation is performed on the active parts of the HPA. For this simulation a copper base plate was considered, the thermal setup is given in Figure 6.19. The thermal properties of the layers in the thermal stack are given in Table 6.4, where for the thermal conductivity the equation $\kappa_{GaAs}(T) = 56,873 \cdot T^{-1.23}$ is used, as was discussed in section 6.2.6.

Figure 6.19: Setup for thermal HPA simulations.

Table 6.4: Thermal properties of materials.

	Thickness (μm)	Thermal conductivity ($W/m \cdot K$)	Heat capacity ($J/kg \cdot K$)	Density (kg/m^3)
GaAs	100	$\kappa_{GaAs}(T)$	350	5361
Die attach	20	20	235	4900
Copper	200	380	385	7800

The simulated step response is shown in Figure 6.20. The total dissipation in the transistors is 30 W and the copper backside temperature is set to 80 °C. The maximum temperatures of the topside of the copper, backside of the MMIC and active channels are given versus time. It can be seen that the rise time is approximately 1 ms. The 10-year lifetime (162 °C) is met, if the maximum pulse time is below 200 μs . This means that the amplifier can operate in pulsed mode, but Continuous Wave (CW) operation, with the current thermal setup, is not feasible.

Figure 6.20: Result of thermal simulation at maximum output power, copper backside temperature is 80 °C.

6.3.5 Matching networks

Since the first HPA is a single stage amplifier, it contains an input and output matching network only. These matching networks are not fundamentally different than those for CS based amplifiers. The impedance ratios for these matching networks, however, are lower than for CS amplifiers, as was discussed in section 6.2.3. This results in a higher obtainable bandwidth or lower loss.

Output matching network

The OMN of the amplifier should perform the following functions:

- Present the optimum impedance to the Stacked-FETs,
- Supply the drain voltage and current to the Stacked-FETs,
- Provide DC decoupling between the Stacked-FETs and amplifier output.

The equivalent schematic of the OMN is shown in Figure 6.21. It basically consists of three LC-sections with an additional shunt inductor to the Vdd connection for drain biasing. This bias inductor presents the imaginary part of the required load admittance. The Vdd connection is decoupled with a shunt capacitor that is designed to provide a low impedance to ground in the frequency band of interest.

Figure 6.21: Schematic of output matching network.

The layout of the OMN is depicted in Figure 6.22. The inductors from Figure 6.21 can be identified as transmission lines. Most capacitors are implemented as a series connection of two or more MIM capacitors to support the high voltage swings on these components. The inputs in2 and in3 are connected via a resistor to suppress odd-mode oscillations.

Figure 6.22: Layout of output matching network.

The OMN is analysed in a single Momentum [123] simulation. The result of this analysis is shown in Figure 6.23, where the simulated matching to the required admittance at the inputs of the OMN is given together with the total loss of the network. The matching levels, determined according to Eqn. (2.9), are shown for the four individual inputs of the OMN. Within the target frequency band, the simulated matching is better than -18 dB, which is close to the goal of -20 dB as argued in section 3.6.3.

Figure 6.23: Simulated matching and loss of OMN.

Input matching network

The requirements for the IMN of the amplifier are:

- Transform the input impedance of the Stacked-FETs, loaded with the OMN and terminated in 50Ω , to the required amplifier input impedance of 50Ω .
- Supply the CS gate voltage and currents to the Stacked-FETs.
- Provide DC decoupling between the Stacked-FETs and amplifier input.

The equivalent schematic of the IMN is shown in Figure 6.24. The RC stability networks are included as a part of the IMN. The gate bias voltage is supplied to the gates of CS the transistor via the shunt inductor to the V_g connection, which also compensates the imaginary part of the input impedance of the stabilised transistors. The impedance matching step to the required 50Ω HPA input impedance is performed by the LC-section.

Figure 6.24: Schematic of input matching network.

The layout of the IMN is shown in Figure 6.25. The stability networks for the CS transistors are visible at the output ports of the matching network. The blocking capacitor at the input is implemented as a series connection of two MIM-capacitors for better robustness against Electro Static Discharge (ESD) events.

Figure 6.25: Layout of input matching network.

6.3.6 Simulations

The simulated output power of the HPA is shown in Figure 6.26. The frequency sweeps are given for three levels of source power, from 23 to 25 dBm. At a source power level of 25 dBm, the HPA has reached saturation as can be seen from the power sweeps. The output power at the maximum source power varies between 42.5 dBm and 43.3 dBm, which implies that the Large Signal (LS) gain is between 18.5 dB and 19.3 dB.

Figure 6.26: Simulated output power of single stage HPA.

The simulated PAE of the HPA is shown in Figure 6.27. Within the target operating frequency band from 2.9 GHz to 3.4 GHz, the simulated PAE is higher than 35 %.

Figure 6.27: Simulated PAE of single stage HPA.

The simulated drain voltage waveforms of the three FETs in one of the stacks in the HPA are shown in Figure 6.28. The peak voltage levels at the three drains

are 15 V, 30 V and 45 V which demonstrates the voltage scaling within the stack.

Figure 6.28: Drain voltage waveforms, $f=3$ GHz, $P_{avs}=24$ dBm.

The simulated drain current waveforms of the three FETs in one of the stacks in the HPA are shown in Figure 6.29. It is seen that these waveforms have a similar, overdriven class-B shape. The differences between the individual waveforms are due to small variations in fundamental and harmonics loads of the transistors in the stack.

Figure 6.29: Drain current waveforms, $f=3$ GHz, $P_{avs}=24$ dBm.

6.3.7 Measured results

The amplifier was manufactured and tested [179], a chip photograph of the amplifier is shown in 6.30. The chip dimension are 3.95×2.35 mm², including pads and scribe street. The measurements are performed on a device soldered on

a CuMo carrier.

Figure 6.30: Chip photograph of the 20 W S-band stacked FET amplifier.

The measured pulsed output power of the amplifier is shown in Figure 6.31 together with the simulated data. The results versus frequency are given at a source power $P_{avs}=24$ dBm, the power sweeps are shown at a frequency $f=3.1$ GHz. A measured output power level in excess of 42.5 dBm is seen in the frequency band from 2.9 to 3.6 GHz. Inside this band, the fit with the simulated power is within ± 0.1 dB. The measured bandwidth is ± 100 MHz larger than simulated.

Figure 6.31: Measured and simulated output power of 20 W S-band amplifier on carrier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $PW=10\mu s$, $\delta=10$ %, $P_{avs}=25$ dBm (left) and $f=3.1$ GHz (right).

Figure 6.32 shows the measured PAE of the amplifier together with the simulated data. Within the frequency band from 2.7 to 3.6 GHz the measured PAE is more than 40 %, which is approximately 8 %-point higher than simulated. This is explained by the inaccuracy of the drain current simulation, as will be shown later.

Figure 6.32: Measured PAE of 20 W S-band amplifier on carrier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $PW=10\mu s$, $\delta=10$ %, $P_{avs}=25$ dBm (left) and $f=3.1$ GHz (right).

The measured and simulated large-signal gain of the amplifier are shown in Figure 6.33. The fit between the measurement and simulation is within 0.1 dB in the saturation region. In the soft compression region the simulation error is approximately 1 dB.

Figure 6.33: Measured large-signal gain of 20 W S-band amplifier on carrier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $PW=10\mu s$, $\delta=10$ %, $P_{avs}=25$ dBm (left) and $f=3.1$ GHz (right)

The measured drain current of the amplifier is shown in Figure 6.34 together with the simulated data. The measured drain current is approximately 10 %

lower than simulated. This explains the observed difference in PAE.

Figure 6.34: Measured drain current of 20 W S-band amplifier on carrier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $PW=10\mu s$, $\delta=10$ %, $P_{avs}=25$ dBm (left) and $f=3.1$ GHz (right).

6.4 HPA 2: 30 W, two-stage amplifier

After the successful demonstration of the single stage 20-W amplifier, a second development was initiated. The aim of the development of this second amplifier was:

- To increase the output power level by approximately 3 dB.
- To design a two-stage Stacked-FET amplifier. The increased gain makes this amplifier more suitable for application in systems with limited drive power.
- To demonstrate a Stacked-FET power amplifier suitable for packaging in a plastic QFN package. For this the dissipation of the amplifier should be limited.

In this section the design steps, simulation results and measured result of this amplifier are discussed.

6.4.1 Two-stage HPA architecture

The increase in output power of 3 dB, with respect to the first amplifier, means that the total transistor area in the output stage needs to be enlarged by a factor of two. As argued in the previous section, the chosen number of transistors per stack is three. This means that the increased output stage can be obtained by enlarging the constitutive transistors in the stack, by increasing the number of Stacked-FETs in parallel or a combination of the two. As was shown in figure 6.12,

the transistor power density decreases with gate width therefore the required doubling of output power cannot be obtained from increasing the transistor size only. For this reason an output stage with eight Stacked-FETs in parallel is chosen.

The power dissipation in the input stage of the two-stage HPA, reduces the overall PAE. This means that in order to maintain or increase the overall PAE, the PAE of the output stage should be increased. This is achieved by selecting a transistor load admittance for higher efficiency and lower output power. In order to still achieve the HPA output power goal, the unit gate width of the transistors is increased from $350\text{ }\mu\text{m}$ to $390\text{ }\mu\text{m}$. The resulting architecture of the HPA is shown in Figure 6.35. The input stage consists of a single $3\times 8\times 260\text{ }\mu\text{m}$ stack. The ISMN between the two stages is expected to be the limiting factor in terms of achievable bandwidth, as argued in section 6.2.3.

Figure 6.35: Architecture of 30 W HPA.

The increased transistor size degrades the stability of the stack. Besides, the addition of an input stage increases the possible instabilities of the HPA. For these reasons, during the design of this amplifier, the stability considerations were an integral part of the design and optimisation of the Stacked-FETs. The incorporation of stability considerations as described in chapter 5 are discussed in detail in the next section. One of the degrees of freedom with respect to the design of a stable stack is the internal transistor load admittance. For the current amplifier the selected transistor load is moved toward an efficiency optimum, which results in a load impedance with a larger real part. This increased real part is beneficial for the stack stability as indicated in Figure 6.36, which shows the stability parameter μ' of a Stacked-FET versus the real part of the load impedance of the internal transistors in the stack. The internal load resistance for maximal output power for these transistors is $10\text{ }\Omega$. It is seen that for load resistance values between 0 and $10\text{ }\Omega$, the parameter μ' can be as low as is -1 in the frequency range from 1 GHz to 5 GHz. This indicates instabilities that cannot be

suppressed without a significant reduction of RF-performance. Choosing a larger internal load resistance, which corresponds to optimisation for PAE, reduces these instabilities.

Figure 6.36: Stability parameter μ' of a $3 \times 8 \times 350 \mu\text{m}$ Stacked-FET as a function of frequency and real part of the internal transistor load impedance.

6.4.2 Stack design including stability constraints

The stability considerations start with the analysis of the K -factor of a single $8 \times 390 \mu\text{m}$ transistor in CS configuration, which is shown in Figure 6.37 for different levels of drive power. It is seen that initially the K -factor reduces with drive power, eventually an increase is visible as the device is driven into saturation. The worst case situation is just before this saturation region, at a source power level of 19 dBm.

The required value of series resistance for a target K -factor value of 1 was calculated using Eqn. (5.5). An RC-network is dimensioned such that within the S-band frequency range around 3 GHz, the required and applied resistance values match very well whilst outside this band, the applied value is larger than required. This can be seen from Figure 6.38 where the required and applied effective series resistance of the parallel RC-network are shown. By using this RC-network, the K -factor requirement within the band is met whilst outside of the band, some additional stability margin is present.

The optimum load for the $8 \times 390 \mu\text{m}$ transistor at a frequency of 3.1 GHz is obtained from a linear scaling of the optimum load impedance of the $8 \times 350 \mu\text{m}$. The obtained load is $Z_L = 14.3 + j5.9 \Omega$ or $\Gamma_L = -0.541 + j0.142$. The results from cold FET measurements at $V_d=0$ and $V_g=0$ on the $8 \times 350 \mu\text{m}$ are used to extract

Figure 6.37: Stability factor K of $8 \times 390 \mu\text{m}$ CS transistor for different levels of drive power, $V_d = 8 \text{ V}$, $V_{gs} = -1 \text{ V}$.

Figure 6.38: Required and applied effective series resistance for CS $8 \times 390 \mu\text{m}$ transistor.

the extrinsic component values, which are scaled to values for the $8 \times 390 \mu\text{m}$ transistor using the EEHEMT1 [180] scaling rules, see Table 6.5.

Table 6.5: Extrinsic component values, $8 \times 390 \mu\text{m}$ FET.

C_{pd}	C_{pg}	L_g	L_d	L_s	R_g	R_d	R_s
(fF)	(fF)	(pH)	(pH)	(pH)	(Ω)	(Ω)	(Ω)
45.4	32.2	38.1	35.5	0.83	2.5	0.33	0.14

For the $8 \times 390 \mu\text{m}$ transistor, an equivalent two-port scattering matrix is determined under large-signal excitation with $f_{LS} = 3.1 \text{ GHz}$ and a small-signal

test tone with $f_{SS}=3.0$ GHz. This two-port matrix is then de-embedded up to the reference plane of the intrinsic transistor [144] using the component values from Table 6.5. The equivalent model parameter values are extracted from this de-embedded result. The extracted parameter values are shown in Figure 6.39. The power dependency is mainly observed in the gate-to-source capacitance and the transconductance. The parameter values are read at a source power of 20 dBm. From Figure 6.37 it was found that this power level is in the worst case stability region, which implies that stability analysis using these figures is valid for the worst case situation. The obtained parameter values are: $C_{ds}=0.98$ pF, $C_{gs}=3.32$ pF, $C_{gd}=0.32$ pF and $g_m=0.38$ S. With these component values, the brute-force method described in section 5.3.2 is initiated.

Figure 6.39: Model parameters at $f_{SS}=3.0$ GHz versus source power, for $f_{LS}=3.1$ GHz, $\Gamma_{LS} = -0.541 + j0.142$, $V_d=8$ V, $V_g=-1$ V, $T=25$ °C.

The external load impedance of the 8×390 μm FET that yields the highest PAE for this transistor, was translated to the load of the intrinsic transistor and this load is used as the centre of the search area for stable solutions. The real and imaginary parts are independently swept together with the values for the stabilising resistors in series with the voltage and current balancing capacitors. For each load setting the values for the balancing capacitors were determined using (3.17) and (3.28). Each combination of balancing capacitors and series resistors that was found to be unconditionally stable was analysed in Keysight ADS [181].

The identified stable solutions are summarised in Figure 6.40. It is seen that there is a significant variation in RF-performance. Several groups are visible due the variation in transistors load that are either more optimal for output power or PAE. Within these groups variations are present due to the different values of stability resistors. The selected solution is indicated in the figure. At this point the PAE is less than 1 %-point lower than the maximum obtained value while the

output power is 0.4 dB higher than the output power at the maximum PAE point.

Figure 6.40: Stable stack options, $3\text{x}8\text{x}390\text{ }\mu\text{m}$.

Following section 5.3.1, the stability parameters $M1$ and $M2$ of the selected solution for the two drain nodes ($d1$ and $d2$ of the CS and first DCG FET, respectively) are shown in Figure 6.41. It is seen that both $M2_{d1}$ and $M2_{d2}$ are positive over the entire frequency range. $M1_{d1}$ and $M1_{d2}$ are slightly smaller than zero for frequencies above 4 GHz, which means that the Stacked-FET is not unconditionally stable. Load reflection coefficients very close to 1 can map into the unstable regions of the transistors. Due to the loss in the matching networks, however, such large reflection coefficients are not expected at the output of the stacked-FETs which means that practically speaking the device is stable for all expected loads. This is further analysed using the internal stability analysis tools that were described in section 2.4.3, in particular though the STAN software tool, over the entire operating power range; no instabilities were found.

Figure 6.41: Stability parameters $M2$ and $M1$ at internal nodes $d1$ and $d2$.

The designed $3 \times 8 \times 390 \mu\text{m}$ Stacked-FET is the basis for the further design of the 30 W HPA. The thermal behaviour of eight of these stacks in parallel is analysed in the next section.

6.4.3 Thermal analysis

A thermal analysis is performed on the layout of the 30 W HPA. During this analysis the effects of packaging are taken into account by including the copper pedestal of the QFN. The analysis is carried out in two steps. In the first place the reference temperature, defined at the backside of the package, is translated to the backside temperature of the chip. This is done using the average dissipation over time, taking into account the pulse profile. At this point, the temperature is assumed to be uniform and constant over time. During the second step, the channel temperatures on the chip are calculated using a single step excitation. From these results the maximum temperature for any pulse length can be determined.

The temperature profile of the chip backside for a duty cycle $\delta=10\%$ is given in Figure 6.42. For this simulation a reference temperature of 45°C is defined at the backside of the package. The observed chip backside temperature for this scenario is 94°C .

Figure 6.42: Temperature profile of chip backside 30 W HPA, $PW=10 \mu s$, $\delta=10 \%$.

The thermal step response of the MMIC from the chip backside temperature of 94°C is shown in Figure 6.43. For this simulation, the highest dissipation levels extracted from the HB simulations on the HPA are used. After $100 \mu s$ the maximum channel temperature is 139°C , which is significantly lower than for the first HPA.

Figure 6.43: Thermal step response 30 W HPA, $PW=10\ \mu\text{s}$, $\delta=10\ \%$.

6.4.4 Matching networks

The two stage design contains three matching network: the OMN, the ISMN and the IMN. In this section the topologies, layouts and EM-simulation results of these matching network are given. As discussed in section 6.2.3, the ISMN is expected to limit the overall achievable bandwidth due to the large matching ratio for this network.

Output matching network

The schematic of the OMN is shown in Figure 6.44. The drain bias of the second stage is applied via a shunt inductor to V_{dd2} , which also provides the imaginary part of the required load admittance. The real part of the impedance is matched by three LC-sections. The series capacitor at the output is for DC blocking only.

Figure 6.44: Schematic of output matching network of 30 W HPA.

The layout of the OMN is shown in Figure 6.45. All inductors are implemented as micro-strip lines. Due to the inherent stability of the stacks in the output stage, odd-mode resistors are not required. The shunt capacitances near the output are implemented as series connections of three capacitors to withstand the large DC+RF voltage swing at these points.

Figure 6.45: Layout of output matching network of 30 W HPA.

The OMN was analysed entirely in a single Momentum [123] simulation. The simulated matching to the required impedance and the loss of the OMN are given in 6.46. The matching levels, determined according to Eqn. (2.9), are shown for the eight individual inputs of the OMN. Within the frequency band of interest, the matching level is better than the desired -20 dB, with a loss below 0.7 dB.

Figure 6.46: Simulated matching and loss of OMN.

Interstage matching network

The schematic of the ISMN is shown in Figure 6.47. The RC stability networks of the CS transistors in the output stage are a part of this matching network. As explained in section 6.2.2, the matching requirements for the ISMN are more difficult to meet than for the OMN and IMN. For this reason an additional series resistor is included in series with the RC stability network, to provide a better matching level at the expense of a higher loss.

Figure 6.47: Schematic of interstage matching network of 30 W HPA.

The layout of the ISMN is shown in Figure 6.48. The gate bias of the output

stage is supplied via a lumped inductor, which is possible due to the low current levels in this path.

Figure 6.48: Layout of interstage matching network of 30 W HPA.

A single Momentum simulation was performed on the entire ISMN. The simulated matching to the required impedance and the loss of the ISMN are given in Figure 6.49. At the low side of the frequency band the matching level is -7 dB, which illustrates the matching difficulty. The loss of the ISMN is significantly higher than the loss of the OMN. This is due to the presence of the stability

network and the additional series resistor.

Figure 6.49: Simulated matching and loss of ISMN

Input matching network

The schematic of the IMN is shown in Figure 6.50, the layout is shown in Figure 6.51. Also here the stability network is included in the matching network. Due to the use of the lumped inductors, a compact network is obtained.

Figure 6.50: Schematic of input matching network of 30 W HPA.

Figure 6.51: Input matching network of 30 W HPA.

6.4.5 Simulations

The simulated output power of the HPA is shown in Figure 6.52 at an MMIC backside temperature of 25°C. It can be seen that at a frequency of 3 GHz, the HPA is in saturation for source powers above 13 dBm. At a frequency of 3.3 GHz, a source power of 16 dBm is required to reach the saturation region.

Figure 6.52: Simulated output power, $V_{dd}=24$ V, $T_{MMIC}=25$ °C.

The simulated PAE of the HPA is shown in Figure 6.53. For power points above 16 dBm, no variation in PAE is observed, which implies that the optimum window with respect to PAE starts at this source power level.

Figure 6.53: Simulated PAE, $V_{dd}=24$ V, $T_{MMIC}=25$ °C.

The simulated drain voltage waveforms in the HPA are shown in Figure 6.54. The peak voltage levels for the three FETs are 15, 30 and 45 V which demonstrate voltage scaling within the stack.

In comparison to the simulated voltage waveforms of HPA 1, which were shown in Figure 6.28, these voltages waves are more squared. This is the indirect results of the optimisation for efficiency.

Figure 6.54: Drain voltage waveforms, $V_{dd}=24$ V, $f=3$ GHz, $P_{avs}=18$ dBm, $T_{MMIC}=25$ °C.

The simulated drain current waveforms in the HPA are shown in Figure 6.55. It is seen that the currents for the three FETs are almost equal, demonstrating the successful balancing of the stack. These waveforms show a large similarity to the current waveforms from in HPA 1, that were shown in Figure 6.29.

Figure 6.55: Drain current waveforms, $V_{dd}=24$ V, $f=3$ GHz, $P_{avs}=18$ dBm, $T_{MMIC}=25$ °C.

6.4.6 Measured results

The chip photograph of the amplifier is shown in 6.56. The chip dimensions are 4.5×4.5 mm², including pads and scribe streets. The first stage consists of a single stack of 3 transistors. To save chip space in the x-direction, the transistors in the stack were placed vertically, i.e. in the y-direction.

Figure 6.56: Chip photograph of 30 W S-band Stacked-FET amplifier.

The results are given as measured on the bare chips, mounted on a CuMo carrier, as well as from the measurements on the QFN packages. The pulsed output power of the amplifier is shown in Figure 6.57. The red traces show the results of the on-wafer measurements, the blue traces give the results from the QFN packages. The first plot shows the results versus frequency, an output power level in excess of 44 dBm is seen in the frequency band from 2.6 GHz to 3.5 GHz. The simulation results are included in the figure, simulation and measurement match within ± 1 dB over the targeted frequency band from 2.9 GHz to 3.4 GHz. The second plot shows the output power at a frequency of 3 GHz versus source power. It can be seen that at a source power of 10 dBm, the measured output power has already reached saturation, while the simulated output power saturates at a source power of 13 dBm.

Figure 6.57: Output power of 30 W S-band amplifier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $P_{avs}=15$ dBm, $PW=10$ μ s, $\delta=10$ %.

Figure 6.58 shows the measured PAE of the amplifier. Again the red traces show the results of the on-carrier measurements, the blue traces give the results from the QFN packages. Within the frequency band from 2.6 to 3.5 GHz the PAE is more than 40 %. The simulation result is included as the black trace. It is seen that the measured efficiency is approximately 7 %-point higher than simulated. This is due to the drain current prediction of the model, which is too high as is shown later.

Figure 6.58: PAE of 30 W S-band amplifier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $P_{avs}=15$ dBm, $PW=10$ μ s, $\delta=10$ %.

The large-signal gain of the amplifier is shown in Figure 6.59. In the saturation region the gain is well predicted, however, in the soft compression region the simulated gain is too low. This results in the difference in compression behaviour as was observed from the output power and PAE results.

Figure 6.59: Measured large-signal gain of 30 W S-band amplifier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $P_{avs}=15$ dBm, $PW=10$ μ s, $\delta=10$ %.

The large-signal drain current from both the on-carrier and the QFN measurements are shown in Figure 6.60 together with the simulated results. It is seen that the measured current is lower than the simulated current. This was traced back to inaccurate prediction of the large-signal current of the non-linear transistor model used in the design. This higher current partly explains the lower PAE that is seen in Figure 6.58.

Figure 6.60: Drain current of 30 W S-band amplifier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $P_{avs}=15$ dBm, $PW=10$ μ s, $\delta=10$ %.

6.5 Conclusion

In this chapter the design procedure for Stacked-FET power amplifiers is developed. The considerations with respect to amplifier architecture, as well as the practical implementation is described. The feasibility of Stacked-FET amplifiers is demonstrated by the design of two, well-considered implementations. A comparison between the measured output and PAE of the two implemented HPAs is shown in Figure 6.61.

The first amplifier is designed according to the strategy described in Chapter 3. This single stage amplifier has an output power of 20 W with an associated PAE of more than 40 %. The second amplifier has an output power of 30 W with an associated PAE of more than 40 % as well. During the design of this amplifier the stability considerations were included as an integral part of the design procedure, such as described in Chapter 5.

The results presented in this chapter show a good fit between measurements and simulation while the RF-performance of the devices forms the state of the art. This implies that the design and simulation approaches are valid. During the measurements of the amplifier no significant stability problems were observed and no evidence is found that the amplifiers suffer from oscillations. From this it is concluded that the described stabilising strategy results in stable Stacked-FETs which are building blocks for power amplifiers with excellent RF characteristic.

Figure 6.61: Comparison of HPA 1 and HPA.

CHAPTER 7

Amplifier yield and screening

7.1 Introduction

The power amplifiers and Stacked-FET test structures described in the previous chapter are manufactured in a mature, well controlled process. The processing yield of this process is usually high, however, variations on electrical performance due to the variation of processing parameters are inevitable. In this chapter the effect of processing variations and imperfections are analysed and methods are discussed to discriminate between good and non-good devices.

The amplifiers and test structures are processed on 6-inch wafers. The on-wafer measurements on the power amplifiers that were reported in the previous chapter have been obtained from one quarter of this wafer, this quarter is shown in Figure 7.1. This quarter wafer contains approximately 30 similar reticles, each containing one copy of the single-stage and two copies of the two-stage HPA. A second quarter of this wafer has been diced for mounting and characterisation on carriers. The next sections give details on the expected yield with respect to electrical performance related to processing variations.

The manufacturing of radar front-ends is preferably performed with components that are fully tested and known to be functional. This decreases the chances of instant failure or rapid degradation of the system. Complete testing of the RF-performance of the individual MMICs, however, is not always possible due to technical, infrastructural or financial limitations. A good alternative is the screening of several DC parameters that are relevant for a reliable operation. Commonly used parameters for this DC-screening are the pinch-off voltage and breakdown voltage of the transistors. To measure these parameters on all transistors, access is required to the gate, drain and source terminals of these transistors. From the chip photograph of the Stacked-FET amplifiers in Figure 6.30 and Figure 6.56 it can be seen that not all transistors terminals are directly

Figure 7.1: Quarter WIN-PP25-20 wafer containing the single-stage and two-stage Stacked-FET power amplifiers.

accessible via DC pads and the inclusion of extra pads will result in a significantly larger layout. This is typical for Stacked-FET amplifiers and the goal therefore is to measure the DC behaviour without the need for extra DC pads. In this chapter methods are developed to support this goal.

7.2 Process variations

The first part of this section gives the characteristics of the wafers from which the previously shown HPA and test-structure results were obtained. In the second part, the effect of process variation of RF-performance of the single-stage Stacked-FET HPA is analysed.

7.2.1 Process control monitoring

To monitor the quality of each specific wafer that is processed, Process Control Monitoring (PCM) structures are included on each tile, to measure technology specific parameters. In addition to the active transistor parameters, the PCMs

contain passive element parameters including MIM capacitance, Epi resistance, Thin Film Resistor (TFR) resistance and isolation leakage. A Wafer Acceptance Test (WAT) is performed by measuring 11 critical parameters on these PCMs. 75 % of the measured parameter values must lie within pre-defined minimum and maximum boundaries, for a wafer to be approved by the foundry.

The PCM data for the wafers on which the test-structures and amplifiers were processed is given in Table 7.1. In this table the monitored parameters are given together with the target value for this parameter and the average values measured on the two wafers. W1 is the wafer on which the test-structures were present and W2 contained the two HPA types. The first four parameters in the table are related to passive components, the remaining parameters refer to the active transistors. Most parameter values are close to the target values. The MIM capacitance value of W2 is smaller than the target of 600 pF/mm², which explains the positive frequency shift that was observed for both amplifiers. The drain currents at $V_{gs}=0$ V and at $V_{gs}=0.5$ V of W2 are significantly larger than target values, which means that the output power delivered by the transistors from this wafer is expected to be larger than average.

Table 7.1: PCM data of two wafers.

<i>Parameter Description</i>	<i>Unit</i>	<i>Target</i>	<i>W1</i>	<i>W2</i>
MIM Capacitance	pF/mm ²	600	593	579
Backside via resistance	Ω	1	0.18	0.17
Epi sheet resistance	$\Omega/\square$	160	163.1	164.5
TFR sheet resistance	$\Omega/\square$	50	50.0	49.0
Peak g_m	mS/mm	410	420	417
I_{ds} @ $V_{gs}=0$ V	mA/mm	360	374	392
I_{ds} @ $V_{gs}=0.5$ V	mA/mm	490	507	517
Turn-on resistance	$\Omega \cdot \text{mm}$	1.3	1.26	1.23
V_{dg} breakdown	V	20	21.3	20.6
Threshold voltage	V	-1.15	-1.15	-1.21
Cut-off frequency	GHz	60	61.7	63.0

7.2.2 Monte-Carlo analysis on HPA 1

The effect of process variation on HPA performance is performed through a MC analysis, in which the relevant parameters are varied according to their expected distributions. An overview of these parameters and their variations is given in Table 7.2.

Table 7.2: Parameter variation for MC analysis, all distributions are Gaussian.

<i>Parameter</i>	<i>Unit</i>	<i>Nominal</i>	<i>Standard deviation</i>
Wafer thickness	μm	100	$\pm 3.3 \%$
MIM capacitance	pF/mm^2	600	$\pm 7.5 \%$
OGATE capacitance	pF/mm^2	370	$\pm 7.5 \%$
TFR sheet resistance	$\Omega/\square$	50	$\pm 5 \%$
Epi sheet resistance	$\Omega/\square$	160	$\pm 5 \%$
Threshold voltage	V	-1.15	$\pm 0.35 \%$
Voltage for maximum g_m	V	N/A	$\pm 0.1 \%$
Transconductance	S	410	$\pm 17 \%$

During the MC analysis, 100 trials were performed with random parameter sets from the given distributions. The simulated output power and PAE are given in Figure 7.2. The result from the nominal simulation, performed with the Momentum data of the passive networks, is indicated in black. The MC trials are performed with a model of this Momentum data, therefore the results from the nominal trial are not necessarily equal to the nominal simulation result. For some MC trials, convergence of the HB simulation is not obtained for all frequencies, which results in discontinuities in the results. It can be seen that the upper frequency band edge of 3.4 GHz is guaranteed. The lower frequency band edge is shifted toward 3.0 GHz for several trials.

Figure 7.2: MC simulation results (red) and nominal simulation result (black) of output power and PAE of 20 W S-band amplifier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $P_{avs}=25$ dBm.

The Probability Density Function (PDF) and Cumulative Density Function (CDF) of the simulated output power frequencies of 2.9 GHz, 3.1 GHz and 3.4 GHz are given in Figure 7.3. The possible reduction of output power at a

frequency of 2.9 GHz is visible, at this frequency the output power is higher than 42 dBm for more than 50 % of the cases. At the centre frequency of 3.1 GHz, more than 90 % of the devices have an output power within a range of 1 dB. This variation is comparable to the variation that can be expected from a standard CS amplifier [182, 183].

Figure 7.3: Distribution of output power of 20 W S-band amplifier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $P_{avs}=25$ dBm.

Figure 7.4 shows the PDF and CDF of the simulated PAE. At a frequency of 2.9 GHz, the PAE is higher than 35% for 50% of the cases. For 3.1 GHz and 3.4 GHz, this PAE is reached for 90% and 80 % of the cases respectively.

Figure 7.4: Distribution of PAE of 20 W S-band amplifier, $V_{dd}=24$ V, $V_{ss}=-5$ V, $T_a=25$ °C, $P_{avs}=25$ dBm.

7.3 Screening

The active devices of conventional amplifiers are normally tested on pinch-off behaviour and breakdown voltage. In a standard, CS amplifier all terminals of the transistors in a single stage share a single DC connection, which mean that these parameters cannot be determined for each individual transistor. The goal of the measurements, however, is to find if any of the transistors in the stage shows an excessive leakage current below pinch-off, often caused by incomplete etching of the gate recess [184], or an excessive breakdown current below the breakdown voltage. If all transistors in a stage are measured simultaneously, the currents of a malfunctioning transistor will dominate the overall current, which means that the presence of such a transistor is detected. Although applying these methods to a complete power amplifier does not provide the pinch-off and breakdown voltages for each individual transistor, it tells whether any of the devices in the stage either has a very low breakdown voltage or is not able to pinch-off the active channel. In both cases the MMIC concerned should be labelled as 'bad' and should not be applied in a front-end.

7.3.1 HPA screening procedures

Within a Stacked-FET amplifier, the common screening procedure is not applicable. This is illustrated on the basis of Figure 7.5, which shows the topology of a single Stacked-FET amplifier stage with respect to DC connectivity. In contrast to a CS stage, not all transistor in a Stacked-FET stage share a common gate, drain and source connection which means that not all pinch-off or breakdown currents can be monitored simultaneously. The Stacked-FETs within the stage only share a common drain supply connection, which implies that only the total drain current of all Stacked-FETs in the stage can be measured. The terminals of the transistors in the stacks are not accessible via test nodes, which means that the transistors cannot be forced into the required pinch-off or breakdown region using the standard screening method. For these reasons alternative screening methods need to be defined.

Figure 7.5: Typical Stacked-FET amplifier stage build-up from DC point of view, where each stacked-FET is comprised of three transistors.

Simulations and measurements are performed on the $3 \times 8 \times 350 \mu\text{m}$ Stacked-FET test structure depicted in Figure 7.6. This test structure was already reported in Chapter 3 and contains a single Stacked-FET as applied in HPA1, including the gate biasing circuits. Stabilisation is obtained through the RC-network at the gate of the CS-FET and the stabilisation resistors in series with the external voltage balancing capacitors of the gates of the DCG-FETs. All issues relevant in the HPA are present in this test structure which makes it a useful device for testing the developed screening procedure.

Figure 7.6: Stacked-FET of three $8 \times 350 \mu\text{m}$ FETs including gate biasing circuits.

7.4 Pinch-off screening

The first screening step is performed to see whether all the active channels in the transistors can be pinched-off via the gate voltage. For the WIN PP25-20 process, the pinch-off voltage is defined as the gate-to-source voltage where the drain current is 1 mA/mm. The pinch-off measurement of the PCM devices, performed by the foundry to monitor the quality of the wafer, is performed at a drain-to-source voltage of 1.5 V.

7.4.1 Procedure and simulations

The pinch-off voltages of the transistors in the Stacked-FET are measured sequentially. The gate-to-source voltage of the FET under test is swept from -3 V to 0 V while at the remaining FETs the gate-to-source voltage is kept at 0 V. By doing this the FET under test dominates the total drain current in the pinch-off voltage can be found. The pinch-off voltage tests are performed at a stack drain supply voltage of 8 V.

The pinch-off screening is described, starting from the top DCG-FET and working toward the CS-FET. The exact order, however, is not relevant.

Degenerated Common Gate FET 2

To find the pinch-off voltage of DCG-FET 2, the voltages V_{g1} and V_{g2} are kept at 0 V (see Figure 7.7) , while V_{g3} is varied from -3 V to 0 V.

Figure 7.7: Determination of pinch-off on DCG-FET 2.

The simulated drain current of the stack is shown in Figure 7.8 as a function of V_{g3} , for different values of pinch-off voltage shift. The voltage V_{g3} at which the stack starts to conduct corresponds to the pinch-off voltage of DCG-FET 2. From the nominal situation, with $\Delta V_p=0$ V, it is found that the nominal pinch-off voltage is approximately -1.53 V. The simulations at $\Delta V_p=\pm 0.3$ V, which are the boundaries of the window guaranteed by the foundry, show that this shift directly translates to the measured drain current profile.

Figure 7.8: Drain current of stack as function of V_{g3} , $V_{g1}=V_{g2}=0$ V, $V_{dd}=8$ V.

Degenerated Common Gate FET 1

The pinch-off voltage of DCG-FET 1 is determined with a voltage V_{g1} of 0 V. Gate voltage V_{g3} was kept equal to the drain voltage of the stack to maintain transistor DCG2 in its conductive state, see Figure 7.9. Gate voltage V_{g2} is varied from -3 V to 0 V.

The simulated normalised stack current is shown in Figure 7.10. The shift in drain current profile corresponds to the shift in pinch-off voltage of DCG FET 2.

Figure 7.9: Determination of pinch-off on DCG-FET 1.

Figure 7.10: Drain current of stack as function of V_{g2} , $V_{g1}=0$ V, $V_{g3}=V_{dd}=8$ V.

Common source FET

To determine the pinch-off voltage of the CS-FET, the gate voltages of both DCG FETs are equal to the stack drain supply voltage, see Figure 7.11. The gate voltage V_{g1} of the CS-FET is varied from -3 V to 0 V.

The simulated normalised stack current is shown in Figure 7.12. Also for this setup the observed drain current profile shift shows a one to one relation with the offset in pinch-off voltage.

Figure 7.11: Determination of pinch-off on CS-FET.

 Figure 7.12: Drain current of stack as function of V_{g1} , $V_{g2}=V_{g3}=V_{dd}=8$ V.

Pinch-off voltage extraction

The gate supply voltages at which the drain current limit of 1 mA/mm is reached are given in Table 7.3 for all transistors and simulated values of ΔV_p . The obtained pinch-off voltages are equal for all three transistors and have a direct relation to the pinch-off variation of the process.

Table 7.3: Pinch-off voltages extracted from simulations.

ΔV_p	V_{CS}	V_{DCG1}	V_{DCG2}
-0.3	-1.84	-1.83	-1.83
0	-1.54	-1.53	-1.53
0.3	-1.24	-1.23	-1.23

7.4.2 Measurements on test-structure

The test sequence described in the previous section is applied to the Stacked-FET test structure depicted in Figure 7.6.

The measured drain current versus gate-to-source voltage for the three FETs in the stack is shown in Figure 7.13. For all three FETs in the stack, a pinch-off voltage of ± 1.39 V is extracted. This yields a ΔV_p of 0.14 V.

Figure 7.13: Pinch-off measurement on stack of three FETs.

7.5 Breakdown screening

The breakdown voltage of the PP25-20 transistors is defined as the drain-to-gate voltage where the (negative) gate current is 1 mA/mm while the gate-to-source voltage is lower than the pinch-off voltage. The foundry measures the breakdown voltage of the PCM devices at a gate-to-source voltage of -3 V, this value is maintained for the screening of the Stacked-FET amplifiers.

7.5.1 Procedure and simulations

To determine the breakdown voltages of the individual FETs of the stack, the gate-to-source voltage of the FET under test is kept at -3 V while the drain supply voltage is swept from 1 V to 25 V . This corresponds to the breakdown test of the foundry. In the stack, however, the remaining FETs are kept in their conducting state ($V_{gs}=0\text{ V}$) or isolating state ($V_{gs}=-3\text{ V}$), depending on whether they are in the current path or not, to ensure that the breakdown current is dominated by the FET under test. The breakdown currents are measured on the drain supply connection. The breakdown screening is described, starting from the top DCG transistor, and working towards the CS transistor. The exact order in which the measurements are performed, however, is not relevant.

Degenerated Common Gate FET 2

Breakdown of the DCG-FET 2 can be determined by pinching off all FETs in the stack and increasing the stack supply voltage as illustrated in Figure 7.14. Only the drain-to-gate junction of DCG-FET 2 is stressed and therefore the only current that is drawn from the drain supply source flows through the gate of DCG-FET 2.

Figure 7.14: Determination of breakdown on DCG-FET 2.

The resulting breakdown current is shown in Figure 7.15 for different values of gate resistor R_{g3} . As discussed in Chapter 3, the gate resistance of the DCG-FETs will be in the $\text{k}\Omega$ range. Since the gate resistor of the FET to be measured is in the current path, the maximum current is limited by this resistor.

The breakdown voltage is defined as the drain-to-gate voltage at which the

drain-to-gate current equals 1 mA/mm. It is seen that for gate resistance values larger than 10 Ω this current is limited by the gate resistor and the breakdown voltage cannot be read from the result. For this reason an alternative definition of breakdown voltage V'_{bd} is defined as the drain-to-gate voltage at which the drain-to-gate current equals 1 μ A/mm. It can be seen that at this low current level the impact of the gate resistor is negligible.

Figure 7.15: Simulated breakdown current of DCG-FET 2, $V_{g1}=V_{g2}=V_{g3}=-3$ V, $\Delta V_{br}=0$ V, $R_{g2}=3.2$ k Ω , $R_{g1}=125$ Ω .

Figure 7.16 shows the simulated breakdown current as a function of stack drain supply voltage for three values of breakdown voltage shift. The gate resistance is 3.2 k Ω , equivalent to the value in the test structure. At a breakdown current value of 1 μ A/mm, the three curves are parallel with a shift in voltage of 3 V, which is equal to the shift in breakdown voltage. This shows that the alternative breakdown voltage definition is valid.

Figure 7.16: Breakdown current of DCG FET 2, $V_{g1}=V_{g2}=V_{g3}=-3$ V, $R_{g2}=R_{g3}=3.2$ k Ω , $R_{g1}=125$ Ω .

Degenerated Common Gate FET 1

The breakdown voltage of the DCG FET 1 is measured with V_{g3} equal to the stack supply voltage and V_{g1} and V_{g2} at a voltage of -3 V, see Figure 7.17. As the DCG-FET 2 conducts, the drain-gate of DCG-FET 1 is stressed and carries all breakdown current.

Figure 7.17: Determination of breakdown on DCG-FET 1.

The simulated DCG-FET1 breakdown current is shown in Figure 7.18. Also for this transistor the voltage shift at a breakdown current level of 1 μ A/mm equals the breakdown voltage shift, showing the validity of the alternative

breakdown voltage definition.

Figure 7.18: Breakdown current of DCG-FET 1, $V_{g1}=V_{g2}= -3$ V, $V_{g3}=V_{dd}$, $R_{g2}=R_{g3}=3.2$ k Ω , $R_{g1}=125$ Ω .

Common Source FET

To determine the breakdown of the CS-FET, V_{g2} and V_{g3} are equal to the stack drain supply voltage and V_{g1} is connected to -3 V, see Figure 7.19.

Figure 7.19: Determination of breakdown on CS-FET.

The simulated breakdown current of the CS-FET is shown in Figure 7.20. It can be seen that the onset of current saturation occurs at a higher current level when compared to the measured results from the DCG-FETs. This is due to the

lower series resistance, which in this case consists of the gate resistance of the CS transistor and the channel resistance of the DCG FETs. At a breakdown current of $1 \mu\text{A}/\text{mm}$, the voltage shift equals the breakdown voltage shift, showing that the alternative breakdown voltage definition is also valid for this transistor.

Figure 7.20: Breakdown current of CS-FET, $V_{g1} = -3 \text{ V}$, $V_{g2}=V_{g3}=V_{dd}$, $R_{g2}=R_{g3}=3.2 \text{ k}\Omega$, $R_{g1}=125 \Omega$.

Breakdown voltage extraction

The drain supply voltages at which the alternative drain-to-gate current limit of $1 \mu\text{A}/\text{mm}$ is reached is given in Table 7.4. The variation between the observed results for the transistors is approximately 0.6 V . For all three transistors a direct relation to the breakdown voltage shift ΔV_{br} is visible.

Table 7.4: Alternative breakdown voltages extracted from simulations.

ΔV_{br}	$V'_{br,CS}$	$V'_{br,DCG1}$	$V'_{br,DCG2}$
-3	13.82	14.17	14.24
0	16.82	17.17	17.24
3	19.82	20.17	20.24

7.5.2 Measurements on test-structures

The breakdown current measurement sequence is applied to the Stacked-FET test structure. The measured breakdown currents versus drain-to-gate voltage for the three FETs in the stack is shown in Figure 7.21. Due to that fact that the gate resistor for the CS-transistor is significantly smaller than for DCG-transistors, the maximum current for the CS-FET is one order of magnitude higher, as could

already be observed from a comparison of Figure 7.16, Figure 7.18 and Figure 7.20 . It is seen that the accuracy of measured currents smaller than $10 \mu\text{A}/\text{mm}$ is poor due the limited resolution and accuracy of the measurement system.

Figure 7.21: Breakdown measurement on stack of three FETs.

The alternative breakdown voltages at a drain current of $1 \mu\text{A}/\text{mm}$ are obtained from extrapolation of the measured data and given in Table 7.5, together with the estimated ΔV_{br} obtained from a comparison with the nominal results given in Table 7.4. A variation of breakdown voltage between the transistors in the Stacked-FET of 3.1 V is observed, transistor DCG2 shows the lowest breakdown voltage. In order to find these breakdown voltages with higher accuracy, the breakdown current measurement should be performed with more accurate current measurement equipment.

Table 7.5: Alternative breakdown voltages and ΔV_{br} extracted from simulations.

Transistor	V'_{br}	ΔV_{br}
CS	14.49	-2.3
DCG1	15.97	-1.2
DCG2	12.92	-4.3

7.6 Conclusion

In this chapter the effect of processing imperfections on Stacked-FETs is analysed. It is shown that the expected sensitivity of output power and PAE to process variation is not larger than for CS-based amplifiers. A method for the screening of Stacked-FET power amplifier is defined and demonstrated by the measurements on a single $3\times 8\times 350\text{ }\mu\text{m}$ stack. This procedure provides the possibility to discriminate between good and non-good dies before further application of these dies. From the simulated results it is concluded that the pinch-off and breakdown voltage shifts of the individual FETs can be observed from measurements on the entire stack under various DC bias conditions. The pinch-off voltage can directly be determined from a gate voltage sweep on the particular FET. The breakdown currents are limited by the gate resistors, this makes it more difficult to directly determine the breakdown voltage. This implies that either an alternative definition should be used or an additional measurement point should be introduced directly at the gate. The latter is not preferred and therefore an alternative breakdown voltage is defined at a drain-to-gate current density of $1\text{ }\mu\text{A/mm}$. Using this alternative current limit puts a higher demand on the accuracy and resolution of the breakdown current measurement. The developed method is demonstrated by the measurements on $3\times 8\times 350\text{ }\mu\text{m}$ test-structure. The same method can be applied to the individual stages of a complete Stacked-FET power amplifier. Although the method does not provide the exact values of pinch-off and breakdown voltages, it is capable of detecting extreme cases in which the devices concerned can be labelled as non-good.

CHAPTER 8

Conclusions and outlook

8.1 Thesis overview

This thesis describes, structures and demonstrates the application of Stacked-FETs as building blocks for GaAs Monolithic Microwave High-Power Amplifiers for Active Electronically Scanned Array Radar Front-Ends. In chapter 2 of this thesis, the basic concepts and terms related to the field of high power amplifier design are given. The Stacked-FET concept is introduced and a brief overview is given of related fields where the concept of transistor stacking can be beneficial.

In chapter 3, a procedure for the design of Stacked-FETs is given, taking into account the parasitic capacitances of the transistors. A detailed description is given of the methods to equalize the voltages and currents of the transistors in the stack, which is required for efficient power summation in the stack. For the equalisation of the voltages across the different transistors in the Stacked-FET, external gate capacitances are used. For the equalisation of the currents within the Stacked-FET, three main methods are described. These are: an external shunt inductor at the source, an external capacitor from the source to the drain of the upper transistor and an external drain-to-source capacitor. The latter was selected as the optimum solution for GaAs pHEMTs, since this offers a larger bandwidth and requires less chip area. Although the described method is based on the small-signal model of the transistors, the method is still valid in the non-linear regime if the large-signal equivalents of the model parameters are extracted. Two methods are described to perform this extraction. One method is based on the linearisation of the response of a non-linear transistor model to a small test signal while being excited by a large RF-signal. The second method is based on the measured small-signal two-port parameters for various biasing conditions, from which the model parameters can be extracted. The equivalent large-signal model

parameters are determined along the expected load line during large-signal operation. The effect of transistor stacking on obtainable bandwidth is first analysed using the Bode-Fano limit. The maximum bandwidth that can be obtained through optimal matching, reduces as the number of transistors in the Stacked-FET increases. This is due to the increase of the Q-factor of the required load. The significance of this effect depends on the selected current balancing option. It was shown that the implementation with an external drain-to-source capacitance is suitable for application at S-band. The reduction of the matching ratio due to the increased real part of the load impedance of the Stacked-FET relaxes the matching problem at the amplifier output and has a large effect on the practically obtainable bandwidth. The stacking of three transistors can increase the maximum obtainable bandwidth with a factor of 2 in comparison to a conventional CS output stage. Analysis of the load mapping of the DCG stages show that possibilities for harmonic tuning of the Stacked-FET are limited. The balancing procedure is demonstrated by the design and verification of a family of Stacked-FET structures containing two to four transistors.

Chapter 4 describes a modelling approach that increases the flexibility with respect to transistor layout, which is required for accurate simulation of the unconventional transistor layouts of the DCG FETs. The modelling approach is based on the extraction of the parameters of a single intrinsic gate finger from S-parameter measurements on a two-finger transistor and an accurate EM-simulation on the extrinsic part of that transistor. The electrical behaviour of the single intrinsic gate finger is described with a compact model. Arbitrary transistor geometries can now be constructed from this intrinsic gate finger model in combination with an EM analysis results on a newly defined extrinsic part. It is shown that this modelling approach can be used to perform accurate simulations on large Stacked-FET structures.

In chapter 5, the stability of the Stacked-FET is analysed. The stability of the individual FETs in the stack is discussed and methods to increase the stability are investigated. The CS-transistors are stabilised using parallel RC-networks at the gate. This approach is copied from the design of standard, CS-transistor based amplifiers. The parallel RC-network is dimensioned such that the CS-transistor of the Stacked-FET is unconditionally stable. This relaxes the requirements for the DCG-transistors, where the penalty in RF-performance for stabilising is larger. Improvement of the DCG stability is often performed with a resistor in series with the gate balancing capacitor. This method is thoroughly investigated and it is shown that this approach is not adequate for the GaAs based Stacked-FETs that are discussed in this thesis. In order to find the optimum solution of a stable Stacked-FET with maximum possible RF performance, a brute-force method is introduced to incorporate the stability considerations into the Stacked-FET design procedure. To analyse the stability of the Stacked-FET, the expected loads at the source of any transistor in the stack are compared with the load stability

circles of the preceding transistors.

Chapter 6 describes the design and analysis of two S-band GaAs HPAs based on Stacked-FET topologies. The first amplifier is a single-stage amplifier that was designed according to the strategy described in chapter 3 and has an output power of 20 W with an associated PAE of more 40 %. The second amplifier is a two-stage amplifier, which has an output power of 30 W with an associated PAE of more 40 %. It is designed according to the brute-force procedure described in chapter 5, including the stability consideration as an integral part of the design procedure. A comparison of the results of these two HPAs with previously published results is given in section 8.2.

In chapter 7, the expected yield of the Stacked-FET HPAs is discussed. The sensitivity to process variations is analysed and a method is developed and demonstrated to perform DC screening of the transistors inside a Stacked-FET HPA. Test sequences are given to measure shift in threshold voltage and breakdown voltage. The procedure is successfully applied to a single Stacked-FET containing three transistors, both in simulation and measurement.

8.2 Comparison to previously published results

In this section the performance of the two HPAs described in chapter 6 is benchmarked against prior results from literature. For this purpose two figures of merit are defined. The first Figure Of Merit (FOM), denoted as Efficient Power per Area (EPA) combines output power, PAE and chip area A according to:

$$\text{EPA} = \frac{P_{out} \cdot \text{PAE}}{A}. \quad (8.1)$$

The reasoning behind this FOM is that output power and PAE are key aspects of power amplifier performance while the chip area is directly related to costs.

In the second FOM the fractional bandwidth and large-signal gain G_{LS} are included as key parameters. A high amplifier output power and PAE are more difficult to achieve over a larger fractional bandwidth whilst the large-signal gain G_{LS} is directly related to the number of stages and therefore indirectly limits the achievable amplifier PAE and x-size. This FOM, the Broadband Efficient Power per Area (BEPA), is defined according to:

$$\text{BEPA} = \frac{P_{out} \cdot \text{PAE} \cdot G_{LS} \cdot (f_h - f_l)}{A \sqrt{f_h f_l}}, \quad (8.2)$$

where f_l and f_h are the lower and upper frequency band edges respectively.

Table 8.1 provides a comparison of the current results against published GaAs and GaN S-band power amplifiers.

The drain bias voltage of the two Stacked-FET HPAs is substantially higher than for the other GaAs devices. The highest EPA for GaAs devices is achieved by HPA 1, mainly due to the compact design. The GaAs device with the highest BEPA is HPA 2, due to the inclusion of the first amplifier stage without losing compactness. This HPA also shows the highest output power level.

When compared to the GaN devices in the table, the two current HPAs have a drain supply voltage that is comparable to the other devices. The EPA approximates the other values while the BEPA is within the GaN range, even beating two of the four mentioned designs.

This shows the positioning of the Stacked-FET GaAs performance in-between the conventional GaAs-HPA and GaN-HPA performance.

Table 8.1: Comparison to previous work.

Reference	Technology	V_d	$I_{d,LS}$	Frequency	P_{out}	PAE	G_{LS}	A	EPA	BEPA
		(V)	(A)	(GHz)	(W)	(%)	dB	(mm ²)	(W/mm ²)	(W·dB/mm ²)
[31]	GaN	28	5.93	2.9 - 3.5	85	59	24	5 × 4.4	2.28	10.3
[33]	GaN	25	2.67	2.8 - 3.4	32	47	20	4.3 × 5.6	0.62	2.4
[36]	GaN	35	3.1	3.2 - 4.3	50	43	21	4.1 × 3.1	1.69	10.5
[185]	GaN	26	3.87	2.7 - 3.3	30	30	16	5 × 3.3	0.55	1.8
[20]	GaAs	8	7.38	2.4 - 3.6	16.6	28	24	4.9 × 5.7	0.17	1.6
[21]	GaAs	8	4.5	2.8 - 3.8	14	40	32	6 × 4.65	0.2	2.0
[186]	GaAs	6	1.17	2.75 - 3.75	2.5	44	29	5.25 × 2.8	0.07	0.7
HPA 1	GaAs	24	1.7	2.9 - 3.6	18	41	15.5	3.95 × 2.35	0.8	2.7
HPA 2	GaAs	24	3	2.6 - 3.5	25	40	31	4.5 × 4.5	0.5	4.56

8.3 Conclusions

The application of Stacked-FETs results in amplifiers with an increased drain bias voltage that are smaller in y-dimension, due to the reduced number of transistors in parallel. The x-dimension of the chip can be smaller as well. Although the dimension of the active parts in this direction is increased, the reduced number of passive power combiners and possibly the reduction of the number of stages due to the higher gain offsets this increase. The chip area reduction is illustrated in Figure 8.1, where the layout of the two-stage Stacked-FET HPA is compared to the estimated size of a conventional CS HPA with equal output power and gain. This estimation is obtained by linear scaling of the y-dimension of the amplifier in [21] to the required output power. The major difference in x-size and y-size is easily identified.

Figure 8.1: Comparison of chip size Stacked-FET HPA and conventional CS HPA.

8.4 Original contributions

The original contributions reported in this thesis are:

- Structured microwave Stacked-FET analysis and the derivation of design equations for voltage and current balancing components based on all relevant transistor parameters including parasitic capacitances.
- Analysis of the effect of transistor stacking on bandwidth limitations for Stacked-FET microwave power amplifiers.
- Adaption of single intrinsic gate finger modelling approach and application to accurate simulation of Stacked-FET layouts.
- Analysis of the mapping of out-of-band terminations, showing the limited

possibilities for harmonic tuning for Stacked-FETs, as well as the origin of the stability complexity.

- Definition of a strategy for the inclusion of stability constraints during the design of a Stacked-FET, enabling the explicit compromising between stability and RF-performance.
- Introduction of method for DC-screening of transistors in a Stacked-FET HPA.
- Demonstration of the potential for 30-Watt class, GaAs Stacked-FET microwave power amplifiers.

8.5 Future directions

Future research on Stacked-FET amplifiers is suggested to focus on four different directions:

1. *Increase of output power level*

The Stacked-FET concept helps to increase the output power of integrated power amplifiers, while maintaining an acceptable chip size. One of the limits to the amount of power that can be generated is the chip temperature. The area-efficient power combining provides the option to sacrifice some chip-area efficiency and allow a larger chip for the benefit of a lower thermal resistance.

By selecting the proper combination of unit transistor size, stack height and number of stacks in parallel, the required load impedance of the output stage can be optimized, perhaps even to directly match the target load impedance of the amplifier.

The most straightforward approach for output power increase is by increasing the number of parallel stacks. It is expected that this approach is feasible for an increase of $\sim 50\%$. For higher power levels the chip dimensions will become unacceptably large.

2. *Extension of operating frequency*

One of the main focusses of future research will be on the extension of the operating frequency of the GaAs Stacked-FETs described in this thesis, up to Ku-band and above. In chapter 3 the design of a Stacked-FET is demonstrated by a numerical example. It is seen that with the current parameter values, the real part of the required external gate admittance becomes negative, which yields a first operating frequency limitation.

The real part of the required $Y_{gX,n}$ of stage n can be written as:

$$\Re Y_{gX,n} = \frac{-\omega((n-1)C_{gs} + nC_{gd})(\omega C_{gd}G_{L,CS} + g_m B_{L,CS} + C_{gd}g_m\omega + \omega C_{ds}g_m)}{(G_{L,CS} + (1-n)g_m)^2 + (B_{L,CS} + n\omega C_{gd} + \omega C_{ds})^2}. \quad (8.3)$$

Since $C_{gs} \gg C_{gd}$ the real part of $Y_{gX,n}$ is almost directly proportional to C_{gs} . This means that a reduction C_{gs} reduces the real part of the required $Y_{gX,n}$. A method to reduce the effective value of C_{gs} is by applying an external gate-to-source inductor [81]. It is expected that this method can be used to extend the maximum possible operating frequency of the Stacked-FETs described in this thesis.

Operation at higher frequencies requires an even more accurate modelling approach. For the dimensioning of the voltage and current balancing components, more parasitic effects (such as the extrinsic inductances and access resistances) might have to be taken into account. For the simulations, the single gate finger modelling as described in chapter 4 needs to be extended to include the non-linear behaviour of the active transistor part.

3. Expansion of Stacked-FET theory

Expansion of the theory and mainly on the impact of stability considerations can lead to Stacked-FETs that lose less power and efficiency due to stability enhancement. Deeper insight can help to develop Stacked-FET structures that are 'just stable enough'. These stacks might not be unconditionally stable, but are stable within the actual expected impedance levels in the stack.

High efficiency operating classes for Stacked-FET can be further explored. An example of mixed class operation of the transistors in a Stacked-FET is described in [104]. It is to be investigated if this approach, in combination with the load mapping of the DCG transistors as described in chapter 3, can be used to increase the efficiency of the Stacked-FETs. Internal load tuning could be applied, not only to generate the required impedance levels, but also to modify the load mapping functions at the harmonic frequencies.

4. Application to different semiconductor material systems

The theory developed in this thesis can also be used to design Stacked-FET amplifiers in other technologies. Although the concept of transistor stacking is often applied in (Bi)CMOS processes, the stability and modelling approach might improve the RF-performance of the stacks in these technologies. Modern high power processes such as GaN and LDMOS, benefit from the high breakdown voltage of the transistors and, hence, already support the use of a high drain bias voltage. The application of

Stacked-FETs in these technologies, however, can still further increase the supply voltage and the effective power per chip-area.

Stacked-FET GaAs amplifiers offer an interesting alternative to amplifiers implemented in III-V technologies with a high breakdown voltage, such as GaN. The results presented in this thesis show that Stacked-FET GaAs HPAs can be true competitors for GaN devices, possibly extending the lifetime for GaAs based processes as power technologies for AESA radar front ends.

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- [P1] G. van der Bent, A. P. de Hek, and F. van Vliet, "Incorporating Stability Analysis in the Design of Integrated GaAs Stacked-FET High-Power Amplifiers," Submitted for publication to *IEEE Transactions on Microwave Theory and Techniques*.
- [P2] G. van der Bent, A. P. de Hek, and F. E. van Vliet, "Design Procedure for Integrated Microwave GaAs Stacked-FET High-Power Amplifiers," Submitted for publication to *IEEE Transactions on Microwave Theory and Techniques*.
- [P3] G. van der Bent, A. P. de Hek, and F. E. van Vliet, "EM-Based GaN Transistor Small-Signal Model Scaling," in *European Microwave Integrated Circuits Conference (EuMIC)*, Sept. 2018.
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Summary

The HPA is a key component for any modern AESA radar front-end, both in terms of costs and performance. The task of this HPA is to generate the high level of required output power with an efficiency that results in feasible requirements for the cooling of the system. This must be combined with a reasonable cost price and reliable operation.

To increase the supply voltage of a radar front-end yields several advantages. At the system level, lower DC currents are present, resulting in lower losses in the supply lines. On transistor level, the real part of the optimum load impedance is higher, which eases the matching problem, resulting in matching networks with higher bandwidth or lower loss. State-of-the-art technologies based on wide-bandgap materials such as GaN, support the requirements for high supply voltages. The cost of these technologies, however, is significantly higher than the GaAs technologies, while the latter still have a more proven record of reliability.

The research question addressed in this thesis is whether the advantages of an increased supply voltage can be obtained without the use of a wide-bandgap semiconductor technology, specifically by the application of the Stacked-FET technique. At the heart of this approach is a single CS FET, followed by one or more DCG FETs. Stacking a number of transistors linearly increases the overall breakdown voltage and hence the possible drain supply voltage, providing the previously mentioned advantages. An additional benefit of the Stacked-FET concept is due to the internal power combining by voltage summation, which decreases the chip area required for passive combining networks.

Answering this question is not a straightforward matter. The voltages and currents of the individual transistors in the Stacked-FET should be well balanced in order to efficiently combine the RF power contributions of these transistors. The Stacked-FET should operate without any instabilities, which is not trivial due to the presence of the DCG FETs, which are inherently unstable. Balancing and stability are not always compatible and the goal of the design is to find the solution which yields a Stacked-FET configuration with maximum RF performance within the boundary condition of stable operation. Stability needs to be ensured by design, as unstable operation may instantly lead to failure.

Finally, the simulation of power transistors operating at microwave frequencies requires transistor models that accurately describe the intrinsic and parasitic effects, not only in the operating frequency band but, due to the requirement of accurate prediction of instabilities, for the entire frequency range from DC to the maximum frequency where the transistor exhibits gain. This research question has been addressed by others, for example at lower frequencies, at low power levels or including numerous simplifications. The aim of this work is to answer this question for contemporary S-Band high power amplifiers and without simplifications that might unnecessarily limit achievable performance.

In this thesis, the research questions are tackled through deeply understanding the mathematical voltage and current waveform limitations in a Stacked-FET configuration, the bandwidth limitations that arise due to the transistor stacking and the loading of the transistors inside the Stacked-FET; this places strict requirements on the accuracy on the transistor models and establishes the necessity of a proper stability to RF-performance trade-off. All these ingredients together enable the demonstration of HPAs that positively answer the initial research question, which can be screened on processing failures.

As a first step in this approach, the theoretical and practical behaviour and limitations of Stacked-FET amplifiers are systematically investigated. The in-depth analysis of Stacked-FET operation resulted in design equations which can be used to balance both the voltages and the currents within the stack. In contrast to previously published analysis results, this balancing takes into account all relevant transistor parameters.

As a second step, with the obtained insights in the operation of Stacked-FETs, the analysis of the maximum theoretical bandwidth of Stacked-FET amplifiers has shown that, depending on the balancing approach, the Bode-Fano limit can reduce with the numbers of FET in the stack. This puts a practical limit on the number of transistors that can be used in a Stacked-FET, typically three to four for GaAs power amplifiers operating at frequencies around 3 GHz.

The third step, having defined the current and voltage balancing components in the Stacked-FET, is to analyse the out-of band the loading effects of the transistors in the stacks. To this end the load mapping functions from the drain to the source of the DCG transistors are introduced. It is found that for certain combinations of DCG parameters, a passive load may results in an input impedance with a real part much smaller than zero, which is the root cause of the stability challenge. The approach to the stabilisation is therefore to modify this mapping function such that the stability problem can be solved with minor impact on the RF performance. Beside the impact on stability, the observed DCG load mapping also limits the possibilities for harmonic tuning of the transistors in the Stacked-FET, which means that operation at high efficiency classes is not trivial.

The fourth step in the approach is to develop a methodology to obtain accurate models of arbitrary, large transistors. Simulation of Stacked-FETs requires modifications to the standard transistor model, which is often only available for and suited to CS transistors. The flexibility in connecting especially the DCG transistors is obtained by excluding the transistor's extrinsic metal from the model such that the model describes the active intrinsic part only. The intrinsic gate finger characteristics are deembedded from a two-finger test transistor measurement and modelled using an intrinsic transistor model. This gate finger model is then used to model complex transistor geometries, in combination with an EM simulation on the extrinsic part.

After being able to analyse and accurately model the Stacked-FET, the fifth step is to investigate the stability of the Stacked-FETs as well as the stability of constitutive transistors. Many degrees of freedom exist to improve the stability of a Stacked-FET, all with a different impact on RF-performance. Due to this complexity of the stability problem, a brute-force method is defined to find the optimum compromise between RF-performance and stable operation.

As a sixth step the potential of Stacked-FET GaAs amplifiers is demonstrated by showing the results of several Stacked-FETs as well as two Stacked-FET power amplifiers. These amplifiers are a 20 W single stage amplifier and a 30 W two-stage amplifier, both delivering state-of-the-art performance with respect to output power, efficiency and bandwidth.

Finally, as a seventh step, a strategy is introduced to verify whether the transistors in the Stacked-FET amplifier are functional. Deviations in the pinch-off and breakdown voltage of the transistors can be monitored using the voltage supply pads of the amplifier.

The reported results demonstrate that GaAs Stacked-FET power amplifiers, designed according to the strategy defined in this thesis, can deliver an output power in excess of 25 W with a PAE higher than 40 % over a bandwidth of 30 % at S-band frequencies. With this RF performance, these devices can be competitive to many GaN based amplifiers, at significantly lower costs.

Samenvatting

Het verhogen van de voedingsspanning van een radar front-end levert verschillende voordelen op. Op systeemniveau resulteren de lagere DC-stromen in minder verliezen in de voedingslijnen. Op transistorniveau is het reële deel van de optimale belastingsimpedantie hoger, wat het ontwerp van de aanpassingsnetwerken vereenvoudigt. Dit resulteert in netwerken met een hogere bandbreedte of lager verlies. State-of-the-art technologieën op basis van materialen met een grote bandkloof, zoals GaN, ondersteunen de eisen voor hoge voedingsspanningen. De kosten van deze technologieën zijn echter aanzienlijk hoger dan de GaAs-technologieën, terwijl de betrouwbaarheid van de laatste nog steeds meer bewezen is.

De onderzoeksvraag die in dit proefschrift wordt behandeld, is of de voordelen van een verhoogde voedingsspanning kunnen worden verkregen zonder gebruik te maken van een halfgeleidertechnologie met grote bandkloof. Dit met name door toepassing van de gestapelde FET techniek, waarbij een enkele CS-FET wordt gevolgd door één of meer DCG-FET's. Het stapelen van een aantal transistoren resulteert in een lineaire verhoging van de totale doorslagspanning en derhalve de mogelijke voedingsspanning, hetgeen de eerder genoemde voordelen oplevert. Een bijkomend voordeel van het gestapelde FET concept is het feit dat de vermogens van de individuele transistoren worden opgeteld door spanningssommatie, waardoor minder chip oppervlak nodig is voor passieve combinatienetwerken.

Het beantwoorden van de onderzoeksvraag brengt verschillende uitdagingen met zich mee. De spanningen en stromen van de afzonderlijke transistoren in de gestapelde FET moeten goed gebalanceerd zijn om de RF-vermogensbijdragen van deze transistors efficiënt te combineren. Tegelijkertijd moet de gestapelde FET stabiel werken. Dit is zeker niet triviaal vanwege de aanwezigheid van de DCG-FET's, welke inherent instabiel zijn. Correcte balancerings- en stabiliteits- zijn niet altijd verenigbaar. Het doel van het ontwerp is om een gestapelde FET configuratie met maximale RF-prestaties te vinden binnen de randvoorwaarde van een stabiele werking. Stabiliteit moet worden verzekerd tijdens de ontwerpfase, omdat een instabiele werking tot onmiddellijke schade

kan leiden. Tenslotte vereist de simulatie van vermogenstransistoren die werken op microgolffrequenties, transistormodellen die de intrinsieke en parasitaire effecten nauwkeurig beschrijven. Deze nauwkeurigheid is niet alleen vereist in de primaire frequentieband, maar voor het gehele frequentiebereik van gelijkstroom tot de maximale frequentie waarbij de transistor versterking heeft. Deze onderzoeksvraag is door anderen aangepakt, bijvoorbeeld op lagere frequenties, voor lage vermogensniveaus of met talrijke vereenvoudigingen. Het doel van dit werk is om deze vraag te beantwoorden voor moderne S-Band vermogensversterkers en zonder vereenvoudigingen die de haalbare prestaties onnodig beperken.

In dit proefschrift worden de onderzoeksvragen beantwoord door diep inzicht te verkrijgen in de beperkingen van de spanning- en stroomgolfvormen in een gestapelde FET-configuratie, de bandbreedtebeperkingen die ontstaan door het stapelen van de transistoren en de belasting van de transistoren binnenin de gestapelde FET; dit bepaalt de vereiste nauwkeurigheid van de transistormodellen en de noodzaak van een goed compromis tussen stabiliteit van RF-prestatie. Al deze ingrediënten samen maken het mogelijk om HPA's te demonstreren die de initiële onderzoeksvraag positief beantwoorden, die tevens kunnen worden gescreend op fabricagefouten.

Als een eerste stap in deze benadering worden het theoretische en praktische gedrag en de beperkingen van gestapelde FET versterkers systematisch onderzocht. De diepgaande analyse van de werking van gestapelde FET's resulteert in ontwerpvergelijkingen die kunnen worden gebruikt om zowel de spanningen als de stromen in de stapel te balanceren. In tegenstelling tot eerder gepubliceerde analyseresultaten, houdt deze analyse rekening met alle relevante transistorparameters.

Als een tweede stap heeft, met de verkregen inzichten in de werking van gestapelde FET's, de analyse van de maximale theoretische bandbreedte van gestapelde FET versterkers aangetoond dat, afhankelijk van de balanceringsaanpak, de Bode-Fano-limiet kan verminderen met het aantal FET's in de stapel. Dit vormt een praktische limiet voor het aantal transistoren dat kan worden gebruikt in een gestapelde FET, meestal drie tot vier voor GaAs-vermogensversterkers die werken op frequenties rond 3 GHz.

De derde stap is, met de gedefinieerde stroom- en spanningscompensatiecomponenten in de gestapelde FET, het analyseren van de belastingseffecten van de transistors in de stapel buiten de primaire frequentieband. Hiertoe worden de impedantie afbeeldingsfuncties van de drain naar de source van de DCG-transistors geïntroduceerd. Het is gebleken dat voor bepaalde combinaties van DCG-parameters, een passieve belasting kan resulteren in een ingangsimpedantie met een reëel deel veel kleiner dan nul, wat de hoofdoorzaak is van de stabiliteitsuitdaging. Het doel van de stabilisatie is daarom om deze afbeeldingsfunctie zodanig aan te passen dat

het stabiliteitsprobleem kan worden opgelost met minimale invloed op de RF-prestatie. Naast de impact op de stabiliteit, beperkt de waargenomen DCG-belastingsafbeelding ook de mogelijkheden voor harmonische afsluiting van de transistoren in de gestapelde FET, wat betekent dat het toepassen van hoge efficiëntie klassen niet triviaal is.

De vierde stap in de aanpak is het ontwikkelen van een methodologie om nauwkeurige modellen van willekeurig grote transistoren te verkrijgen. Simulatie van gestapelde FET's vereist aanpassingen aan het standaard transistormodel, dat vaak alleen beschikbaar en geschikt is voor CS-transistoren. De benodigde flexibiliteit bij het aansluiten van met name de DCG-transistoren wordt verkregen door de effecten van het extrinsieke metaal uit het model van de transistor te nemen, zodanig dat het model alleen het actieve intrinsieke deel beschrijft. De intrinsieke transistorkarakteristieken worden verkregen uit de meting aan een tweevingerige testtransistor en gemodelleerd met behulp van een intrinsiek transistormodel. Dit intrinsieke transistormodel wordt vervolgens gecombineerd met een EM-simulatie aan het extrinsieke deel om een complexe transistorgeometrie te modelleren.

Na het nauwkeurig kunnen analyseren en modelleren van de gestapelde FET structuur, is de vijfde stap het onderzoeken van de stabiliteit van deze structuur evenals de stabiliteit van constitutieve transistoren. Er zijn veel vrijheidsgraden om de stabiliteit van een gestapelde FET te verbeteren, allemaal met een andere impact op de RF-prestaties. Vanwege deze complexiteit van het stabiliteitsprobleem, is een brute-force methode gedefinieerd om het optimale compromis te vinden tussen RF-prestaties en stabiele werking.

Als een zesde stap wordt het potentieel van gestapelde FET GaAs-versterkers gedemonstreerd door de resultaten te geven van verschillende gestapelde FET's en twee gestapelde FET vermogensversterkers. Deze versterkers zijn een 20 W eentrapsversterker en een 30 W tweetrapsversterker, beide leveren state-of-the-art prestaties met betrekking tot uitgangsvermogen, efficiëntie en bandbreedte.

Tenslotte wordt als een zevende stap een strategie geïntroduceerd om te verifiëren of de transistoren in de gestapelde FET versterkers functioneel zijn. Afwijkingen in de afknijp- en doorslagspanning van de transistoren kunnen worden opgespoord via de voedingsaansluitingen van de versterker.

De gerapporteerde resultaten tonen aan dat GaAs gestapelde FET vermogensversterkers, ontworpen volgens de strategie gedefinieerd in dit proefschrift, een uitgangsvermogen van meer dan 25 W kunnen leveren met een PAE hoger dan 40 % over een bandbreedte van 30 % op S-band frequenties. Met deze RF-prestaties kunnen deze versterkers concurrerend zijn met veel op GaN gebaseerde versterkers, tegen aanzienlijk lagere kosten.

List of Abbreviations

ADS	Advanced Design System
AESA	Active Electronically Scanned Array
BCB	Benzocyclobutene
BEPA	Broadband Efficient Power per Area
CBC	Current Balancing Component
CCA	Current Conduction Angle
CDF	Cumulative Density Function
CG	Common Gate
CS	Common Source
CW	Continuous Wave
DC	Direct Current
DCG	Degenerated Common Gate
DUT	Device Under Test
EM	Electro-Magnetic
EPA	Efficient Power per Area
ESD	Electro Static Discharge
FET	Field Effect Transistor
FOM	Figure Of Merit
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HB	Harmonic Balance
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HPA	High Power Amplifier
IMN	Input Matching Network
InP	Indium Phosphide
ISMN	Inter Stage Matching Network
KCL	Kirchhoff's Current Law
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LNA	Low Noise Amplifier

List of Abbreviations

LS	Large Signal
MC	Monte Carlo
MESFET	Metal-Semiconductor Field Effect Transistor
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
MSAG	Multifunction Self-Aligned Gate
MTTF	Mean Time To Failure
NDF	Normalised Determinant Function
NDPA	Non-Uniform Distributed Power Amplifier
NGF	Number of Gate Fingers
NPD	Normalised output Power Density
OMN	Output Matching Network
PAE	Power Added Efficiency
PCB	Printed Circuit Board
PCM	Process Control Monitoring
PDF	Probability Density Function
QFN	Quad-Flat No-Leads
RD	Return Difference
RF	Radio Frequency
RF-CMOS	Radio Frequency Complementary Metal Oxide Semiconductor
RR	Return Ratio
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
TaN	Tantalum Nitride
TFR	Thin Film Resistor
UGW	Unit Gate Width
WAT	Wafer Acceptance Test

List of Symbols

<i>Symbol</i>	<i>Description</i>	<i>Unit</i>
A_{IC}	Area of IC	mm ²
a_k	Coefficient for Lopez approximation of Fano equation	-
AF	Acceleration factor of MTTF	-
b_k	Coefficient for Lopez approximation of Fano equation	-
B_L	Imaginary part of load admittance	S
$B_{L,CS}$	Imaginary part of optimum load admittance for CS transistor	S
BW	Relative bandwidth	-
C	Component matrix	-
C_{ds}	Intrinsic drain-to-source capacitance	F
C_{dsT}	Total drain-to-source capacitance	F
C_{dsX}	External drain-to-source capacitance	F
C_{gd}	External gate-to-drain capacitance	F
C_{gs}	External gate-to-source capacitance	F
C_{gX}	External gate capacitance	F
c_{map}	Centre of load mapping circle	-
C_{out}	Output capacitance	F
C_{pd}	Parasitic drain capacitance	F
C_{pg}	Parasitic gate capacitance	F
C_{ps}	Parasitic source capacitance	F
c_L	Centre of load stability circle	-
C_L	Load capacitance	F
c_S	Centre of source stability circle	-
Γ^e	Reflection coefficient for even-mode excitation	-
Γ_{in}	Input reflection coefficient	-
Γ_L	Load reflection coefficient	-
Γ^m	Matching to required load	-
Γ_{ref}	Required load reflection coefficient	-

List of Symbols

δ	Duty cycle	%
ΔV_{br}	Breakdown voltage shift	V
ΔV_p	Pinch-off voltage shift	V
E_a	Activation energy	eV
f	Frequency	Hz
f_0	Fundamental frequency	Hz
f_h	Upper limit of frequency band	Hz
f_l	Lower limit of frequency band	Hz
G_A	Antenna gain	dB
G_{ds}	Drain-to-source conductance	S
G_k	Loop gain	-
G_L	Real part of load admittance	S
$G_{L,CS}$	Real part of optimum load admittance for CS transistor	S
g_m	Transconductance	S
G_P	Power gain	-
G_T	Transducer gain	-
η_d	Drain efficiency	%
i_{cor}	Correction current	A
$\mathbf{I}$	Identity matrix	-
$\mathbf{I}_e$	External current vector	A
$\mathbf{I}_i$	Internal current vector	A
i_{in}	Input current	A
I_{max}	Maximum current of transistor	A
i_{out}	Output current	A
I_{peak}	Peak of current waveform	A
I_0	DC part of current	A
I_1	Current at fundamental frequency	A
I_d	Drain current	A
I_g	Gate current	A
J_{ds}	Drain-to-source current density	A/m
k	Boltzmann constant	eV/K
K	Rollet stability factor	-
κ	Thermal conductivity	W/m·K
L_{IMN}	Loss of input matching network	dB
L_{ISMN}	Loss of interstage matching network	dB
L_{OMN}	Loss of output matching network	dB
$L_{stacking}$	Loss due to non-perfect power combining in stacked-FET	dB
L_d	Drain inductance	H
L_g	Gate inductance	H
L_M	Loss of matching network	dB
L_s	Source inductance	H

λ	Wave length	m
M	System matrix for Ohtomo analysis	-
$m1$	Internal stability parameter	-
$M1$	Internal stability parameter	-
$m2$	Internal stability parameter	-
$M2$	Internal stability parameter	-
$MTTF$	Mean time To Failure	h
μ	Edwards / Sinsky Stability parameter	-
μ'	Edwards / Sinsky Stability parameter	-
N	Number of transistors in Stacked-FET	-
P_{avs}	Available source power	W
P_{DC}	Consumed DC power	W
P_{dens}	Power density	W/m
P_{diss}	Dissipated power	W
P_{in}	Input power	W
P_{out}	Output power	W
P_t	Transmitted power	W
PW	Pulse Width	s
Q	Quality factor	-
r	Matching ratio	-
R_d	Drain resistance	Ω
$R_{ds_{on}}$	Channel resistance below knee voltage	Ω
R_{ds}	Intrinsic drain-to-source resistance	Ω
R_{dsX}	External drain-to-source resistance	Ω
R_g	Gate resistance	Ω
R_{gX}	External gate resistance	Ω
R_{id}	Intrinsic drain-to-gate resistance	Ω
R_{is}	Intrinsic gate-to-source resistance	Ω
r_L	Radius of load stability circle	-
r_{map}	Radius of load mapping circle	-
R_{opt}	Optimum load resistance	Ω
RR	Return Ratio	-
R_s	Source resistance	Ω
r_S	Radius of source stability circle	-
R_{stab}	Stability resistance	Ω
R_{th}	Thermal resistance	K/W

List of Symbols

S	Scattering matrix	-
S	Number of parallel Stacked-FETs	-
S_{min}	Minimum detectable power	W
σ	Radar cross section	m ²
T_a	Ambient temperature	K or °C
T_{back}	Chip backside temperature	K or °C
T_{ch}	Active channel temperature	K or °C
T_{ref}	Reference temperature	K or °C
τ	Transconductance delay	s
V_0	DC part of voltage	V
V_1	Voltage at fundamental frequency	A
V_{br}	Breakdown voltage	V
v_d	Drain voltage	V
V_{dd}	Drain supply voltage	V
V_{dg}	Drain-to-gate voltage	V
V_{ds}	Drain-to-source voltage	V
V_e	External voltage vector	V
v_g	Gate voltage	V
V_{gs}	Gate-to-source voltage	V
V_i	Internal voltage vector	V
V_k	Knee voltage	V
V_p	Pinch-off votlage	V
v_s	Source voltage	V
W_u	Unit gate width	m
x	State variables	V or A
Y_{DCG}	Admittance matrix of DCG transistor	S
Y_{dNs}	Admittance of current balancing component from source to supply	S
Y_{ds}	Drain-to-source admittance	S
Y_{dsT}	Total drain-to-source admittance	S
Y_{dsX}	External drain-to-source admittance for current balancing	S
Y_{ee}	Submatrix of admittance matrix	S
Y_{ei}	Submatrix of admittance matrix	S
Y_F	Three port admittance matrix of FET	S
Y_{gd}	Gate-to-drain admittance	S
Y_{gs}	Gate-to-source admittance	S
Y_{gX}	External gate admittance	S

$\mathbf{Y}_{ie}$	Submatrix of admittance matrix	S
$\mathbf{Y}_{ii}$	Submatrix of admittance matrix	S
$Y_{L,CS}$	Optimum load admittance of CS transistor	S
$Y_{L,stack}$	Optimum load admittance of Stacked-FET	S
$\mathbf{Y}_{meas}$	Measured admittance matrix	S
Y_{ref}	Reference admittance	S
Y_{sX}	External shunt admittance to ground of current balancing	S
Y_L	Load admittance	S
Y_S	Source admittance	S
$\mathbf{Y}_{SGF}$	Admittance matrix of single gate finger	S
Z_L	Load impedance	Ω
ω	Angular frequency	Hz
ω_c	Angular centre frequency	Hz
ω_h	Upper angular frequency band limit	Hz
ω_l	Lower angular frequency band limit	Hz

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About the Author

Gijsbert van der Bent was born in Leiden, The Netherlands, 1975. He received the B.Sc. degree in electrical engineering from De Haagse Hogeschool in 1998. His bachelor thesis dealt with the design of high temperature integrated circuits in standard CMOS processes. In 2003 he joined TNO, The Netherlands, where he is involved in the design and characterisation of Monolithic Microwave Integrated Circuits. His main interest is in the design of integrated microwave power amplifiers for Active Electronically Scanned Array Radar applications.