**NANOSTRUCTURED
HYBRID
ORGANIC/INORGANIC
ELECTRONIC DEVICES**

TAMER DOĞAN

*NANO-STRUCTURED HYBRID ORGANIC / INORGANIC
ELECTRONIC DEVICES*

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**NANO-STRUCTURED HYBRID ORGANIC / INORGANIC ELECTRONIC
DEVICES**

DISSERTATION

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on the account of the decision of the graduation committee,
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by

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This thesis is dedicated to my wife...

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Chapter 1 Introduction

1.1. Motivation

There has been an increasing interest in organic semiconductors within the last decades due to their attractive properties such as flexibility, low-temperature deposition, solution processibility, light-weight, unique charge transport, electronic band-gap tunability, chemical sensitivity and photoconductivity [1,2]. These materials have already been utilized in some commercial applications (organic light-emitting diodes, radio-frequency identification tags) with their state-of-the-art characteristics, and they are still expected to perform well and excel in a number of fields (bio-sensing, photovoltaic cells, flexible electronic devices) [3-5]. Beyond their unique attributes, organic semiconductors are also alluring for investigation of various phenomena spanning hopping charge transport, short-channel effects, exciton diffusion etc [6]. However, in order to examine these behaviors, it is necessary to fabricate/form/confine organic materials into pre-determined configurations.

For the investigation of electronic and optical properties of new organic materials and transport characteristics of novel device architectures, hybrid organic-inorganic electronic devices are excellent testbeds. The hybrid nature enables utilization of well-established fabrication methodologies, which results in devices with reliable fabrication and minimal device to device variation. Typically, the organic component of these devices is the subject of inquiry, however their compatibility with the processing techniques of the inorganic matter is a challenging endeavor. In this thesis, a variety of fabrication procedures is followed in order to produce state-of-the-art hybrid organic-inorganic nano-electronic devices. The main novelty is the decrement of at least one dimension, with the help of nano-structuring technologies, to a level where interesting phenomena occur.

When confined to one-dimension, organic semiconductors present unique opportunities in terms of optical and electrical features [7]. Since exciton diffusion and electron transport characteristic lengths can be up to tens of nanometers, organic (π -conjugated) wires with diameters below 100 nm are especially interesting to study [8]. Naturally, there are a number of structural factors, such as uniformity, packing density, accurate scaling, that could improve investigation of the nanowires. From that perspective, the manufacturing methodology also becomes important. This thesis comprises a fabrication procedure to form a silicon-based template with horizontally lying nano-channels that provide direct examination of organic nanowires. Atomically precise control over the final dimensions allow to form a few nanometer wide nanowires without size variation over tens of micron long ranges. Fluorescence from organic dye nanowires that run more than 100 micron is measured. However, beyond organic molecules, this template could also be used for other inorganic materials.

Electronic transport in organic semiconductors are also widely investigated. Main device architecture is 3-terminal organic field-effect transistors where charge transport is modulated via gate field [9]. Performance of these transistor can be improved by high-mobility organic semiconductors. However, it is also greatly affected by the device structure. Thin-film transistor theory suggests that the performance parameters, such as the current density and the cut-off frequency, increases drastically as the channel length decreases [10]. However, this is not very straightforward to establish because there occurs a phenomenon with short-channel lengths, where the charges experience large drift between two electrical contacts, and they are exempt from the gate electric field [11]. Therefore, it is crucial to confine the organic semiconductor in three-dimensional framework where the gate surrounds the organic polymer in order to have full effect. A vertical organic field-effect transistor (VOFET) that has gate electrodes around the organic polymer nano-pillars are fabricated and presented in this thesis, as well.

Another novel approach towards reducing/minimizing the short-channel effect is to force the charge carriers to enter the organic system via only near the dielectric interface. The main problem with short-channel transistors comes from unintentional injection of charges from the electrodes away from the gate field-effect. However, as the injection window gets thinner, charges lose their immunity to gate modulation and the current can be drastically switched. For this purpose, a VOFET with a bulk current stopping mechanism is also introduced in this thesis. The device utilizes highly doped

silicon nano-pillars as the gate electrode and it has an insulating layer, on the bottom electrode, that compels charge injection near the gate pillars only.

1.2. Outline

The composition of the thesis goes as follows. Theoretical fundamentals for organic electronics and organic field-effect transistors are first explained in Chapter 2. In addition, a short overview about fabrication methodologies for one-dimensional organic nanowires is also given in this chapter. Chapter 3 gives a brief overview of the techniques, equipment, and recipes that are used throughout the rest of the thesis. A number of lithography, thin-film deposition and etching procedures are employed at different steps depending of the need. In Chapter 4, an unprecedented fabrication strategy is created in order to obtain high-density arrayed silicon nano-crystals. Two distinctive lithography methods, displacement Talbot lithography (DTL) and edge lithography (EL), is combined with a series of wet-etching steps in order to form eventual nano-structures. All three dimensions of the nano-crystals measure below 15 nm with a confinement goal towards zero-dimensionality. Using a similar fabrication procedure, a silicon wafer with nano-channels is produced in Chapter 5. The nano-channels run hundreds of microns along the substrate without variation in width (< 25 nm) and opening (< 10 nm). They are used to manufacture nano-wires, 1D confinement, of fluorescent organic dyes. In Chapter 6, an approach for a 3D confined vertical organic field-effect transistor (VOFET) is designed. The organic semiconductor for this type of devices has a shape of a disk with radius and thickness of hundreds of nanometers. The shape is constructed via plasma etching and the drawbacks of this procedure are demonstrated. Chapter 7 explores a completely different scheme for fabrication of a VOFET with transistor channel lengths below 100 nm. With the help of multiple nano-pillars as a single transistor gate and an insulating layer partially covering the bottom electrode, undesired short-channel effects are reduced.

In summary, a variety of fabrication processes leading to diverse hybrid devices are explored in this thesis. Usage of both organic and inorganic materials for examination presents a wide range of possibilities for the final nano-structured designs.

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Chapter 2 Theoretical Background

The basic motivation behind this thesis is to fabricate and study organic semiconductor-based electronic devices. Within this chapter, theoretical background is provided in order to give fundamental insights for the following chapters. Mainly, a qualitative description of organic semiconductors is given, the working principles behind (vertical) organic field-effect transistors are reviewed, and significant properties and fabrication procedures of organic nanowires are discussed.

2.1. Organic Electronics

Interest in the usage of organic materials as part of electronic devices has been increasing, especially during the last two decades, as their unique capabilities are more and more explored [1,2]. While silicon is the king of the inorganic electronics world, the main advantage of organic semiconductors (OSCs) lies in their electronic flexibility [3,4]. It is not only achievable to fabricate brand new OSCs, but it is also possible to chemically modify existing materials to improve their characteristics [5,6]. The ability to manufacture semiconductor components, which could have a variety of bandgaps and mobilities, translates into application-specific materials synthesis [7]. This possibility pushed the development of this field so far that there are already a vast number of organic semiconductors commercially available [8]. Beyond the materials span, a part of this progress made the cut towards direct utilization in daily-life electronic devices, examples of which are organic light-emitting diode (OLED) displays and organic radio-frequency identification (RFID) tags [9,10]. Furthermore, organic electronics holds even more potential, considering that their properties involve solution processability and physical flexibility [11]. When these aspects are combined with appropriate device structures, such as flexible substrates, state-of-the-art electronic devices and systems, such as flexible panel displays and flexible organic transistors become feasible [12,13].

2.2. Organic Semiconductors

When describing inorganic semiconductors, the simplest picture is to consider a fully occupied valence band, fully unoccupied conduction band, and an energy band gap that separates the two, with the mid-point being the Fermi level (Figure 2.1) [14]. Naturally, this description of semiconductors, which also portrays insulators under general circumstances, holds only for temperatures close to or at absolute zero. Unlike insulators, semiconductors have a relatively small energy band gap that can be overcome at finite temperatures due to thermal activation of the charge carriers from the valence band to the conduction band. It is also possible to introduce external elements by means of doping the semiconductor material in order to create an impurity level that is either above or below the Fermi level (either close to the conduction band or the valence band). This procedure effectively decreases the band gap, making it more conductive than the

intrinsic semiconductor. If the impurity level is close to the conduction (valence) band, then the semiconductor becomes n-type (p-type).

Figure 2.1 Schematic band diagrams of a) insulators, b) semiconductors at 0 K, c) semiconductors at 300 K, d) n-type doped semiconductors at 300 K and e) p-type doped semiconductors at 300 K.

The above depiction is only applicable to semiconductors that are periodic along the whole crystal structure, allowing delocalization of charges and formation of bands. Only a few molecular organic semiconductors (pentacene, rubrene) can exhibit such periodic nature under special conditions and they are quite difficult to produce, not to mention the cumbersome process required to utilize them in any device architecture [15,16]. The theory differs for OSCs and it includes energy levels (highest occupied molecular orbital, HOMO, and lowest unoccupied molecular orbital, LUMO) that are localized at each molecular position [17]. Depending on the relative orientation of the molecule with respect to its adjacent neighbors, partial delocalization of the charges could occur (Figure 2.2).

Figure 2.2 Schematic (de)localization of charges regarding molecular arrangement.

The elementary units of conduction in organic semiconductors are molecules, unlike their inorganic analogues where atoms are the fundamental components. OSCs are formed of π -conjugated molecules where unsaturated carbon atoms with alternating double bonds are present [18]. This formation culminates in delocalization of π -electrons along the molecular orbitals that emerge due to overlapping valence orbitals of the carbon atoms. When large amounts of such molecules are brought together, a specifically packed network is formed by the mobile electrons in order to further extend their orbitals. A general arrangement towards lowering the energy of the system is a face-to-face orientation in which the molecular orbitals overlap (see Figure 2.2). Under the influence of a potential difference and the presence of free carriers, a flow of electrons (holes) through the entire structure is established, while minimizing the potential barrier that could hinder conduction.

OSCs can be divided into two general subgroups: molecular and polymeric. As mentioned above, molecular semiconductors can form crystals when evaporated under certain circumstances [15,16]. On the other hand, polymers are deposited through solution processing, which makes them a low-cost option for device fabrication [19]. Although polymers, as their name suggests, could form chains of a few monomers, they fail at achieving as good ordering as molecular crystals. Polymer chains are usually stranded around each other without any definite arrangement. This forms a potential barrier among the chains, delocalizing charge carriers to the fibers. Therefore, there are more complicated percolation paths for the charges to follow in polymeric OSCs than in molecular ones. Therefore, the mobility tends to be orders of magnitude higher in molecular organic crystals.

Regarding the molecular orientation in polymer semiconductors, a number of studies is reported [20,21,22]. The most important aspect is the interaction between the molecules and the dielectric surface during deposition. Depending on this interaction the polymer could grow in various orientations, changing the overall mobility of the device. A well-established example of this is poly(3-hexylthiophene) (P3HT). Kim *et al.* showed that when the surface of the SiO₂ dielectric is modified with self-assembled monolayers (SAMs) with different end groups of amines (-NH₂) or methyls (-CH₃), the molecular ordering of the P3HT changes from edge-on (chains perpendicular to the substrate) to face-on (chains parallel to the substrate) [20]. After annealing, this difference is reflected in the mobility, which is higher in the edge-on case by a factor of four. They stated that the edge-on orientation is mediated by the repulsion between the π -electrons and the polar groups with unshared electron pairs.

Molecular ordering can directly be related to the intrinsic properties of the OSCs. However, it is still of utmost importance for the energy levels of the OSC to be compatible with the other materials in the device, especially with the Fermi level of the metal contacts and the dielectric interface [23]. Generally, good injection of carriers is established if the work-function (Φ_M) of the metal is in close proximity to the HOMO or the LUMO level of the organic material, depending on the conduction type. An energy difference between Φ_M and the relevant orbital could result in contact resistance, and prevent injection of carriers or could produce a built-in potential, stimulating diffusion of carriers. For example, conduction is achieved through the HOMO level for p-type OSCs. In this case, a metal with a work-function as close to the HOMO level as possible is required. When Φ_M is above this value, a Schottky contact appears and conduction is suppressed. In the opposite case, Φ_M below the HOMO level, carriers already accumulate without any external potential applied. In order to prevent any of these circumstances, metals with suitable work-functions must be utilized. However, it is also possible to chemically modify the surface of the metal via SAMs such that the Fermi level at the interface changes to a different value [24,25]. De Boer *et al.* reported that the work-function of evaporated gold is around 4.9 eV, which is at least 0.2 eV lower than the generally accepted values (>5.1 eV) [24]. They modified the gold surface with two different monolayers, 1H,1H,2H,2H-perfluorodecanethiol (-SC₂H₄C₈F₁₇) and 1-hexadecanethiol (-SC₁₆H₃₃), and measured an increase and a decrease in the work-function by 0.6 eV and 0.8 eV, respectively.

Unlike inorganic semiconductors, p- or n- type for OSCs is not the consequence of externally introduced impurities because all OSCs can intrinsically conduct both electrons and holes with comparable mobilities. The type is rather defined by how easily the charge carriers can be injected from the electrodes into the OSC [26, 27]. However, an OSC usually has better conduction properties through one of the levels, and they are referred to as p- or n- type depending on which level shows dominating transport characteristics. Pentacene and rubrene are widely known examples for p-type molecular OSCs. As mentioned before, they can be deposited in the form of single-crystals to exhibit electronic mobility values of $58 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (for pentacene at 225 K) and $18 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (for rubrene at room temperature) [15,16]. For polymer OSCs mobility values above $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are rarely observed. A recent study by Chen *et al.* presented a new p-type OSC of diThiopheneIndenoFluorene-BenzoThiadiazole (TIF-BT) that could approach a mobility of $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [28]. Apart from that, the commonly investigated p-type polymer OSCs (P3HT, PBTTT) can have mobilities on the order of $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [29,30]. An outstanding molecular example of an n-type OSC is the C_{60} molecule. Even though it does not form a single-crystal, it is reported to show mobilities up to $6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [31]. Derivatives of perylene- and naphthalene- tetracarboxylic diimide (PTCDI and NTCDI) molecules are additional examples that show mobilities above $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [32,33]. Diketopyrrolopyrrole (DPP) based p-type polymers are demonstrated to show mobilities above $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [34].

Even though molecular n-type OSCs are reported to exceed mobility values of $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, their performance highly depends on the environment. The high energy LUMO levels of these molecules render them vulnerable to ambient conditions. When oxygen and/or water molecules intermix or react with the active region of the device, they form impurities of excess potential barriers, thus decreasing the mobility by at least an order of magnitude [35]. In addition, electronic devices that rely on electron conduction through the OSC employ metals that have low work-functions, such as aluminum (-4 eV), magnesium (-3.6 eV) and calcium (-2.9 eV) [36]. Those metals cannot withstand ambient air without oxidizing partially or completely. Therefore, self-assembled monolayers for dielectric surfaces, capping layers for metal electrodes and protective coatings for the overall device are applied [26, 27, 36].

2.3. Organic Field-Effect Transistors

In a lateral organic field-effect transistor (OFET), the gate electrode is separated from the organic semiconductor by a dielectric layer, and together they always form a stack [37]. The source and drain electrodes, on the other hand, are only required to be in contact with the OSC, and are not necessarily touching the dielectric part. Ideally, when a voltage bias is applied between these two electrodes, while the gate and source are at the same potential, only a negligible number of carriers is expected to flow (Figure 2.3). As the potential difference between the source and gate increases, more and more carriers are induced in the OSC in close proximity of the dielectric interface. Under this circumstance, non-zero source-drain bias introduces significant current flow through the semiconductor. In most cases, the carrier concentration only develops within the first few monolayers of the OSC near the dielectric surface [38].

Figure 2.3 Schematic representation for accumulation of charges for p-type OFET when gate and source voltages are the same (left) and when gate voltage is approaching drain voltage (right).

The required magnitude of the potential bias differs depending on the geometry and materials choice. The main parameters are the distance between the source and drain contacts (transistor channel length, L), the dielectric layer thickness (d), and the quality of the dielectric material (dielectric constant, k) [39]. However, unlike the magnitude, the sign of the potential difference is simply determined by the type of OSC. For p-type (n-type) semiconductor, negative (positive) potential must be applied to the gate relative to the source so that holes (electrons) accumulate at the OSC-dielectric interface.

The OFET operation is characterized by two different regimes, depending on the drain-source voltage (V_{DS}) at a fixed finite gate-source voltage (V_{GS}), the linear regime and the saturation regime [40,41]. In the first regime, as V_{DS} is changed from zero to finite values, the current increases linearly and the current-voltage curve (I_D - V_{DS}) follows

Ohm's law with a certain resistance. As V_{DS} approaches the fixed V_{GS} value, the current starts to saturate. Ideally in this second regime, after V_{DS} exceeds V_{GS} , the current does not depend on the V_{DS} anymore. Below are the equations that explain the linear (Eq. 1) and saturation (Eq. 2) regimes.

$$I_D = \frac{\mu CW}{L} \left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (1)$$

$$I_D = \frac{\mu CW}{2L} (V_{GS} - V_{th})^2 \quad (2)$$

When the characteristics of an OFET are measured, fittings must be performed well within one of the two limiting regimes. Errors can be made if the intermediate (transition) regime is used in the calculation. Recently, Choi *et al.* also reported that if the I_D - V_{GS} or $\sqrt{I_D}$ - V_{GS} transfer curves, that deviate from the ideal cases, are not treated carefully, they could result in miscalculation of the mobility by at least an order of magnitude different from the intrinsic (real) value [41]. In addition, they mention that the linear regime is more suitable for mobility calculations, because the saturation mobility is more susceptible to errors, especially if it depends on the carrier concentration. They also introduce the new concept of measurement reliability factor, which translates into how much the real electrical performance alters from the calculated mobility value.

The common transistor characteristics involve three merits [42]:

- 1) Maximum current density: the saturation current divided by the effective cross-section of the transistor.
- 2) ON/OFF ratio: ratio between saturation currents at $V_{GS} = V_{DS}$ and $V_{GS} = 0$.
- 3) Operation frequency: maximum frequency at which the transistor can switch between ON and OFF current values.

The performance of an OFET as defined by these criteria is primarily affected by two parameters, the mobility (μ) and the transistor channel length (L) [43]. The current density and the ON/OFF ratio are proportionally related to μL^{-1} and the operation frequency depends on μL^{-2} . As it becomes obvious, an organic semiconductor with a

high mobility and a short transistor channel length contributes to improvement of an OFET. However, those parameters are not straightforward to change, especially the mobility, since it is an intrinsic characteristic of the OSC and its morphology. It requires costly and time-consuming methods, such as e-beam or nano-imprint lithography, to fabricate channel lengths below 100 nm for a conventional OFET. Furthermore, organic transistors with sub-100 nm channel lengths suffer from short-channel effects [44].

Short-channel effects occur due to an enhanced electric field between the source and the drain electrodes [45]. In a normal transistor, the dielectric layer thickness must be much smaller than the channel length. However, with short-channel devices, these two dimensions start to become comparable. As this happens, bulk organic material that is not in close proximity to the dielectric-organic interface, does not respond to the gate electric field and contains charges that drift strongly due to a high source-drain electric field. At this condition, the charge transport adapts into a gate-independent space-charge-limited current (SCLC) regime. The current does not saturate regardless of the V_{GS} and V_{DS} values and it follows a power law given by the following equation [46].

$$J_D = \frac{9}{8} \epsilon_0 \epsilon \mu \frac{V_{DS}^2}{L^3} \quad (3)$$

The short-channel phenomenon also depends on the energy levels of the OSC and work function of the metal. For an ideal OFET, it is a requirement that these two parameters match. However, this demand is disadvantageous for short-channel transistors since it stimulates formation of a depletion layer by eliminating its contact resistance. Hirose *et al.* showed that energy level mismatch between the metal and the semiconductor diminishes preemptive diffusion of carriers into the system and allows regular OFET operation [47]. In their study, they create OFETs with channel lengths as small as 30 nm and use pBTTT (-5.1 eV) as the semiconductor with modified (-5.3 eV) and as-deposited (-4.9 eV) gold contact electrodes. The conduction mechanism follows SCLC behavior for the OFET with modified gold, while the as-deposited gold electrodes form a Schottky barrier and tolerate only a small number of carriers to flow at low gate voltages (Figure 2.4). Even though the maximum output current is lowered by half, it can be seen as a small cost to enable conventional transistor operation with short-channels.

Figure 2.4 Change in transport characteristics depending on the work function of the metal contacts reported by Hirose *et al.* [47]. Regular transistor operation, -4.9 eV (left) and gate independent transport (right).

2.4. Vertical Organic Field-Effect Transistors

Even though it is possible to exploit high-cost structuring in order to investigate fundamental properties of the OFETs with shorter channel lengths, organic electronics eventually requires easy-to-produce device geometries for low-cost and large-area utilization [48]. Vertical OFETs (VOFETs), where the transistor channel length is defined by the active organic layer thickness, are promising candidates towards applications with area restrictions [49]. A vertical device geometry also brings along the advantages of low operation voltages and high output currents [50]. There are already a number of designs in this field, yielding transistor performances that competes with lateral OFETs [51,52].

It is important to note that although the accumulation of a sheet of charges at the dielectric-organic interface is the general mechanism for OFETs, some VOFET architectures introduce new phenomena where the conduction is wielded by more complex charge transport paths [53,54]. For example, Kleemann *et al.* fabricated devices with stacked source and drain contacts on a thin organic semiconductor layer that rest on a gate dielectric (Figure 2.5) [53]. Although there exists a direct path from source to drain away from the dielectric interface, the gate field manages to accumulate charges under the source contact, triggering an increase in the conduction. They studied the operation characteristics for both p-type and n-type using pentacene and C₆₀

respectively, and achieved ON/OFF ratios as high as 10^6 and mobility values in the order of $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (Figure 2.5).

Figure 2.5 Vertical OFET without a gate dielectric from source to drain (top) reported by Kleemann *et al.* [53]. Transfer characteristics for n-type (left) and p-type (right) materials.

Most common VOFET designs still aim to maintain a two-dimensional conduction path over the gate dielectric [42,55]. Vertical transistors with their gate electrode running along the entire height are called step-edge VOFETs (SE-VOFETs) [56]. In a step-edge architecture, the source or the drain makes contact at the bottom of the edge, while the other is at the top, and charges are accumulated at the surface of the step-edge enabling transistor operation. Johnston *et al.* reported a step-edge transistor fabricated on a silicon substrate by etching interdigitated trenches [57]. This procedure allowed them to use silicon directly as the gate material. Their SE-VOFET operates at only 1 V and still supplies a current density of 40 mA cm^{-2} , which is enough to drive an OLED. However, their structuring scheme starts by patterning of the interdigitated resist by e-beam lithography, a high-cost, slow process. In Chapter 7, fabrication of a novel SE-VOFET, where a silicon substrate is etched and used as the gate material, is explored. However, in this case, silicon is etched in the shape of nano-pillars and an organic material surrounds them. In Chapter 6, another VOFET design in which the organic material is patterned as nano-pillars with a surrounding gate is produced.

Although VOFET technology is relatively new, there are already reports where fabrication on flexible platforms is achieved. Uno *et al.* reported an SE-VOFET design

that utilized polyethylene-naphthalate (PEN) as the flexible substrate and patterned step-edges on it by lithographic process with SU8 photoresist [58]. Sputtering metals at the step-edges enabled their functionality as the gate electrodes. High switching frequencies (up to the MHz range) and high ON/OFF ratios of 10^6 were realized from their design, using dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) as the OSC.

2.5. Organic Nanowires

Beyond the afore-mentioned transistor architectures where the conduction mostly happens in a two-dimensional (2D) plain, there is also a branch of organic electronics exploring one-dimensional organic nanostructures [59,60]. When the radial dimension of a bulk OSC is decreased in a controlled manner, while the packing order and/or the crystallinity is protected, the charge transport evolves into a unique regime [61,62]. In other words, as the probability for the charge carriers to percolate and to be affected by the surrounding conduction paths is minimized, the collective transport becomes more efficient.

Several techniques have been investigated towards achievement of organic nanowires that could surpass the characteristics of thin-film organic devices [63,64]. It is most favorable to force the growth of the nanowires into a self-assembly process since the organic molecules already tend to pack in such a fashion that the molecular orbitals are aligned (overlapped) and the delocalization is extended [65]. Some methods suggest patterning of pre-grown thin organic films by means of lithographic processes [66]. However, in those cases, nanowires inherit the pre-defined packing order and lose the possibility to form the most useful structure.

An example of this process is solution-phase self-assembly in which the organic nanowires are produced within the solution before deposition onto a substrate [67,68]. The process relies on the temperature-dependent solubility of the OSC. An organic material, that does not dissolve in a specific solvent at room temperature, becomes soluble at elevated temperatures. After the OSC is dissolved, depending on the cooling speed of the system nanowires with different dimension can be realized. Additionally, a non-solvent could be included in the solution as another parameter to increase the range of dimension. Despite these advantages, solution phase self-assembly lacks the ability to align the nanowires for further applications and characterization.

Similar assembly can also be stimulated in vapor-phase within quartz tubes that have a temperature gradient [69,70]. When an organic material is sublimed at the high temperature side of the tube and transferred to the cooled side with a vapor stream, molecules start to form highly crystalline nanowires around the nucleation points. Even though high mobility wires can be achieved with this growth technique, it is a cumbersome procedure to manipulate wires into functional devices.

Electrospinning is another well-studied method that can deliver extremely long nanowires [71,72]. In this approach, a high voltage is applied between the metallic needle of a syringe containing the organic polymer and the collector substrate. Fluid jet bursts from the capillary and are randomly spins onto the system. A single fiber from the collection can be separately characterized by mobilizing the needle and the collector. However, it still requires cumbersome labor to integrate nanowires with high alignment and accurate positioning.

Template-assisted assembly methods, apart from the afore-mentioned ones, present direct applicability to electronic circuits [73,74], because templating employs pre-defined molds with a desired pattern. Solution-deposited organic semiconductors could also follow this pattern and assemble freely in the confined space [75]. This technique does not hinder favorable energetic ordering and could result in a nicely packed organic matrix. Anodic alumina (AAO) is a commonly utilized hard template that has vertical nanopores with densities as high as 10^{11} per cm^2 [76]. The dimensions and the density of the pores can be tuned during fabrication facilitating a vast range of sizes. One way to form nanowires is to spin-coat the polymer on the membrane [77]. Another manner is to place the template on a substrate onto which the organic substance is spin coated. Heating it in an oven enables capillary forces to fill the pores of the template by melting the polymer [78]. The alumina can be etched away by immersing it in a NaOH solution after the membrane is fully loaded. The template can directly be used for vertical transistor devices, but it is not straightforward to use the organic nanowires for other applications. Below is a comparison table created by Vincent Teernstra (my former master student), reviewing various aspects of 1D organic nanowire fabrication techniques (Table 2.1) [65]. In Chapter 5, a new templating method is introduced where a silicon wafer is processed to obtain massively parallel trenches with dimensions below 10 nm.

	Morphology	Typical dimensions	Packing	Form of alignment	Uniformity	Throughput
Template-assisted methods	nanorods nanotubes	d = 50 nm L = 150 nm	good	massive	moderate	Moderate - high
Electro-spinning	nanofibers	d > 50 nm L = mm up to several km	decent	none (or massive)	bad	high
Lithography	nanowires nanoribbons	d > 10 nm L > 100 nm	decent	individual (or massive)	good	low (or moderate)
Self-assembly (solution-phase)	nanowires nanoribbons	d > 20 nm L > 100 nm	good	none	bad	high
Self-assembly (vapor-phase)	nanowires nanobelts nanoribbons	d > 100 nm L > μm	good	none	good	low

Table 2.1 Comparison of organic nanowire fabrication techniques created by Teernstra [65].

2.6. Conclusion

In this chapter, general overview is given about organic semiconductors, lateral and vertical organic field-effect transistors, and organic nanowires. First, electronic properties of organic molecules, delocalization of charges among adjacent molecules and importance of molecular ordering is discussed. Definition for p- and n- type for organic semiconductors with various examples are also briefly explained. After elaborating on transistor mechanism and characteristics, architectural parameter for improved performance is established to be the channel length. However, below 100 nm short-channel effects impair the transistor operation due to high bulk currents and decreased ON/OFF ratios. In Chapter 6 and Chapter 7, vertical designs with thin active layers are fabricated and characterized. In this chapter, fabrication methodologies for fabrication of organic nanowires are also reviewed. Template-assisted technique with its good packing, alignment and uniformity is discussed to be an ideal candidate for organic nanowire fabrication. Chapter 5 presents a new template that enables decrement of wire radius while having high throughput.

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Chapter 3 Fabrication Details

Throughout this thesis, micro and nano fabrication procedures have been followed to eventually obtain nano-structures and devices. In this chapter, the basic equipment and working mechanisms of less common techniques are explained. However, further details about each fabrication procedure will be given in the corresponding chapters. Therefore, the intention of this chapter is to provide the general experimental background necessary to understand the rest of the thesis.

3.1. Lithographic Processes

Three different lithography technologies utilized in this thesis, are explained below.

3.1.1. PhableR Tool – Displacement Talbot Lithography

In Chapters 4, 5 and 7, the fabrication schemes start with a relatively new lithography technique that was invented last decade, displacement Talbot lithography (DTL). DTL is a method to create a periodic grating on a photoresist by utilizing a phenomenon known as the Talbot effect [1,2]. When a mask with a grating pattern is illuminated by a monochromatic wave plane, a self-image of this pattern forms at a specific distance (d) from the mask. This self-image reappears periodically also at multiple integer units of this distance. There are two basic formulas describing the relation between the distance (d), the wavelength (λ) and the grating periodicity (p)

$$d = \frac{2p^2}{\lambda} \quad , \quad \lambda < p \quad (1)$$

$$d = \frac{\lambda}{1 - \sqrt{1 - \frac{\lambda^2}{p^2}}} \quad , \quad \lambda \approx p. \quad (2)$$

It should be noted that at first fraction ($d/2$), an exact self-image of the grating is repeated with a lateral shift of $p/2$.

It is difficult to make use of the Talbot effect, since it requires very accurate positioning of the substrate. However, the DTL technology minimizes this problem by moving the substrate one Talbot period (d) back and forth in the direction normal to the grating (see Figure 3.1). This process diminishes the problem of positioning, in fact the distance from the grating mask turns out to be irrelevant, and the only important parameter becomes the exposure time for a fixed laser power density.

For the patterning of lines, a bottom anti-reflective coating (AZ BARLi-II 200) and a thin photoresist (PFI-88 diluted in 1:1 propylene glycol monomethyl ether acetate (PGMEA)) are successively spin coated [3]. They are spin coated for 45 seconds at 3000 rpm and 4000 rpm, pre-exposure baked at 185 °C and 95 °C, respectively. Using the DTL technology periodic line patterns in the photoresist with linewidths in the range 75 nm –

125 nm with a fixed periodicity of 250 nm are realized (Figure 3.2). In the PhableR 100 Eulitha machine, the best result is obtained for 100 nm lines for 75 s exposure time, 20 s target cycle, 1 mW cm⁻² laser intensity, 3 μm DTL-range, 65 μm DTL-gap and 1 pre-cycle step.

Figure 3.1 Schematic presentation for working mechanism of DTL, Solak *et al.* [35].

It is also possible to expose the resist a second time after rotating the wafer at a desired angle to create dots with different shapes and periodicity. Naturally, the exposure time for each step must be decreased in order to avoid over exposure. Engineers at the MESA+ Institute for Nanotechnology found the precise time required as 49 seconds in order to make excellent round dots under 90° angle (see Figure 3.2) [4]. In Chapter 6 of this thesis, the same exposure time is applied but by applying a rotation of 60° between the two line exposures. This forms closely packed hexagonal lattice of nano-pillars so that the distances between the first and second nearest neighbors are comparable. After exposure of both lines and dots, the resist is baked at 120 °C for 2 minutes and developed in Olin OPD 4262 developer for 1 minute. Finally, the wafers are rinsed in DI water and blow dried with nitrogen.

Figure 3.2 SEM images of single and double exposure in DTL. Single exposures of a) 75 sec and b) 95 sec result in 100 nm and 85 nm wide lines, respectively. Double exposure with angles of c) 60° and d) 90° result in hexagonal lattice and square lattice dots with radii around 90-125 nm and 90 nm, respectively. All scale bars are 250 nm.

3.1.2. Photo Lithography

In order to make metal electrodes for lateral OFET and VOFET devices in Chapter 6, a conventional photo lithography (PL) process is used. For both cases, a self-assembled monolayer (hexamethyldisilazane, HMDS) is first spin coated at 4000 rpm in order to improve adhesion of the photoresist. After that a commercially available positive resist, Olin 17 (Olin OIR-907-17, Arch Chemicals Inc.), is spin coated at 4000 rpm for 30 seconds and baked at 95 °C. Exposure is performed with intensity and time settings of 12 mW cm⁻² and 4-5 seconds in an EVG 620 UV mask aligner.

3.1.3. Electron-Beam Lithography

Although the DTL method is utilized to make lines at the sub-micron, electron beam lithography (EBL) is used to increase the distance between the lines for fluorescence studies of organic nanowires, fabrication of which is further explained in

Chapter 5. Hydrogen silsesquioxane (HSQ 6% dissolved in methyl isobutyl ketone, MIBK, Dow Corning Corp.) is used as the resist for EBL. It is spin coated at 4000 rpm and baked at 160 °C for 1 min. Lines on this resist were patterned with Raith 150TWO (Raith GmbH). Parameter settings this patterning are 20 kV acceleration voltage, 120 pA beam current, 10 mm working distance, 150 $\mu\text{C cm}^{-2}$ beam dose, 20 μm aperture and 100 $\times$ 100 μm^2 write-field size.

3.2. Thin-Film Processes

Apart from spin coating resists and organic semiconductors, the growth and deposition techniques used for the dielectric materials and metals are described in this section.

3.2.1. Thermal Oxidation of Silicon

Oxidation of silicon is a well-established process. Throughout this thesis (Chapters 4, 5, 6), thermal oxidation is used for different purposes, however all in the same manner. The dry oxidation process exposes the silicon wafer to oxygen gas at high temperatures (900 °C-1150 °C) in a furnace (Amtech Tempress). The silicon oxide (SiO_2) growth rate is proportional to the square-root of the time [5]. The expected oxide thickness (z) at 900 °C for a given time (t) is as follows.

$$z = 7.75\sqrt{t} - 5.87 \quad (3)$$

As mentioned above, this process results in the growth rather than deposition of SiO_2 . In other words, silicon wafer is consumed to form this layer. The final SiO_2 thickness is 2.22 times larger than the originally consumed silicon thickness. Therefore, only 55% of the oxide actually stays above the original starting point.

3.2.2. Low-Pressure Chemical Vapor Deposition of Silicon Nitride

Silicon nitride (Si_3N_4) is used as a hard mask to which the DTL lines are transferred using reactive ion etching, because in some recipes that are used in this thesis (Chapter 4, 5, 7), the wafers go through high-temperature processes where simple resists cannot survive. Si_3N_4 deposition is performed in a furnace at 800 °C by mixing two gases

of dichlorosilane (SiH_2Cl_2) and ammonia (NH_3). Since it is a deposition process, it grows linearly with time and the rate in our system (Amtech Tempress) is 5 nm min^{-1} . The chemical reaction is given below.

3.2.3. Atomic Layer Deposition of Aluminum Oxide

Atomic layer deposition (ALD) is known to surpass all technologies when it comes to deposit completely conformal layers (Chapter 5, 6). Therefore, it is an excellent process to cover nanostructures without pinholes which could be damaging for electrical measurements. Additionally, aluminum oxide (Al_2O_3) is a high- k dielectric material (~ 9), meaning that thick layers of it can form large gate capacitance while avoiding leakage currents. During thermal ALD, gases are fed into the system alternately, with N_2 purging steps in between. The first gas, trimethylaluminum $\text{Al}(\text{CH}_3)_3$ (TMA), settles on the surface and forms a monolayer due to its self-limiting nature of this process. After purging, water is pulsed to react with the TMA monolayer and to form an Al_2O_3 layer, thus completing one cycle. Below is the chemical reaction that takes place.

This deposition is performed at 300°C with a rate of 0.1 nm per cycle in our system (Picosun). However, the first 10 cycles are not effective because they form nucleation points, instead of a uniform coverage of the substrate. Thus, in order to deposit, *e.g.*, 40 nm of Al_2O_3 , 410 cycles must be performed. The pulsing occurs at a base pressure of $10\text{-}3 \text{ mTorr}$ with water pulse and purge times of 0.2 s and 5 s , TMA pulse and purge times of 0.1 s and 4 s .

Figure 3.3 Etch rate calculation for anisotropic wet etching of silicon. 20% KOH at 20°C (a), 25% TMAH at 65°C (b) and 25% TMAH at 75°C (c).

3.2.4. Electron-Beam Evaporation

Various metals (Cr, Al, Au, Pd, Ti) and dielectric materials (SiO_2 , Al_2O_3) are evaporated using an e-beam evaporation system. Deposition of dielectric materials via evaporation is performed in order to form patterned layers on nanostructured substrates because previously described techniques form uniform coverage over the entire wafer. The rate for each material can be fine-tuned by adjusting the e-beam current and target area. Rates ranging from 0.01 nm s^{-1} to 1 nm s^{-1} are used in this thesis. However, certain limits must be considered for each specific purpose. For example, in Chapter 4, chromium is evaporated in order to reverse the DTL duty-cycle. For that purpose, a minimum evaporation rate of 0.01 nm s^{-1} had to be used. Another example is deposition of metals on top of thin organic semiconductor layers. For this purpose, rates above 0.2 nm s^{-1} are favorable, but 0.5 nm s^{-1} would be optimum. Also, it would be even more helpful to deposit thin layers of dielectric materials for organic layers because the metal atoms are able to punch through the OSC layers and short the VOFET structures. However, a thin dielectric layer could form nucleation points for the metal and stop them from diffusing into the organic matrix [6]. In Chapter 6, this method is used by evaporating 3 nm of SiO_2 layer.

3.3. Etching Processes

Wet and dry etching techniques used to structure the silicon wafers, and plasma etching techniques used to etch thin layers of organic and inorganic materials are explained below.

3.3.1. Anisotropic Wet Etching of Silicon

Silicon wet etching is a widely known method. The two basic chemicals that etch silicon in an anisotropic manner are water solutions of potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) [7,8]. Hydroxyl (OH^-) groups in aqueous solutions are strong enough to break silicon bonds. Since different plane directions have different bond lengths and bond strengths, etch rates differ from plane to plane. The temperature also plays a strong role by giving more kinetic energy to the molecules targeting the silicon. However, in this thesis (Chapter 4 and 5) we utilized room-temperature etching for KOH because its slow etch rate enables nanometer precision

during fabrication. The etch rates of the Si [100] and [111] planes in 20% KOH at room temperature (RT) are roughly 25 nm min^{-1} and 0.5 nm min^{-1} , respectively. The doping concentration also strongly affects the etch rates. For 20% KOH at RT, it takes approximately an hour to etch 10 nm of highly doped silicon in [111] direction. Hence, high-temperature etching with TMAH is used to etch those wafers. Etch rates of 9.9 nm min^{-1} and 4.9 nm min^{-1} are found for 25% TMAH at 75°C and 65°C , respectively. Etched thicknesses in the [111] direction for various time lengths are plotted in Figure 3.3.

3.3.2. Anisotropic Dry Etching of Silicon

A common way to etch silicon with reactive ion etching (RIE) is the Bosch process [9]. Two gases (sulfur hexafluoride, SF_6 and octafluorocyclobutane, C_4F_8) are used in this process. The former (SF_6) is the reactive gas and the latter is the deposition gas. First, the SF_6 is pulsed in the form of a plasma with a directional component towards the wafer for tens of milliseconds, etching part of the silicon. Secondly, the C_4F_8 is applied for tens of milliseconds conformally depositing on the whole substrate. When the SF_6 plasma is administered again, its kinetic energy towards the wafer aims at removing the deposited C_4F_8 and etch the silicon. However, since the plasma is not directed towards the walls of the previously etched part, it cannot remove the C_4F_8 and etch the silicon further in that direction (Figure 3.4). By repeating this cycle, high-aspect-ratio silicon structures can be realized. It is also possible to continuously apply both of the gases, and smoothly etch the silicon. However, this concurrent application cannot etch very deep into the silicon, so it is only used to etch nano-structures with extremely smooth edges. This procedure is exploited in Chapter 7 to make silicon nano-pillars with a plasma etching machine (Oxford PlasmaPro 100 Estrelas). The etching is performed at 0°C , under 22 mTorr chamber pressure and 10 mTorr helium substrate cooling pressure. The inductively and capacitively coupled plasma powers of 800 W and 35 W are used while SF_6 and C_4F_8 gases flow with 30 sccm and 45 sccm, respectively, for 35 seconds.

3.3.3. Isotropic Wet Etching of Silicon Nitride

Si_3N_4 , deposited by LPCVD, is later etched in an 85% aqueous solution of Phosphoric Acid (H_3PO_4) in Chapters 4 and 5. The etch rate at 160°C and 140°C are 1.26 nm min^{-1} and 0.7 nm min^{-1} , respectively.

Figure 3.4 Dry etching processes. a) First etching of silicon via SF_6 plasma. b) Conformal deposition of C_4F_8 polymer on the substrate. c) Second etching with SF_6 plasma. d) Formation of trenches after series of etching-deposition steps. (Bosch process). e) Concurrent formation of SF_6 and C_4F_8 plasma. f) Etched trench after continuous application of plasma.

3.3.4. Reactive Ion Etching of Dielectrics and Resist

RIE is used to etch the Si_3N_4 and BARLi resists in order to transfer the DTL lines or dots to the wafer surface in Chapters 4, 5, 7. This etching is different from silicon etching, because in this process, etching is mostly mediated by forward biasing the plasma with parallel plates. Therefore, there is still, a slight effect towards the side walls of the resist. Two recipes are used for different materials in our system (TEtske) due to their different stiffness' and consequently reactivity to the plasma. Si_3N_4 etching is performed with gas flow rates of 25 sccm CHF_3 , 5 sccm O_2 while BARLi is etched only with 50 sccm flow rate of N_2 gas. Both recipes use 25 W RF power and 10 mTorr pressure. The etch rates are 25 and 30 nm min^{-1} for Si_3N_4 and BARLi, respectively.

3.3.5. (Reactive) Ion Beam Etching of Organic Thin-Films

In order to make organic nanowires in Chapter 5, ion beam etching (IBE) is utilized. The working mechanism of this system (Oxford i300 RIBE) resembles the

previous machine with the option for involvement of reactive atoms. However, in this case the angle at which the beam showers the substrate can be changed. There is also a secondary ion mass spectrometer (SIMS) that counts the atoms. Depending on which atoms are detected, one can tell if the material is completely etched. N,N'-bis(2,6-dimethylphenyl)-perylene-3,4,9,10-tetracarboxylic diimide (DXP) is the organic material that is etched with this machine. In this case, since there was an Al_2O_3 layer under the DXP, detection of aluminum was performed in order to confirm that the surface was reached and that all DXP was depleted. The recipe includes 5 sccm flow of argon gas with a beam current of 50 mA and acceleration voltage of 300 V. Although non-reactive Argon gas is used for DXP etching, reactive oxygen gas is utilized for the shrinkage of BARLi lines while etching of the PFI-88 resist. Unlike argon, oxygen also attacks the walls of the BARLi and ensures linewidth decrement. The oxygen flow used for this purpose is 20 sccm.

3.4. Conclusion

Fabrication details spanning lithographic processes, thin-film methodologies and etching recipes are explored in this chapter. In the following chapters, a number of processes are combined in order to fabricate nano-structured substrates. Chapter 4 utilizes PhableR tool, thermal growth, LPCVD, e-beam deposition, RIE and wet etching processes. Chapter 5 involves PhableR and e-beam lithographies, oxide growth and deposition, wet and dry etching processes. In Chapter 6, photolithography, e-beam lithography, silicon oxidation, ALD, metal evaporation and RIE processes are used. Fabrication procedure in Chapter 7 includes PhableR tool, LPCVD, e-beam evaporation and dry etching recipes.

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Chapter 4 3D-Fabrication of Tunable and High-Density Arrays of Crystalline Silicon Nano-Structures

In this chapter, high-density ordered silicon nano-crystal arrays are fabricated for potential applications in optical sensing and electronics. The top-down process includes two nanolithography methods, displacement Talbot lithography (DTL) and edge lithography (EL), to fabricate the silicon nanostructure array. DTL is utilized to pattern a thin Si_3N_4 layer in two orthogonal resist-patterning steps, and EL is employed as a retraction etch step for the Si_3N_4 pattern. The patterned Si_3N_4 layer acts as a hard mask for anisotropic wet etching and oxidation of silicon substrate. The procedure allows fabrication of silicon nano-crystal arrays with a density of 10^{10} per cm^2 .[‡]

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4.1. Introduction

Silicon quantum dots (Si-QDs) have been intensely studied due to their promising properties and application possibilities in photonics, photovoltaics, spintronics and memory structures [1-4]. Due to the quantum confinement effect, silicon nanostructures are also expected to show increased photoluminescence (PL) [5,6]. Normally, silicon is known to have an indirect bandgap of 1.12 eV [7,8]. However, when quantum confinement comes into play, this indirect bandgap enlarges and top of the valence band and the bottom of the conduction band occurs at the same wavevector, revealing a direct energy gap [9]. This direct gap, therefore, eventually enables radiative transitions, *ergo* higher photoluminescence. However, the size of the nano-clusters should not be as small as possible because the PL intensity roughly depends on the volume [5]. Therefore, clusters should have largest possible volume that can still benefit from quantum confinement effect.

There are different bottom-up and top-down examples to manufacture silicon nanocrystals. Bottom-up techniques are usually based on chemical synthesis with plasma, sol-gel or solution precipitation [10,11]. Top-down methods span (electro)chemical etching, lithography patterning combined with dry and wet etching [3]. For example, Valenta *et al.* utilized e-beam lithography to fabricate silicon nano-pillars via dry-etching, and decrease their sizes with further oxidation and wet etching techniques [12]. In this chapter, a fabrication procedure for high density nano-crystal silicon arrays is explained in detail [13]. Single nano-crystal sizes below 15 nm are realized with (an)isotropic wet etching for potential photoluminescence studies. Additionally, this top-down approach results in a highly-ordered array of nanostructures that are not deep-embedded within a matrix. The procedure resembles a previously published top-down method to make single-crystal silicon nano-tetrahedra structures [14]. Berenschot *et al.* reported a series of anisotropic wet etching steps, followed by edge lithography (isotropic wet etch) on photolithographically defined Si_3N_4 line patterns. The final density in that case was 10^7 cm^{-2} and final dimensions were around 25 nm. However, the limiting factor for the density was photolithography since it was not possible to pattern sub-micron features with conventional UV-contact lithography.

Using displacement Talbot lithography (DTL) instead of conventional lithography, the amount of line patterns on the same area can be multiplied by at least

an order of magnitude [15]. Doubling the duty-cycle of the DTL pattern results in orders of magnitude increase on the final density. This strategy is accomplished here and density is increased by a factor of 1000.

4.2. Fabrication Procedure and Discussion

Nano-crystal arrays are fabricated on a silicon <100> wafer without any external silicon source. Therefore, the ultimate purpose is to etch the wafer in systematic steps such that there are regularly spaced free-standing silicon nano-crystals in stoichiometric silicon nitride (Si_3N_4) matrix. The <100> wafer is first coated with 10 nm LPCVD Si_3N_4 (see Chapter 3.2.2). The purpose of this initial nitride layer is to form a hard mask for the wafer during anisotropic wet etching step. Bottom anti-reflective coating (BARLi) (160 nm) and photo-resist (PFI-88) (160 nm) coatings are spin-coated following the standard procedure given in Chapter 2.1. DTL lines (see Chapter 3.1.1) with different exposure times, *ergo* exposure doses (75 mJ, 85 mJ, 95 mJ and 105 mJ), are applied with a PhableR 100 machine (Eulitha), each resulting in different linewidths and gaps (Figure 4.1). Despite the different dimensions, all doses give lines with straight vertical resist patterns. Differently dosed areas existed on the same wafer in a total of $3 \times 3 \text{ cm}^2$ area. In order to achieve this, a black shadow card with a hole of $1.5 \times 1.5 \text{ cm}^2$ is utilized, exposing a quarter of the original area for each dose. The purpose for having various doses on the same wafer instead of separate wafers is to precisely monitor differences during fabrication under the same conditions.

Since DTL has a limit on the linewidth of the pattern, a reactive ion beam etching (RIBE) step is deployed to shrink the width even more. Etching BARLi and PFI-88 coatings for 3.5 minutes with 20 sccm oxygen in this system causes approximately 40 nm shrinkage, hence increasing the gap in between the lines as much (Figure 4.2). The vertical etch rates for PFI-88 and BARLi, on the other hand, are found to be about 35 nmmin^{-1} and 45 nm min^{-1} , respectively. After RIBE, directional reactive ion etching in another setup facilitated transferring of lines into the Si_3N_4 layer. The same recipe from Chapter 3.3.5 is used but only for 30 seconds. The remaining organic coatings are stripped with 5 minutes oxygen plasma treatment, leaving only Si_3N_4 pattern on the wafer. Naturally, exposed silicon parts among Si_3N_4 lines, start to have interfacial SiON

Figure 4.1 SEM images of resist layer after exposing with various doses, a) 75 mJ, b) 85 mJ, c) 95 mJ, d) 105 mJ.

Figure 4.2 SEM images of the resist width before (left) and after (right) RIBE process.

oxide after this step. Dipping the wafer into 50% hydrofluoric (HF) solution for 10 seconds etches the oxide and reveals bare silicon while only slightly attacking the Si_3N_4 . Before any more oxide compounds grow on silicon surface, the previous step must be immediately followed by anisotropic wet etching. Wafers are immersed into 20% KOH for 5:30 minutes and V-grooves with (111) planes on each side are obtained between the Si_3N_4 lines (Figure 4.4). At this stage, when thermal oxidation on the whole wafer is performed, the so called LOCal Oxidation of Silicon (LOCOS) takes place and silicon

oxide (SiO_2) does not grow underneath the Si_3N_4 lines. Dry oxidation at 900°C for 35 min develops approximately 12.5 nm SiO_2 on (100) plane and 21 nm SiO_2 on (111) plane. Oxidized V-grooves are now protected from Si_3N_4 etchant, 85% H_3PO_4 thanks to high selectivity between Si_3N_4 and SiO_2 . However, before application of 85% H_3PO_4 , 1% HF dip is performed since top of the Si_3N_4 layer could also be slightly oxidized. 13 minutes etching in 85% H_3PO_4 at 140°C removes all of the Si_3N_4 , and silicon along these lines is completely uncovered after another 1% HF dip to remove the native oxide (SiO_x).

Second anisotropic wet etching is subsequently performed with 25% TMAH at 70°C . The reason for using TMAH instead of KOH, at this step, is its selectivity to SiO_2 . Even though high temperature KOH solution could etch silicon as well, unlike TMAH it also severely damages SiO_2 . After 1 min TMAH etching, the grooves are doubled having the same depth inside and outside the oxide layer. Etch rates of 25% TMAH at 70°C for (100) and (111) planes are 300 nm min^{-1} and 20 nm min^{-1} , respectively. Finally, all of the remaining SiO_2 is etched in 50% HF, and a wafer with plain-tooth-saw like pattern is realized. However, V-grooves with atomically sharp bottoms and rounded bottoms exist in an alternating order. This is due to the rounding of the very first V-grooves after oxidation step. Secondary V-grooves did not go through any oxidation process; therefore, they are still sharp from the wet etching. It should also be noted that although the width of Si_3N_4 lines and gaps in between those lines did not have the same size, the eventual doubling of the V-grooves can still be accomplished by adjusting etching times of KOH and TMAH. In other words, 50% duty cycle can eventually be achieved even if the initial duty cycle is different.

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Figure 4.4 First part of the fabrication scheme. a) V-grooves after first KOH etching. b) Oxidized V-grooves after removal of Si_3N_4 . c) Sawtooth configuration after second KOH etching. d) Clean silicon after wet SiO_2 etching. e) LPCVD Si_3N_4 growth on the whole wafer.

Figure 4.3 Second part of the fabrication scheme. a) Developed wafer after Cr evaporation. b) Reactive ion etching of BARC and Si_3N_4 layers. c) BARC lift-off. d) Third KOH etching reveals diamond structure. e) Retraction of Si_3N_4 . f) Oxidation of the surface. g) Wet etching of Si_3N_4 . h) Slow etching of silicon. i) Zoom in to the nano-crystal positions.

eventual doubling of the V-grooves can still be accomplished by adjusting etching times of KOH and TMAH. In other words, 50% duty cycle can eventually be achieved even if the initial duty cycle is different.

The second part of this whole fabrication procedure happens perpendicular to the first pattern (Figure 4.3). Initially, 19 nm of LPCVD Si_3N_4 layer is grown, covering the entire surface. When a BARLi is coated on this structured wafer, it planarizes the surface, making further spin coating and exposure process of PFI-88 viable. As mentioned above, second DTL is performed perpendicular to the first lithography, with exposure dose of 105 mJ. The maximum linewidth that DTL can give is 125 nm. However, for eventual silicon nano-crystals to have equal spacing it is favorable to start with a larger linewidth and retract the nano-crystal positions later. Therefore, a means for reversal of narrow DTL lines is introduced.

After development of the resist PFI-88, the whole resist is flood exposed for 30 seconds. When a thin layer (10 nm) of chromium is e-beam evaporated directionally on top of the DTL pattern, it fills the gaps among the lines. Since the resist was flood exposed before evaporation, further sonication in the developer (OPD4262) removes all of the resist lines, leaving only chromium pattern and reversing the original duty cycle. Firstly, the reason for this developing procedure instead of conventional acetone sonication of the photoresist is that BARLi is also an organic material. Thus, it would also be stripped in acetone. However, resist developer does not attack BARLi, therefore makes this alternative process applicable. Secondly, it is very important that the chromium is evaporated directionally and as slow as possible in order to avoid any contamination on the walls of the PFI-88 resist. Furthermore, thicker layer (20 nm) induces cracks on the chromium lines, thus that is also not advisable (Figure 4.5).

Chromium acts as a hard mask when BARLi and Si_3N_4 etchings are performed in RIE system. However, different parameters from the first patterning are used for both materials. For BARLi, nitrogen plasma for 9.5 min is used (see Chapter 3.3.4) keeping in mind that it has non-uniform thickness over zig-zag pattern. For Si_3N_4 , it is necessary to perform a longer etching than in the first recipe because the Si_3N_4 layer is thicker in this part. But also due to V-grooves and conformal deposition of Si_3N_4 , the thickness at the bottom of the grooves is approximately 1.73 times thicker (Figure 4.6). To avoid any aberration, the etching time is adjusted for double thickness. Because if there remains any Si_3N_4 at the corners of the grooves, in a later step this would hinder wet etching and form new unintentional grooves.

Figure 4.5 SEM images of evaporated chromium with different rates and thicknesses. a) Rate is 0.02 nm min^{-1} and thickness is 20 nm. b) Rate is 0.01 nm min^{-1} and thickness is 10 nm.

Figure 4.6 Thickness variation of as deposited LPCVD Si_3N_4 from plain surfaces to corners. a) Schematic representation of thicker layer at the sharp corners. b) SEM image of the real sample.

After that, chromium and BARLi layers are etched successively in chromium etchant (mixture of perchloric acid (HClO_4), and ceric ammonium nitrate $(\text{NH}_4)_2[\text{Ce}(\text{NO}_3)_6]$ and 99% Nitric Acid (HNO_3). The wafer is also further cleaned with fresh HNO_3 . Interfacial etching of SiON/oxide with 50% HF for 15 seconds is followed by room temperature 20% KOH etching again for 5:30 minutes. This perpendicular etching resulted in peculiar structures due to non-flat (100) surface. Instead of direct V-grooves, as in the first part, diamond like structures are achieved because the limiting (111) planes are running towards inner side of the Si_3N_4 mask when the etching starts from the top. However, this does not advance continuously since V-grooves are again formed but deeper than it would with a flat starting surface (Figure 4.3d). Meeting point of this V-groove with the upper (111) planes is expected to be exactly at the middle point of the starting height of the second part. This depth can be calculated as follows: the initial DTL periodicity is 250 nm. After doubling of the V-grooves, this periodicity is halved, *ergo* 125 nm. The height (h) of the grooves is related to periodicity (p) by the equation below where 54.7 is the angle between (100) and (111) planes.

$$h = \frac{p}{2} \times \tan(54.7) = \frac{125}{2} \times 1.41 \approx 88 \text{ nm}$$

Since the meeting point is half of this value, it should be 44 nm. From the scanning electron microscopy (SEM) images taken at an angle 45° , the depth is calculated to be *circa* 40 nm. Apart from the small error of 4 nm, which could arise due to imperfect doubling of the first V-grooves, close match consolidates the working principles behind the fabrication methodology, especially the possibility of increasing the duty cycle above 50% by chromium lift-off process.

After formation of diamonds, edge lithography by means of isotropic wet etching of Si_3N_4 is carried out. While Si_3N_4 thickness decreases uniformly, it also retracts from the edges with the same amount. The length of this retracted edge determines the final dimensions of the nano-crystals. Si_3N_4 is etched here with 50% HF since it does not attack silicon at all, while 85% H_3PO_4 is not preferable for precise etching operations. The etched length is designed in this case to be approximately 10 nm. It is noteworthy that the thickness of Si_3N_4 is monitored with a plain dummy wafer that underwent through all processes (except the patterning steps) in the same manner. Etching times and thicknesses could be easily compared with ellipsometry measurements thanks to the flat surface. Etch rate of Si_3N_4 in 50% HF is also measured with this dummy and found to be 7.9 nm min^{-1} .

Another dry oxidation LOCOS process at 1050°C for 1 minute oxidized the exposed silicon parts (*circa* 14 nm on (111) plane). High temperature (1050°C) processing is preferred over lower temperatures (900°C) because it is necessary to protect the shape of the silicon nano-crystal without inducing any stress. Oxidation of silicon nano-structures with sharp edges at low temperatures results in even more sharpened form due to uneven oxide thicknesses at different planes. However, at high temperatures SiO_2 becomes less viscous and stress between different planes can be released, and as an outcome conformal oxide layer is attained.

After a short 1% HF dip, the remaining Si_3N_4 is removed by etching in 85% H_3PO_4 at 140°C for 25 minutes. Final anisotropic wet etching of silicon is accomplished by 20% KOH at room temperature. 3 minutes of etching separated the top part of the silicon tips from the whole wafer, eventually rendering free-standing array of LOCOS SiO_2 with embedded silicon nano-crystals within their tips. Those silicon parts have the shape of a tetrahedron with various edge dimensions. SEM images of the final structures can be seen in Figure 4.7. The periodicity and addressability of individual crystals stands

out as excellent features of this fabrication procedure when compared to randomly found, irregularly sized crystals that are fabricated with other methods.

Samples with different last etching times are imaged with transmission electron microscopy (TEM) (Figure 4.8). Although the final etching step proceeds in the [111] direction and the slow etch rate allows fine control of the eventual size, at some locations there are still not fully developed nano-crystals. The main reason for them not to be etched, is considered to be the incomplete removal of the silicon nitride from the convex corners of the silicon. Even a small amount of Si_3N_4 could act as a perfect mask for anisotropic wet etchants and prevent any etching of the underlying silicon.

An interesting outcome from the TEM images is the three-dimensional size decrement of the silicon nano-crystals. Apparently as soon as the KOH enters the amorphous silicon oxide matrix and etches the silicon to its final dimensions, it starts to leak through the gap between silicon and the oxide. This gap is actually a result of the final isotropic wet etchings by 1% HF and 85% H_3PO_4 . They both attack oxide and actually free the silicon within the oxide stems. It also means that the total oxide thickness is smaller at the stems than elsewhere, since it is etched from both sides. Therefore, this crucial knowledge should be considered for any fabrication that aims at fabricating silicon nano-crystals within an oxide matrix.

Figure 4.7 SEM image of the final product – high-density ordered array of nano-crystals embedded within the oxide framework.

Figure 4.8 Final silicon etching and size decrease of the nano-crystals.

4.3. Conclusion

A new fabrication procedure for high-density ordered arrays of silicon nano-crystals is created by combining DTL and EL with (an)isotropic wet etching and deposition steps. The final nanostructures are embedded in a SiO_2 matrix, and has a potential density of 10^{10} cm^{-2} , and they are shown to have dimensions below 15 nm at some locations on the wafer. However, there were still places where silicon remained in the stem of the freestanding nanostructures. The reasons for this variation has been discussed. These nanostructures may find new applications in optical sensing systems in which attachment of bio-molecules vary the photoluminescence spectra via peak shift or signal broadening.

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Chapter 5 Nano-Channel Template for Producing 1D Organic Nanostructures

In this chapter, a method based on a high-quality nanoscale template for patterning 1D organic nanostructures is introduced. The process to create the template is based on anisotropic wet etching techniques, and it is aimed at the formation of lateral nano-channels. The final channel dimensions can reach below 10 nm and are controllable with nanometer precision throughout the process. The template can simultaneously result in aligned, uniform and a dense array of one-dimensional organic nanowires.

5.1. Introduction

One-dimensional organic nanostructures exhibit unique behaviour, such as enhanced charge transport, polarized light emission and high power conversion efficiency compared to their bulk counterparts [1-3]. However, it is challenging to assemble organic materials into one-dimensional structures in a well-defined configuration. Fabrication methods to form nanostructures cover electrospinning, templating, lithography and self-assembly [4-7]. These methods can result in different types of 1D nanostructures such as nanowires, nanotubes and nanoribbons. However, simultaneous control of size, alignment and uniformity is hard to achieve for 1D organic nanostructures. Electrospinning and self-assembly do not result in aligned nanostructures, which are also not uniform at the nanoscale [1,8]. Organic wires can be defined lithographically, but uniform and reproducible results are difficult to obtain for diameters below 50 nm [2,9]. In contrast, templating employs pre-defined mold formation, and thus provides powerful control over the final configuration and morphology [10]. Yet, templates are reliable only if they can pattern wires without deformation. Current templating technologies can form reproducible and identical structures with dimensions as small as tens of nanometers [9,11]. However, control of the template at the nanoscale is still very difficult due to non-uniformity, clogging and mechanical instability.

In this chapter, a novel templating technique is proposed to realize 1D confinement of organic molecules with critical dimensions below 10 nm. The uniqueness of the approach is that the template dimensions can be controlled with nanometer precision. It consists of a multi-step anisotropic wet-etching process of monocrystalline silicon [12-15]. The fabrication process results in a template with aligned lateral nano-channels. The channels have a narrow opening at the top through which materials can be loaded. This feature helps to avoid clogging, and thus resulting in uniform wires. The opening can be made smaller than 10 nm, allowing formation of nanostructures at this scale. The line edge roughness of the channels is decreased below nanometer level and nearly atomically flat surfaces are obtained owing to anisotropic wet etching. These properties are achieved for the entire length of the channels, which are aligned with respect to the silicon crystal orientation. Since anisotropic wet etching affects all channels with the same mechanism and etch rate, the results are reproducible. Furthermore, the dimensions can be controlled at nanometer scale by adjusting parameters in various steps including wet etching, thermal oxidation and atomic layer deposition (ALD).

5.2. Fabrication Procedure

The nano-channel templates are prepared according to the process shown in Figure 5.1 and Figure 5.2. First, a (100) silicon wafer is uniformly coated with a 10 nm Si_3N_4 layer by low-pressure chemical-vapor-deposition (LPCVD), utilized in further steps as a hard mask to protect certain regions from etchants. Line patterns are created in the Si_3N_4 thin film to define the final channel positions. It is important to align these lines along the [110] silicon crystal orientation, because anisotropic wet etching is used in later steps to define the channels.

Figure 5.1 Fabrication scheme. a) A Si_3N_4 line is patterned on top of a (100) silicon wafer. b) The first KOH etch creates Λ -shaped structures. The inset emphasizes the smooth edges, regardless of the line shapes. c) The wafer surface is locally oxidized except at the position of Si_3N_4 line. d) Removal of the lines exposes the top of the ridges. e) The second KOH etch opens grooves inside the first structure. f) A further TMAH etch widens the inner channel dimensions.

Alignment markers corresponding to the precise crystallographic orientation are fabricated with a simple photolithography method, which has been described elsewhere [16]. Using these markers, displacement Talbot lithography (DTL) is applied to define 100 nm wide, 3 cm long lines with a pitch of 250 nm [17]. This simple and reproducible lithography technique results in a 3×3 cm² area of lines (Figure 5.2a). Directional reactive ion etching (RIE) is used subsequently to transfer the above-mentioned pattern into the Si_3N_4 layer. After stripping the remnants of the photo resist in HNO_3 , a (100) silicon wafer has 90 nm wide lines of Si_3N_4 along the Si [110] direction

(Figure 5.1a). The line width is reduced by 10 nm during the RIE process, but this change is not crucial for the rest of the process since width is further decreased by wet etching. The Si_3N_4 lines serve as hard mask for further wet etching. Before anisotropic wet etching, the wafer is dipped into a 1% HF solution to remove the native silicon oxide on the exposed parts. As a highly anisotropic silicon etchant, a 20% KOH solution at room temperature is used for 50 min [18] (Figure 5.3) in order for the flat silicon plateau underneath the nitride lines to reach 30 nm width (Figure 5.2b).

Figure 5.2 SEM images of fabrication steps. All scales bars are 100 nm a) 100 nm wide lines from displacement Talbot lithography. b) Top view of substrate after first 20% KOH etch. Darker regions in the middle of the white Si_3N_4 lines are flat silicon terraces. c) Cross-section image of the substrate after thermal oxidation. d) Cross-section image after removal of Si_3N_4 lines. e) Second time KOH etching and 2 min TMAH etching results in nano-channels. f) After the ALD step the gap size is below 10 nm.

The etch rates of the Si (100) and (111) planes in 20% KOH at room temperature are 25 nm min^{-1} and 0.5 nm min^{-1} , respectively (see Chapter 3.3.1). As a consequence of this first etching, Λ -shaped peaks centred at the position of the lines are obtained (Figure 5.1b). These structures lie along the full 3 cm length of the substrate. The anisotropic KOH etching results in very smooth planar sides (Figure 5.1b inset). The tops of the plateaus at this stage are still completely protected (covered) by the Si_3N_4 lines. Using this advantage, the whole wafer is oxidized at 900°C for 40 min to turn the slopes of the crests into silicon dioxide (Figure 5.1c, Figure 5.2c). The Si_3N_4 lines are removed in a H_3PO_4 solution (160°C), uncovering the silicon at the tops (Figure 5.1d, Figure 5.2d). The etch rate for Si_3N_4 is 1.26 nm min^{-1} and etching was completed within 10 min. Employing the same KOH etch step creates V-grooves inside the crests (Figure 5.1e). Because of the low

etch rate of the Si [111] crystal plane by KOH, the top grooves become very smooth. However, upon using the faster etching TMAH, the surface is etched deeper in order to obtain free-standing silicon dioxide edges (Figure 5.1f). It is not important which etchant (KOH or TMAH) is used to widen the channel, however KOH gives a smoother surface, while TMAH provides fast etching for wider channels. The SiO₂ edges can be used as protective mask for materials deposited inside the channels. After 25% TMAH etching for 2 min at 70 °C, a channel width below 30 nm was achieved while revealing free-standing SiO₂ edges (Figure 5.2e). If desired, the channel dimensions can be decreased in size by means of atomic layer deposition. ALD can uniformly deposit an atom thick layer of a material without closing the gap. We use ALD of Al₂O₃ to shrink the opening with a conformal layer of 3 nm to reach a gap size below 10 nm (Figure 5.2f).

Figure 5.3 SEM images of a substrate after various steps a) Si₃N₄ lines on top the peaks after first KOH etch. b) Grooves inside the big structures after second KOH etch. c) Further widening of grooves by 3 minutes of TMAH etching. d) Final channel formation after ALD process.

5.3. Adjustable Parameters and Minimum Channel Dimensions

Multiple process parameters allow the channel dimensions to be modified at the nanoscale. The first parameter is the first room-temperature KOH etching. From Figure 5.3, it is obvious that the width of the silicon terraces can be manipulated at a nanometer level. The second parameter is the thermal oxidation time, which determines the upper gap width. It is already known that the thickness of a thermally grown oxide layer depends on time with decreasing non-linearity [19]. The temperature used in this process

is 900 °C, and it results in 28 nm hour⁻¹ ((111) plane) growth rate for the first hour. Therefore, the growth of the oxide can be adjusted efficiently at the nanoscale by varying the growth time. This step gives control over the oxide thickness at the edges and gap size [20]. The third significant parameter is the TMAH etching time which provides expansion of the channel cross section (Figure 5.4). The last important parameter is the number of ALD cycles [21]. By only altering the number of cycles, a wide range of channel dimensions is conveniently obtainable. The final channel dimensions are shown to reach a few nanometers (Figure 5.2f). The inner channel diameter is less than 30 nm and the opening at the top is below 10 nm. Most importantly, the channel shape is conserved along the entire substrate owing to silicon crystal alignment. This property is due to the sharp etching profiles caused by KOH and TMAH. However, the dimensions may differ slightly from one channel to the next, caused by the roughness of the first Si₃N₄ lines. Depending on the roughness, the width of the first Si₃N₄ lines changes from point to point. When KOH etchant is used, it etches the fast etching planes at every access point. Therefore, the width of the resulting flat silicon plateau is determined by the narrowest width of the Si₃N₄ line. Yet, the final dimensions of a single channel are very uniform with consistent gap size and diameter along the entire channel length.

Figure 5.4 Controlled expansion of the channel size via TMAH timing. For different etch times the channel dimension is widened with constant etch rate. Free-standing thermal oxide edges on the surface provide further confinement and protection.

5.4. Dye Deposition into the Nano-Channels

To demonstrate that organic molecules can be easily inserted inside the channels, organic dye molecules are deposited. Since the individual fluorescent line structures of a 250 nm pitch line array are difficult to resolve, electron beam lithography

(EBL) is used to form 100 nm wide Si_3N_4 lines with 5 μm separation. The final nano-channel gap size is tuned to be 35 nm to make sure sufficient material could be deposited, thus making fluorescent detection more convenient. It should be noted that Al_2O_3 deposition by ALD is also performed. This layer helps to detect whether the bottom layer is reached during directional etching which is carried out later in this experiment. $\text{N,N}'$ -Bis(2,6-dimethylphenyl)-perylene-3,4,9,10-tetracarboxylic diimide (DXP) is used as the organic material to be deposited by physical evaporation. Approximately 50 nm of DXP is evaporated directly onto the silicon substrate (Figure 5.5a) [22]. The only possible way for the molecules to enter the channels is through the top slit of 35 nm. After deposition, directional IBE is performed to explicitly remove the organics on the outside section of the channels (Figure 5.5b). The angle of incidence for a substrate with ridges can be calculated geometrically. Considering the height of 150 nm and pitch of 5 μm , the highest angle is figured to be 86° , yet 63° is the best option in order to verify removal of organics homogeneously across the entire surface (Figure 5.6). For this step, during the etching process aluminium detection is carried out by means of a mass spectrometer, and the etching is continued until the Al signal saturates indicating complete removal of DXP (Figure 5.7). The recorded detection period is also used for a second time IBE treatment at the opposite side of the channels (Figure 5.5c).

Figure 5.5 Insertion and observation of organic molecules. a) An organic thin film is evaporated perpendicular to the substrate. b-c) Directional ion beam etching helps to remove organic molecules from the regions outside the channels. d) Fluorescence from patterned DXP molecules proves the concept.

Figure 5.6 Angle calculation for directional etching Above picture is designed for highest possible angle. In this case at least half of the space between two adjacent channels must be exposed to beam. Based on this, second time exposure from opposite side will etch the other half. Below schematic shows angle for equal etching from both base and slope surfaces. Angle of 54.7° is fixed and reflected here as angle between [100] and [111] planes of silicon.

As a consequence of the two directional etching processes, the DXP thin film is patterned into wire shapes with a width of 35 nm residing inside the channels. Applied ion beam exposure is set to a dose so that the shadowing SiO_2 edges of the substrate are barely damaged, thus protecting the DXP inside the channels. After the etching procedure, the final (shielded) line formation is visualized by fluorescence microscopy (Figure 5.5d).

It can be seen that organic wires are patterned along the channels. Since the width and height of the wires are only tens of nanometers, resulting fluorescence from these organic patterns are not very bright. In addition, there are also a couple of $6\text{--}7\ \mu\text{m}$ long defects (dark spots) where discontinuity in the fluorescence can be observed. These spots have similar sizes which suggests that there were defects in the lithography defined lines, and those defects caused etching of the substrate forming discontinuity in the channels. Moreover, there exist multiple bright points close to some nano-channels. They are observed also at the other places of the substrate which indicates that they could as well be irrelevant residues. Despite these minor details, the final image clearly represents

hundreds of micron long organic nanowires that are patterned using the proposed template.

Figure 5.7 Aluminum detection during etching process. Aluminum values (counts per second) start to increase when the thickness of organic material is very thin. This is due to the penetration depth of the ions. Since increase in counts does not necessarily mean that all organics are etched, we continue until the signal saturates. At saturation point, it is only etching aluminum and the surface is disposed of organics.

The ion beam etching is violent for fragile organic molecules. Therefore, 1D nanostructures should stay completely untouched when etching is performed. This template structure provides the possibility to protect organic nanowires while assuring uniformity at nanoscale. Free-standing SiO_2 edges help to surround the inner part without causing any clogging along the nano-channels.

5.5. Conclusion

A novel template for patterning of organic materials has been realized. Using anisotropic wet etching of crystalline silicon, near atomically flat surfaces are obtained. This feature could resolve recurrent problems of other templating techniques, such as surface roughness and continuous uniformity over long distances. In addition, a number of fabrication steps can be tuned to affect the final dimensions of the channels with nanometer precision. When this ultra-fine tuning is combined with ultra-smooth

surfaces, the template allows hundreds of microns long and a few nanometers (< 10 nm) wide wires to be realized. Even though, only fluorescence from organic molecules (DXP) are demonstrated as a proof of principle, wide range of materials can be deposited on this template to be investigated.

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Chapter 6 Fabrication and Characterization of Vertical Organic Field-Effect Transistors based on P3HT Nano-Pillars

This work describes the fabrication of vertical organic field-effect transistors that has 100 nm thick P3HT (poly[3-hexylthiophene-2,5-diyl]) nano-pillars with a surrounding gate dielectric (alumina, Al_2O_3) and gate electrode (aluminum, Al) around them. The shape and the uniformity of the P3HT nano-pillars are established via wedging transfer. This method allows safe contacting on top of the pillars without direct evaporation which causes diffusion and degradation of thin polymer semiconductors. However, electronic transport measurements, in contrast to device simulations, show that the gate field does not modulate the charge carriers. Further analysis and fitting suggest that the gate effect is suppressed due to a damaged, low-mobility layer at the circumference of the actual polymer.[§]

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6.1. Introduction

The electrical characteristics of organic field-effect transistors (OFETs) have been improving continuously since significant research is invested on them due to their attractive features such as low-cost fabrication, solution processability and low-temperature processing [1,2]. The main objectives for OFETs to achieve are production of high output currents and operation at high frequencies [3]. For instance, an OFET has to be able to provide current densities in the order of 10 mA cm^{-2} to drive an organic light-emitting diode (OLED) [4]. It is also favorable if OFETs provide such currents without high power consumption. All these characteristics, *i.e.* the performance, of OFETs can be enhanced not only via intrinsic properties like mobility (μ) and packing order of organic semiconductors, but also via device geometry which is primarily parameterized by the transistor channel length (L) [5]. It is already known from thin-film transistor theory that the current density and the cutoff frequency are inversely proportional to the transistor channel length (L^{-1} and L^{-2} , respectively) [6]. In addition, the transistor power consumption scales with the applied voltage (V). In order to maintain the same level of electric field (E) within the transistor, the required voltage decreases with the channel length ($E = V L^{-1}$) [7]. Therefore, excellent transistor performance is expected to prevail as the channel length shortens.

OFETs are commonly fabricated on planar substrates using photolithography techniques, and the channel length is in the range of microns [8]. In order to achieve even shorter lengths (sub-micron), nanolithography methods must be applied, namely electron-beam lithography (EBL). In addition, there is also a fundamental challenge for the contact resistance for OFETs with short channel lengths [9]. The contact resistance that arises due to the small contact area between the electrodes and the organic semiconductor impairs the high charge carrier injection and high transistor performance with it. Therefore, it is also essential that the gate dielectric, *ergo* gate electrode, coincides with the source/drain electrodes over a large area as in staggered architectures [10].

Vertical OFETs (VOFETs) can fulfill the short channel demand easily, since the thickness of the thin-film organic layer defines the channel length [11]. Vertical construction can also completely avoid the contact resistance problem because the source and drain electrodes do not have to shield the field of the gate electrode [12]. On the other hand, it is not a trivial task to make sub-100 nm VOFETs without encountering diffusion of the top metal electrode into the organic layer [13]. If any metal is directly evaporated

onto the organic, shorting the source and drain for thin devices is inevitable. There are already a number of reports where such problems are circumvented by pre-depositing electrodes before any organic material is applied [14].

In this chapter, a soft-landing method is utilized in order to directly top contact an organic nano-pillar device with a surrounding gate electrode. Previously, the same method was studied by Wilbers *et al.* who managed to fabricate vertical organic junctions with organic layer thicknesses down to 5 nm, which did not result in any diffusion of metals thanks to the so-called wedging transfer technique [5]. In their work, the measurements were also successfully fitted with numerical simulations to which real device parameters were submitted. As a continuation of that work, here a VOFET with 100 nm regio-regular poly(3-hexylthiophene) (P3HT) layer is designed and realized using the wedging transfer technique. In contrast to the previous investigation, a gate dielectric and electrode are introduced to generate charge-carriers along the circumference of the organic nano-pillar. Extensive numerical calculations are also made using the ATLAS simulation software.

6.2. Fabrication Procedure

The fabrication of VOFETs starts with a silicon wafer with a 300 nm silicon oxide layer that is grown at 1100 °C for 4:40 hours (Figure 6.1a). On top of the oxide, the bottom electrodes with contact pads are defined by means of photolithography. Titanium (Ti, 1 nm as an adhesion layer) and palladium (Pd, 20 nm drain contact) are e-beam evaporated for these electrodes and a lift-off procedure is applied through sonication in acetone for 30 min (Figure 6.1e). To make sure that there are not any organic leftovers, the substrate is subjected to UV/Ozone for 10 minutes and rinsed with ethanol. After that, an organic semiconductor (P3HT) is spin-coated on the substrate (Figure 6.1f).

The P3HT is dissolved in bromobenzene (boiling point 156 °C) with a concentration of 20 mg ml⁻¹. The solution is heated and stirred at 80 °C for 4 hours and continuously stirred while slowly cooled down to room temperature. Before spin coating and in order to avoid any particle residues, the solution is filtered through a 0.2 µm filter. Spin-coating is done at 1000 RPM spin speed for 1 minute and then the sample is baked at 100 °C for 1 hour. The final annealing step ensures good packing order and crystallinity of the organic semiconductor by completely evaporating the solvent.

Separately from these substrates, another silicon chip with a native oxide is spin-coated with PMMA and patterned with EBL to have dots ranging in diameters (200 nm, 500 nm, 1 μm and 2 μm) (Figure 6.1b). The direct evaporation of 70 nm of palladium is performed while the substrate is water-cooled. This cooling is crucial because metal dots without any adhesion layer could build up some stress and bend after evaporation [7]. Another disadvantage of not having any adhesion layer is that the dots are vulnerable to any strong sonication and might be removed from the surface. Therefore, very gentle sonication (80 Hz, lowest power, 15 min) is performed to maintain high coverage of dots.

In order to perform wedging transfer of the palladium dots, the sample is dipped into a 30 mg ml⁻¹ ethyl acetate solution of cellulose acetate butyrate (CAB) (Figure 6.1c). CAB is a hydrophobic polymer, thus, it does not stick to the silicon without an oxide overlayer [15]. After dipping 1-2 times consecutively, the whole substrate is covered with a thin layer of CAB, but the edges of the substrate are cleansed of CAB by carefully rubbing acetone. Next, the substrate is immersed slowly into Milli-Q water under 45° angle in order to allow the water to spread between the polymer and silicon, thereby, lifting up the polymer and the ultra-smooth Pd dots with it (Figure 6.1d). Finally, the sample with bottom electrodes and P3HT is brought under the polymer inside the water, and the petri-dish is drained by pumping out the water (Figure 6.1g). During removal of the water, extra care must be taken such that the polymer aligns roughly with the sample. Before proceeding to the next step, the samples are dried overnight in a vacuum oven at 120 °C in order to evaporate all the water within the layers. Extra water content may tamper with P3HT ordering or conductivity by introducing defects [16].

The prepared sample is then etched with directional reactive ion etching (RIE) process which eventually removes all CAB from the top as well as P3HT from everywhere except under the Pd disks, since the metal protects the underlying organic layer (Figure 6.1h). It should be noted that plasma undercuts approximately 10 nm, therefore, it does not form perfectly vertical pillars. This undercut is directly related to the etching time, *ergo* the organic semiconductor thickness. Here, 20 sccm oxygen plasma (100 mTorr, 10 Watt) is applied for 60 seconds.

Figure 6.1 Fabrication scheme. a) Plain 300 nm oxidized silicon wafer. b) E-beam patterned palladium disks. c) CAB dipped substrate. d) CAB lift of in water. e) Photolithographically defined bottom palladium electrodes. f) Spin coating of P3HT. g) Landing of CAB with Pd disks. h) RIE defines pillar structure. i) Atomic layer deposition of Al_2O_3 . j) Evaporation of aluminium. k) Spin coating HSQ. l) Planarization of HSQ. m) Etching Al and Al_2O_3 from the top of the pillars. n) Further gold deposition with photolithography.

When the bottom electrode, the P3HT and the Pd disks are stacked, the next steps comprise the deposition of the gate dielectric and the gate electrode. First, an atomic layer deposition technique is utilized and 20 nm thick Al_2O_3 is grown conformally on the substrate as the gate oxide (Figure 6.1i). It also serves as a separation layer between the bottom and gate contacts. Second, 20 nm of aluminium is e-beam evaporated as the gate electrode with two different configurations (Figure 6.1j). For one type, the substrate is rotated during evaporation and circular coverage is ensured (Figure 6.2). As the other type, the substrate is placed under an angle of 45° and evaporation is carried out only on one side of the pillars. The reason for these two different substrate configurations is that the evaporation performed under rotation does not completely cover the sides of the pillars due to the undercut introduced. Therefore, the gate electrode is actually farther than the thickness of the dielectric, meaning that the electric field from the gate is effectively decreased. However, with the evaporation performed with an angled substrate, this problem is overcome and the aluminum makes a direct contact with the gate dielectric leading to a maximum electric field. Although it is not the perfect configuration, since only half of the circumference is gated, it is still expected to perform within expectations.

Figure 6.2 Colored SEM images showing cross sections of the full-gate (a) and the halfgate (b) test devices: P3HT (100 nm, green), Pd top electrode (150 nm, yellow), Pd bottom electrode (20 nm, yellow), Al₂O₃ gate dielectric (25 nm, purple), and Al gate electrode (30 nm, blue).

The evaporation of aluminum is performed without any photolithographic definition, and therefore, the whole surface is covered. Negative photolithography is used to define the gate contact pads after metal deposition because the resist developer which contains tetramethylammonium hydroxide (TMAH) can etch Al (100 nm min⁻¹) as well as Al₂O₃ (1 nm min⁻¹). If lithography was performed beforehand, that would only damage the Al₂O₃ layer. However, applying developer later removes Al and causes the least possible damage to Al₂O₃.

To fully realize and measure the VOFET structure, the top metal disks must be contacted. The areas of the disks are small and there are already two more layers (Al₂O₃ and Al) on top of it. If wire bonding were to be executed, the force could damage the organic layer thickness. Therefore, contact pads for the disks must also be implemented. The Al₂O₃ and Al layer are removed in the following manner. Initially, Hydrogen silsesquioxane (HSQ) is spin coated on the substrate (Figure 6.1k). This forms a planarized layer which has a very small thickness on top of the disks compared to the rest. Later, reactive ion beam etching (RIE) is employed to etch the thin HSQ, Al and Al₂O₃ layers successively and reach the Pd dots (Figure 6.1l,m). During this etching a secondary ion mass spectrometer (SIMS) measures the counts of aluminum, such that a

sudden drop in the curve is recognized as a complete opening of the Pd dots. After this, another HSQ layer is spin coated to restore a thick enough layer to be an insulator between top and gate contact pads. However, this again introduces a thin layer on top of the disks which has to be cleared with a very short (15 seconds) RIE etch (see Chapter 3.3.4). HSQ is normally a soft material, however, when cured at elevated temperatures ($>100\text{ }^{\circ}\text{C}$), it can become an amorphous silicon oxide with good insulating properties. Therefore, the chips are annealed for 1 hour at $100\text{ }^{\circ}\text{C}$. Finally, photolithography is done to define contact pads and 100 nm Pd is e-beam evaporated on top (Figure 6.1n).

6.3. Transport Measurements

Measurements are carried out at room temperature within a vacuum chamber. During the measurements the bottom electrode is kept as common ground while top and gate electrodes were swept. However, there is not any difference if the top electrode is grounded.

Current vs. source-drain voltage (I - V_{DS}) characteristics at different gate voltages are shown in Figure 6.3 (left panel). In this case, the nano-pillar VOFET has a diameter of $1\text{ }\mu\text{m}$. An asymmetrical current is observed with a ratio of approximately ($I_{-2\text{V}}/I_{+2\text{V}}$) 1.8. The injection of charge carriers (holes) occurs at the electrode with higher potential. Therefore, for negative voltages, injection from the bottom electrode takes place. Since the current is higher at $V_{\text{DS}} = -2\text{ V}$, the contact resistance is smaller for this electrode. Larger contact resistance of the top electrode is possibly due to the wedging transfer since there could be a misconnection between some parts of the organic layer and metal disk. Even though the Pd dots are expected to be extremely smooth, the P3HT layers might have a small roughness which could cause a 50% decrease in contact. There is also a possibility that the dots are not perfectly flat due to stress built up during evaporation. In any case, such behavior is not a surprising feature for this type of VOFETs.

On the other hand, gate response of these curves is almost non-existent. It might seem that there is a small gate effect especially for positive applied voltages, but this variation is only due to time dependent drift. This claim can be clearly seen in Figure 6.3 (right panel) where the current vs. gate voltage (I - V_{GS}) curves are plotted. For different source-drain voltages, the current continuously increases even though the gate voltage is swept back and forth. Therefore, the internal change of the transient current is much

larger than the induced change of the p-type channel carriers. Naturally, a constant and small gate leakage is also observed in the measurements, however this cannot cause any continuously changing disturbance as seen in the I - V_{GS} curves.

Figure 6.3 Transport characteristics of VOFET with 1 μm diameter. I - V_{DS} curves for different gate voltages overlap (left). All I - V_{GS} curves at different drain voltages drift in time regardless of the gate sweep (right).

When the magnitude of the source-drain voltage is increased even further (from 1-2 V up to 3-5 V) and the current response with changing gate is measured, it appears that there is a, although extremely small, field-effect (Figure 6.4). The change in the current is almost embedded in the noise level but clear enough to be observed. Additionally, when the gate is swept to positive and negative values, the current response reproducibly increases and decreases, respectively. Therefore, it is safe to say that this is not a drift driven change but really a gate-effect. However, this response is only observed from two devices with diameters 1 μm and 200 nm and gate electrode from an angled evaporation. Furthermore, the gate effect is very small, not even close to one order of magnitude difference. The VOFETs with P3HT material did not work as expected and the reasons for that are explained with the aid of numerical simulations in the following section. The most probable cause for small or non-present gate action is due to high energy level difference between the electrodes and the organic layer. The work function of Pd is 5.2 eV while the HOMO level of P3HT is 4.6 eV. This difference allows a large number of charges to accumulate throughout the whole nano-pillar. It is not possible to clearly observe the gate induced change in the carrier concentration because the space-charge limited current is much larger. This is also known as short-channel effect and it is possible to avoid it by introducing a Schottky barrier at the source electrode, therefore, minimizing the thickness of the dielectric layer and decreasing the bulk area that cannot be manipulated by the gate-field [17].

Figure 6.4 Small field-effect are observed only for two VOFET devices with 1 μm (left) and 200 nm (right) diameters.

6.4. Numerical Calculations

Simulations are performed in a commercially available semiconductor device simulator software called ATLAS (Silvaco Inc.). Since the device under investigation has a nano-pillar configuration, cylindrical symmetry with a 2D mesh is defined in the simulator which takes care of the 3D projection of a 2D slice by rotating it 360° around the zero axis. As for the inner properties of the organic layer, the drift-diffusion model for a Gaussian density of states (DOS) is utilized. Further parameters are given below.

$$\text{Gaussian DOS width, } \sigma = 0.075 \text{ eV} \quad \text{Site density, } N_t = 1.5 \times 10^{26} \text{ m}^{-3}$$

$$\text{Dielectric constant, } \varepsilon = 4.4 \quad \text{Mobility, } \mu = 7 \times 10^{-3} \frac{\text{cm}^2}{\text{Vs}}$$

The mesh is set differently depending on the proximity to an interface. Next to the gate dielectric and source/drain electrodes, the structure is fine-meshed with 1 nm spacing, and it is gradually increased towards the center of the pillar, where the mesh gets as high as 10 nm, both in the vertical and horizontal directions.

Firstly, devices with varying gate electrode dimensions are simulated. Figure 6.5 (left panel) shows how the current changes with respect to the gate voltage for different aluminum thickness. There, it is clearly visible that a very thin gate electrode decreases the field-effect considerably. In addition to that, the position of the gate electrode also makes quite a big difference. When the gate electrode is located close to the source or the drain, it is less effective than when it is positioned exactly in the middle. It should also

be noted that directly evaporated aluminum forms an electrode with decreasing thickness towards the pillar structure (see Figure 6.2Figure 6.1). Therefore, multiple combinations of gate position and thickness must be checked and compared in order to fully understand the observed behavior.

Secondly, another investigation is a damaged layer that lies at the circumference of the nano-pillars. After the wedging transfer is complete, the organic layer is etched with RIE process. In this case, it is suspected that this plasma etching could be damaging to the organic layer. This is not trivial since RIE is already known to undercut the organic semiconductor. To introduce a damaged layer in the simulations, an organic material but with low mobility values is placed at the circumference of the original pillars. Numerical calculations for this damaged layer with different width and mobility values are performed. As it should be expected, wide layers with low mobilities resulted in excessive decrease in the gate response. However, even simulations of such devices did not approach the measured behavior. Only if the layer has a mobility value of an insulator ($10^{-10} \times \mu_{\text{P3HT}}$) and its width reaches 81 nm for a 200 nm diameter nano-pillar, the experimental results are matched (Figure 6.5, right panel).

Figure 6.5 Simulations show that gate coverage could decrease field-effect considerably (left). Numerical calculations resembles the real measurements only when a thick (81 nm) damaged layer is introduced around 200 nm diameter pillar (right).

6.5. Conclusion

In conclusion, unconventional VOFETs are built around a P3HT pillar with (sub) micron diameters. Due to the complexity of the fabrication procedure, gate electrodes could not completely cover the whole circumference of the devices. A surrounding gate was achieved by rotated evaporation, but it was thin and distanced from the pillar. A half-surrounding gate was fabricated by angled evaporation, which led to incomplete gating of the transistors. Neither device configurations showed any considerable gate response. Numerical simulations suggest an 81 nm thick damaged layer, however, it is still a possibility that the difference in the energy levels of P3HT (4.6 eV) and of Pd (5.2 eV) leads to high built-in voltage. In other words, the current density becomes too high since a large number of carriers flows in the VOFET system even in the absence of a gate field. Therefore, a different material choice could help to overcome this issue.

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Chapter 7 Short-Channel Vertical Organic Field-Effect Transistors with High On/Off Ratios

A unique vertical organic field-effect transistor structure in which highly doped silicon nanopillars are utilized as a gate electrode is demonstrated. An additional dielectric layer, partly covering the source, suppresses bulk conduction and lowers the OFF current. Using a semiconducting polymer as active channel material, short-channel (100 nm) transistors with ON/OFF current ratios up to 10^6 are realized. The electronic behavior is explained using space-charge and contact-limited current models and numerical simulations. The current density and switching speed of the devices are in the order of 0.1 A cm^{-2} and 0.1 MHz, respectively, at biases of only a few volts. These characteristics make the devices very promising for applications where large current densities, high switching speeds and high ON/OFF ratios are required.**

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7.1. Introduction

Organic semiconductors (OSCs) are attractive materials due to their flexibility, solution processability, low cost, light weight, and they are utilized in a number of widely investigated electronic devices spanning organic light-emitting diodes (OLEDs), organic field-effect transistors (OFETs), organic photo-detectors (OPDs) and organic photo-voltaic (OPV) cells [1-5]. Currently, great attention is directed towards combining these components in a single (all-)organic integrated device (OID) [6]. However, when integrated with another organic component, despite efficient operation, OFETs present architectural challenges [7]. Therefore, for integration purposes, not only the performance but also the architecture of an OFET must be critically analyzed and designed.

The performance of a transistor can be quantified by two attributes, current density and switching speed [8]. Since organic semiconductors are a low-mobility class of materials, an OFET requires a large transistor width and a short transistor channel length in order to excel in the mentioned attributes [7-10]. From the architectural perspective, in an integrated pixelated device, transistors should also have small footprints so that light-emitting/-sensing devices can occupy larger areas on each pixel. Yet for planar OFETs, the device area increases with the width, and decreasing the channel length demands high-resolution patterning. A vertical geometry allows reduced area requirements by employing a sub-micron thick organic film as the transistor channel [11,12]. However, when the channel length of an OFET approaches the 100 nm regime, high electric fields result in large bulk current densities that cannot be modulated efficiently via a gate-field [13-15]. This phenomenon is known as the short-channel effect, and it restricts further improvement of vertical OFETs (VOFETs).

In this report, a novel VOFET geometry is demonstrated addressing the short-channel effect, in particular by suppressing the undesired bulk current. It is based on a gate electrode consisting of massively parallel highly doped silicon nanopillars (Figure 7.1). Crucially different from other VOFETs, an insulating layer is deposited on top of the bottom contact in order to force injection of the charge carriers only from the sides of the bottom metal, and current flow within a thin layer close to the gate dielectric, minimizing space-charge limited current through the bulk semiconductor. Thanks to this unique geometry, ON/OFF ratios up to 10^6 can be realized, *i.e.*, at least three orders of magnitude larger than in previously reported short-channel (100 nm) VOFETs [11,13].

7.2. Fabrication Procedure

In order to fabricate the nanopillars with a high areal density ($\sim 10^6$ pillars mm^{-2}), optical resist dots (100 nm radius) arranged in a hexagonal lattice (250 nm lattice constant) are created using displacement Talbot lithography (DTL). It allows for fast wafer-scale patterning [16].

Figure 7.1 Fabrication of vertical organic field-effect transistors (VOFETs) with massively parallel nano-pillars as gate. a) Overview scanning electron microscope (SEM) image of the nanopillars. b) Schematic of a single pillar gate. c) SEM image of a single nanopillar. The p-Si pillar core is not visible due to the off-center cross section. d) Zoom-in to the vertical junction next to a nanopillar gate. The red arrow schematically indicates the most likely conduction path.

This resist dot pattern acts as an etch mask during etching of about 300 nm into the underlying silicon. Since the silicon is highly doped p-type (resistivity of 0.010-0.025 $\Omega \text{ cm}$), it can be directly used as a massively parallel nano-pillar gate electrode for a single device ($\sim 7 \times 10^5$ pillars per device of total size $0.7 \mu\text{m}^2$). In our experiments we use bulk silicon wafers, but silicon-on-insulator wafers can be used in order to electrically separate individual many-pillar devices. A stoichiometric low-pressure chemical-vapor-deposited (LPCVD) 45 nm silicon nitride (Si_3N_4) isolates these pillars from the rest of the

device (Figure 7.1). LPCVD Si_3N_4 has a high relative dielectric constant (~ 8), withstanding high electric fields without deterioration. After deposition of Si_3N_4 the bottom electrode is evaporated, during which material on top of the pillars accumulates, increasing the pillar radius, and causing a mushroom-like shape (Figure 7.1a,b). This property stimulates formation of a trapezoidal bottom contact in between the pillars (Figure 7.1c). Additionally, if a subsequent layer is evaporated, the enlarged top diameter causes an increased distance to the base of the pillars (see Figure 7.1b-d). Here, we utilize this property to our advantage, and evaporate an isolating layer (25 nm Al_2O_3) onto the 25 nm gold bottom contact. As illustrated in Figure 7.1d, the gold surface is only exposed at the sides of the trapezoidal bottom contact. Eventually, this architecture creates a conduction path (schematically indicated by the red arrow in Figure 7.1c) close to the gate pillar surface, minimizing the undesired bulk current.

For the organic semiconducting layer we use the conjugated polymer [poly-[2,5-bis(2-octyldodecyl)-3,6-di(thiophen-2-yl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione]-alt-thieno[3,2-b]thiophene] (DPPTTT). This polymer is chosen because it has a high HOMO level (5.2 eV – comparable to the work functions of Au and Pd), it is stable in air and is reported to have a reasonably high mobility of $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [17]. Before deposition of this polymer, the substrate is treated with UV/Ozone and functionalized with self-assembled monolayers (SAMs) of trimethoxy(octadecyl)silane (OTS) and perfluorodecanethiol (PFDT) on the Si_3N_4 dielectric and Au surfaces, respectively. DPPTTT is spin coated on the nano-patterned wafer, resulting in an approximately 60 nm thick layer on Al_2O_3 , while being *circa* 100 nm thick around the pillars (Figure 7.1c). Finally, a 40 nm palladium top electrode (Pd) with a 3 nm thin intermediate layer of silicon dioxide (SiO_2) is evaporated onto the organic material. This SiO_2 layer plays a crucial role, since it forms an interlayer that blocks metal atoms and stops diffusion into the soft organic matter [18]. In addition, a sufficiently thin (2-3 nm) insulating layer between the metal and organic semiconductor stimulates Fermi-level depinning and promotes quasi-ohmic injection of charges [19].

7.3. Transport Measurements

The asymmetry between the electrodes and the work functions is reflected in the current density-voltage (J_D - V_{DS}) characteristics. Unless stated otherwise, the Au bottom

electrode (source, S) is grounded, while a voltage is applied to the Pd top electrode (drain, D). Figure 7.2a shows the J_D - V_{DS} curve for a potential sweep between +1 V and -1 V at a gate voltage $V_{GS} = 0$ V. Since DPPTTT is a p-type semiconductor, injection of holes occurs from the electrode with the highest potential. For $V_{DS} < 0$ V, i.e., hole injection from the bottom, the current is much smaller than for $V_{DS} > 0$ V, due to the limited contact area of the bottom electrode. Figure 7.2b shows J_D - V_{DS} curves for $V_{DS} < 0$ V at different gate voltages (from +2 V to -6 V). The current density does not saturate when $|V_{GS}| \gg |V_{DS}|$, implying that the short-channel effect is not fully suppressed. When a gate sweep is performed for fixed $V_{DS} = -1$ V, the current density ON/OFF ratio reaches 10^6 (Figure 7.2c). We note that the ON/OFF ratios of several working devices (~ 20) lie within the 10^4 - 10^6 range. For comparison, devices without Al_2O_3 insulating layer and with a thinner organic layer of 50 nm were measured as well. All devices gave ON/OFF ratios of 10^2 , which clearly demonstrates the advantage of the optimized architecture. Additionally, thanks to the thin interfacial SiO_2 layer, none of the fabricated devices were shorted. The sweep rate in this measurement is 0.2 V s^{-1} , and hysteresis is observed in all measurements particularly for slower sweep rates (not shown here). We attribute this behavior to a threshold voltage shift that caused by electrochemical reactions involving unavoidable traces of water, turning holes into protons [20].

Figure 7.2 Transistor characteristics. a) Current density J_D for a device with an area of 0.6 mm^2 (7×10^6 pillar gates) is measured by sweeping the voltage applied at the top electrode while grounding the gate and bottom electrodes. b) J_D as a function of top electrode voltage V_{DS} for different gate voltages V_{GS} . c) J_D as a function of V_{GS} for $V_{DS} = -1$ V, for a forward (2 V to -6 V) and backward (-6 V to 2 V) sweep (0.2 V s^{-1} sweep rate).

7.4. Numerical Calculations for mobility

In order to estimate the hole mobility, a fit to the linear regime of the J_D - V_{DS} curve is performed for the following equation:

$$\mu = \frac{L}{WC V_{DS}} \left(\frac{\partial I_D}{\partial V_{GS}} \right) \quad (1)$$

where μ is the mobility, W is the transistor width, L is the channel length, and C is the capacitance per unit area [21]. The drain current I_D can be found by multiplying the current density J_D by the device area A (0.6 mm^2). The effective transistor channel width W of the total device can be extracted by multiplying the circumference of one pillar P by the number of pillars per device. The number of pillars in a single device can be found from the pillar density D and the total area A , yielding

$$W = P \times D \times A = 250 \frac{\text{nm}}{\text{pillar}} \times 7 \times 10^6 \frac{\text{pillars}}{\text{mm}^2} \times 0.6 \text{ mm}^2 \approx 1 \text{ m}$$

It should be noted that such a large width enables a high current at a small areal footprint, ergo high current density. The current contribution per pillar gate is around 3 nA. Using Equation (1) with $L = 100 \text{ nm}$ derived from the SEM images, and $C = 132 \text{ nF cm}^{-2}$ from the Si_3N_4 capacitance measurements, we calculate an effective mobility of $\mu = 4 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

The extracted mobility is much lower than the $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ value reported in the literature for optimized long channel, planar TFTs [17]. In order to verify the extracted mobility, the J_D - V_{DS} measurements are further analyzed by fitting to the space-charge-limited-current (SCLC) model at $|V_{GS}| \gg |V_{DS}|$, and to the contact-limited-current (CLC) model at $V_{GS} = 0 \text{ V}$. The following two equations are used to fit the data in order to extract the SCLC mobility and the potential barrier at the source electrode, respectively:

$$J_D = \frac{9}{8} \epsilon_0 \epsilon \mu \frac{V_{DS}^2}{L^3} \quad (2)$$

where ϵ_0 and ϵ are the vacuum and relative permittivities, respectively [22].

$$J_D = \frac{q\mu N_0}{L} V_{DS} \exp \left[-\frac{q}{kT} \left(\phi_b - \sqrt{\frac{q V_{DS}}{4\pi\epsilon_0\epsilon L}} \right) \right] (1 - FF) \quad (3)$$

where q is the elementary charge, N_0 is the effective density of localized states in the polymer in between which charge hopping takes place, k is the Boltzmann constant, T is temperature, ϕ_b is the potential barrier and FF is the filling factor, which defines the percentage of the area not contributing to the conduction.

In order to fit to SCLC, an individual J_D - V_{DS} curve at $V_{GS} = -6$ V is used (Figure 7.3a). A mobility value of $\mu_{SCLC} = 3.3 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is extracted from this fitting, where $\epsilon = 3$ is used [23]. This value is consistent with the mobility calculated above. For the CLC fit, the filling factor must be determined. The edge of the bottom electrode next to the pillar, which is the only part contributing to the conduction, has a lateral width of 7 nm (Figure 7.1c). Considering that this edge is 100 nm away from the center of the pillar and that the unit area around one pillar is $(270 \text{ nm})^2$, $1-FF$ is estimated to be only 6%. Inserting this value, the estimated effective localized state density $N_0 = 10^{19} \text{ cm}^{-3}$ and $kT = 26 \text{ meV}$ into Equation (3) results in a fitting that gives a barrier height of $\phi_b = 0.19 \text{ eV}$ (Figure 7.3b) [24]. This potential barrier is attributed to the difference between the work function of the SAM-modified gold and the DPPTTT HOMO level. In order to test whether the conduction is affected by the change of the contact resistance, a vertical device without pillars is produced. The current density stayed constant (not shown here) irrespective of the gate voltage applied to the substrate, confirming that the field-effect mechanism (channel resistance) is responsible for the gate response. Additionally, the approximate channel length is extracted from this fit to be $L \approx 95 \text{ nm}$.

Measurements and fittings consistently show that the mobility of the devices is far lower than expected. The interface between the dielectric layers and the semiconductor or the morphology of the polymer could cause this large deviation. Firstly, the untreated dielectric materials (Si_3N_4 and Al_2O_3) have high surface energy and contain trapped charges [25]. The OTS SAM, used in this study, might be insufficient to diminish this reactive nature of the insulators. Secondly, fibers within the spun polymer tend to form π - π stacking along the in-plane direction, while the conduction occurs in the vertical (out-of-plane) direction [17]. In other words, anisotropy in the mobility could occur as a result of horizontally lying polymer fibers. Lastly, the top interfacial layer of SiO_2 could be degrading the organic semiconductor. Even though the high evaporation

rate (0.5 nm sec^{-1}) is used to minimize intercalation into the polymer, there could be a diffuse interface that decreases the overall mobility [26]. Additionally, e-beam evaporation of SiO_2 results in oxygen vacancies in the eventual composition, forming a defective SiO_x ($x=1.9$) layer, which could introduce charge traps for the organic polymer [27]. A different combination of SAM, polymer and insulators could possibly improve the device performance. We stress, however, that, although the mobility is lower than expected, this does not impair the main result of this paper, which is the high ON/OFF ratio facilitated by the suppression of the bulk current.

Figure 7.3 a) Space-charge limited current fit (purple line) to J_D - V_{DS} sweep at $V_{GS} = -6 \text{ V}$ (green diamonds). b) Contact limited current fit (black line) to J_D - V_{DS} sweep at $V_{GS} = 0 \text{ V}$ (orange circles), yielding a barrier height of $\phi_b = 0.15 \text{ eV}$.

7.5. Transport Mechanism

Although the bottom electrode is partly covered with an insulating layer, the top electrode still has a large contact area with the organic material. This means that the charges can be injected from anywhere along the top electrode, unlike for the bottom electrode, where only the edges are available for injection. Additionally, the top electrode is further away from the pillars due to the shadowing effect of the mushroom-topped pillars, which causes the trapezoidal contact formation. Considering these two features, gate manipulation of the charges that are injected from the top electrode is expected to be difficult. This effect can be observed when the polarity of the device is reversed (Figure 7.4 and Figure 7.5).

For a device different from the one shown in Figures Figure 7.2 and Figure 7.3, Figure 7.4 shows the J_D - V_{DS} curves for opposite polarities. While the accumulation at $V_{GS} < 0$ affects both cases similarly, injection from the bottom electrode allows better control during depletion at $V_{GS} > 0$. This is a consequence of the different contact areas and the different distances of the contacts to the pillar. Simulations for a simple geometry with the device simulation software ATLAS are performed in order to confirm this finding [15]. Figure 7.5 show how the hole concentration is affected by the gate for different polarities. When charges are injected into the polymer from the bottom contact through a small window adjacent to the gate electrode, the overall concentration can be decreased drastically when a positive gate voltage is applied (Figure 7.5b). However, for the opposite case, charges are distributed more evenly in the polymer since there is a much larger injection area. Figure 7.5d clearly shows that the concentration within the polymer stays high even when a positive gate voltage is applied.

Figure 7.4 J_D - V_{GS} curves for opposite polarities. Bottom injection: bottom electrode is grounded (purple circle). Top injection: top electrode is grounded (green diamonds).

Figure 7.5 a, b) Simulated hole concentrations for bottom injection, $V_{GS} \ll 0$ and $V_{GS} \gg 0$, respectively. c, d) Simulated hole concentrations for top injection, $V_{GS} \ll 0$ and $V_{GS} \gg 0$, respectively.

7.6. Switching Speed Measurements

For the fabricated 100 nm short-channel VOFET devices, switching speed measurements were also performed. The setup for these measurements is shown in Figure 7.6a. Square voltage pulses between 0 V and -6 V with a switching time of 5 ns were applied to the gate electrode for 1 ms with a repetition of 2 ms and a top electrode voltage of -1 V (Figure 7.6b). The amount of current that is drawn from the source is converted into a voltage through a 270 Ω resistor and measured with an oscilloscope. Switch-on and switch-off responses are plotted in Figure 7.6c,d. Measured rise and fall times (time it takes for the signal to saturate/flatten) are approximately 5 μ s and 10 μ s, respectively, which translates into 0.2 and 0.1 MHz switching speeds. The contrast between the switching times stems from the difference in accumulation mechanisms. For the rise time, the gate field directly attracts charges to the dielectric surface, while for the fall time charges relax into the bulk material in the absence of any field. Even though the mobility is low ($\sim 10^{-4}$ cm²V⁻¹s⁻¹), the switching speeds are approaching the MHz range. Considering that switching speed directly scales with mobility, higher switching speeds are expected when higher mobilities are realized. Additionally, the parasitic capacitance between bottom electrode and the silicon substrate might also be affecting the transit frequency. Reduction of this capacitance would require a thicker insulating layer between the source and the gate contacts.

Figure 7.6 Switching characteristics. a) Circuit diagram of the setup that is used to obtain the switching times. b) Input signal. c) Transistor switch-on plot. The rise time is around 5 μs . d) Transistor switch-off plot. The fall time is around 10 μs .

7.7. Conclusion

In conclusion, we have shown that nano-pillar gates and evaporation of an insulating layer on top of the bottom electrode makes fabrication of VOFETs with 100 nm channel length feasible. The insulating layer allows high ON/OFF ratios up to 10^6 even for such short channel lengths since it decreases the overall bulk current. Despite the low effective field-effect mobility in the present device, switching speeds approaching the MHz range are measured, made possible by the short transistor channel length. In addition, ON currents can reach up to mA range for device areas less than 1 mm^2 , which equals to a current density of 0.1 A cm^{-2} . These results suggest a promising pathway for future integrated light-emitting/-sensing VOFET devices where short-channel effects are minimized, while maintaining functional device characteristics.

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Chapter 8 Conclusions and Outlook

A variety of fabrication steps has been followed throughout the chapters of this thesis, which aims to reduce the dimensions of organic and inorganic materials. Each fabrication procedure resulted in a different device architecture with nanostructures. In this chapter, conclusions drawn from the experimental results are further discussed. Additionally, a wider perspective, regarding both fabrication and experimental approaches, is provided for future research.

8.1. Outlook

In Chapter 4, a fabrication methodology was developed in order to create a high-density array of silicon nano-crystals for the purpose of photoluminescence studies. The main advantage, in contrast to literature, is the ordered structuring and alignment that was obtained via displacement Talbot lithography (DTL). Thanks to this technique, each nano-crystal can be addressed individually unlike reports where nano-crystals are randomly embedded within an amorphous network [1-3]. However, there are still several aspects that could be improved. First of all, the process includes multiple wet-etching steps that must be timed accurately. Any further etching could destroy the whole array of nanostructures. In this work, the potassium hydroxide (KOH) is used due to its self-limiting nature which gives a precise control of the final dimensions [4]. However, the quality and temperature of KOH makes a difference in etch rates. Additionally, any thin oxide layer could impair the etching performance since KOH has a high selectivity (see Chapter 4). When dimensions approach below 15 nm, accurate timing is needed in order to achieve silicon nano-crystal with required dimensions. Valenta *et al.* showed that even small deviations in the dimensions could suppress photoluminescence, which is the fundamental phenomenon appearing in silicon nano-crystals [5]. In that report, silicon nano-pillars were oxidized in two steps in order to reach the final structures. This

Figure 8.1 An alternative fabrication procedure for nano-channels which stays embedded within a flat wafer.

oxidation approach is more suitable than wet-etching in terms of reproducibility, since it is well-established and the thickness of oxide can be pre-determined for each crystal plane [6]. Therefore, the final shrinkage of nano crystals can be performed by oxidation.

Chapter 5 considers fabrication of nano-channels via local oxidation of silicon and wet-etching methods in order to study 1D conduction and fluorescence mechanisms of different materials, especially organic/inorganic semiconductors. The final opening of the channels can reach below 10 nm and it helps to prevent clogging of the channels. A fluorescent molecule was used as a proof-of-concept material to show filling of the channels. However, the channels can be filled with any material that is evaporated or sputtered.

On the other hand, the non-flat nature of these patterns is cumbersome for removal of the materials and for fabrication of electrical contacts. Another approach can be utilized to form superior nano-channel structures. The recipe can be changed as follows. First, the BARC lines can be shrunk, as in Chapter 4, forming 30-35 nm wide lines. After transferring this pattern into Si_3N_4 , the whole wafer can be oxidized instead of direct wet-etching (Figure 8.1). This would form a wide lines of SiO_2 , and removing Si_3N_4 opens thin lines of silicon plateau. Performing dry-etching creates trenches, and wet-etching of this substrate makes diamond shaped nano-channels that are embedded within the flat silicon substrate. This improves the overall etching of the deposited materials that are subject for experimentation. It is also preferable to use electrodes that can be spin coated as thick layers so that uniform and complete coverage of the nano-channels can be achieved [7].

In Chapter 6, a vertical organic field-effect transistor (VOFET) with the use of wedging transfer technique is produced. This method is the first to confine organic materials into such small dimensions. The transport measurements did not result in a distinct gate modulation as expected from device simulations. This is attributed to a thick layer of defective material at the dielectric/polymer interface. Reactive ion etching can indeed deteriorate the polymer but it should not cause complete malfunction [8]. The

short-channel effect, on the other hand, is a common problem with organic semiconductors. An alternative approach would be to use different OSC with higher HOMO levels or metal electrodes with lower work-functions. Hirose *et al.* reported that forming Schottky contacts could prevent the short-channel effect and present normal transistor operation even for transistor lengths of 30 nm [9]. They use directly evaporated gold as the electrodes and poly(9,9-dioctylfluorene-co-bithiophene) (F8T2) as the organic semiconductor. These combinations seem to be good candidates to try. However, beyond materials selection, the fabrication of the gate electrode also needs improvement. After the contact pads are formed, sputtering could be used to achieve full coverage of the pillars. This requires an additional HSQ step, which ensures that the gate only extends along the OSC and not the top contacts. Additionally, before fabrication of any other device the relation among diameter, height, gate dielectric thickness, metal work-functions and OSC orbital levels must be thoroughly investigated.

Another novel VOFET architecture is discussed in Chapter 7. This structure demonstrates a possible pathway to decrease the unwanted bulk currents, ergo the short-channel effects. Beyond that it also brings other possibilities such as vertical organic/inorganic light-emitting/sensing transistors. First of all, an alternative approach could be sputtering of an inorganic material, such as indium gallium zinc oxide (IGZO) [10]. Secondly, the whole process can be performed on an indium tin oxide (ITO) substrate, creating a transparent gate medium [11]. Additionally, the top layer could also be a sputtered ITO layer creating a transparent top layer. As stated in Chapter 7, a thin layer of SiO₂ must be deposited first before sputtering or evaporation of another material. It is also possible to create nano-pillars in such an orientation that they form a 2D photonic crystal with the active layer [12]. This would drastically improve the external efficiency of light-emission via preventing light to travel in transverse directions. Apart from photonic applications, the VOFET device could be integrated back-to-back with a light-emitting device, and provide it a necessary driving current through a shared electrode.

8.2. Conclusion

Developed intricate fabrication details, prepared nano-structured silicon substrates, investigated hybrid transistors and novel experimental results presented within this thesis bring the conclusion that combination of organic and inorganic materials could yield prevailing nano-electronic devices. However, as described in the outlook, the fabrication procedures still hold a large room for improvement. The silicon substrate can be manufactured in many different ways and introduce various hybrid device perspectives that remain unexplored at this point. In addition, since the active materials are constructed at nanoscale where they exhibit quantum phenomena, the possibilities to confine different materials within the similar systems in order to investigate their unique characteristics are open. Furthermore, the unique VOFET architectures could find applications in integrated devices after optimal material selection.

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SUMMARY

Organic semiconductors have attracted a lot of attention with their unique electrical (tunable bandgap), optical (photoluminescence) and physical (flexibility) abilities. A number of applications, such as organic light-emitting diodes, flexible electronic devices, biodegradable sensors etc. are realized thanks to these properties. However, fundamental understanding of organic semiconductor materials and devices is still necessary in order to obtain near-ideal performance from current and future applications. In light of this quest, this thesis presents a variety of fabrication procedures that provides better device performances or pathways to investigate unique features of organic semiconductors. The proposed methodologies rely on silicon substrates and also utilize a number of inorganic dielectric materials and metal electrodes. Combining organic and inorganic materials creates an easy-to-fabricate hybrid devices. In addition, using nanofabrication processing technologies, devices with nanostructured substrate and confined organic materials are realized. When one or more dimensions of the organic and inorganic materials measure below 100 nm and 20 nm respectively, they provide unique phenomena. For example, when silicon is confined in three-dimensions, it shows increased photoluminescence, and organic semiconductors present increased diffusion of charge carriers when confined between two electrodes.

From the application perspective, the main organic device architecture investigated in this thesis is vertical organic field-effect transistors (VOFETs). The band structure of (organic) semiconductors and transport characteristics of organic FETs are discussed in Chapter 2. In addition, how these aspects are influenced by the molecular arrangement within the bulk organic material is also covered. While ideal packing of the molecules allows delocalization of charge carriers, it is discussed that most materials possess localized states, *ergo* low mobility. Furthermore, the transport mechanism is explained to depend on more reasons such as contact resistance at the organic/metal interface, charge trapping along the dielectric surface and transistor channel length. At the last section, fabrication methods for creating organic nanowires are discussed and superiority of template-assisted methods is elaborated.

Chapter 3 explains nano-fabrication techniques used throughout the thesis. It starts with explaining a novel displacement Talbot lithography (DTL) method that enables patterning of lines and dots with lateral dimension of 80-120 nm. Various lithography, etching and deposition methods are also discussed within that chapter. Furthermore, standard recipes to be used during fabrication are given.

Summary

In Chapter 4, high-density arrays of crystalline silicon nanostructures are fabricated using lithography techniques of DTL and edge lithography (EL). First, two resist patterning steps are performed on silicon wafers coated with silicon nitride (Si_3N_4) hard-mask. In each step, the pattern is transferred to the Si_3N_4 , and wet-etching with potassium hydroxide (KOH) is used to structure the whole wafer. After the wafer is patterned in two orthogonal directions, remaining Si_3N_4 is utilized for EL, where retraction at the edge of the nanostructures allows growth of local oxidation of silicon (LOCOS). Lastly, the Si_3N_4 is removed and silicon is etched to remain only within the LOCOS corners due to high anisotropic etching profile of KOH. Final silicon nanostructures with dimensions below 15 nm are realized with a potential density of 10^{10} cm^{-2} . Individual addressing of these silicon nanocrystals may find applications in optical sensing systems.

A nano-channel template to produce organic nanowires is created in Chapter 5. Similar to Chapter 4, the fabrication includes DTL, wet etching with KOH and growth of LOCOS. The final nano-channels lie along the whole substrate with openings below 10 nm. The template has the potential to have even smaller gaps with the help of atomic layer deposition (ALD) technique. As a proof-of-principle, an organic dye is patterned in these nano-channels and fluorescence is observed from the nanowires. Different organic materials could be patterned/confined using this template to investigate their optical and electrical properties.

In Chapter 6, a pillar VOFET is fabricated and measured. An organic semiconductor poly(3-hexylthiophene) (P3HT) is spin-coated on a substrate with bottom electrodes and top contacted using wedging transfer technique. Initially, the top part has only dots that enables patterning of P3HT into pillars. The organic pillars are covered via ALD and electrodes are deposited via evaporation. Gate electrodes did not cover the circumference of the pillars completely, and highly reduced field-effect observed from these devices. This behavior is attributed to the damaged layer around the organic polymer, that could arise during the reactive ion etching process. However, different combination of organic semiconductor and metal electrodes with improved gate coverage is expected to provide increased performance.

Another novel VOFET is designed, fabricated and characterized in Chapter 7. In this case, the vertical stacking is performed on a silicon substrate with hexagonally arranged nano-pillars with diameter and spacing of 80 nm and 250 nm, respectively. The pillars act as one gate to manipulate charges along the semiconductor that lies next to

them. Even though, the stacking comprises a thin-layer of an active organic semiconductor (short transistor channel length), the bulk current is decreased by orders of magnitude with the help of an insulating layer on the bottom electrode. This design allows injection of charges only around the gate pillars and therefore it increases field-effect on the device by keeping injection window as close to the gate as possible. Such device may be used to decrease the footprint of transistors and improve their characteristics such as current density and operation frequency.

SAMENVATTING

Organische halfgeleiders hebben veel aandacht getrokken met hun unieke elektrische (instelbare bandafstand), optische (fotoluminescentie) en fysieke (flexibiliteit) capaciteiten. Dankzij deze eigenschappen worden een aantal toepassingen gerealiseerd, zoals organische licht-emitterende dioden, flexibele elektronische apparaten, biologisch afbreekbare sensoren enz. Fundamenteel inzicht in organische halfgeleidermaterialen en -apparaten is echter nog steeds nodig om bijna ideale prestaties te verkrijgen van huidige en toekomstige toepassingen. In het licht van deze zoektocht presenteert dit proefschrift diverse fabricageprocedures die betere apparaatprestaties of -routes bieden om unieke kenmerken van organische halfgeleiders te onderzoeken. De voorgestelde methodologieën zijn gebaseerd op silicium substraten en maken ook gebruik van een aantal anorganische diëlektrische materialen en metaalelektroden. Het combineren van organische en anorganische materialen zorgt voor eenvoudig-te-fabriceren hybride apparaten. Daarnaast worden met behulp van nanofabricage verwerkingstechnologieën apparaten op een substraat met nanostructuur en ingesloten organische materialen gerealiseerd. Wanneer een of meer dimensies van de organische en anorganische materialen respectievelijk minder dan 100 nm en 20 nm meten, bieden ze unieke verschijnselen. Bijvoorbeeld, wanneer silicium is ingesloten in drie dimensies, vertoont het verhoogde fotoluminescentie, en organische halfgeleiders hebben een verhoogde diffusie van ladingsdragers wanneer ze zijn ingesloten tussen twee elektroden.

Vanuit het toepassingsperspectief is de belangrijkste organische apparaat architectuur die in dit proefschrift wordt onderzocht verticale organische veldeffecttransistoren (VOFETs). De bandstructuur van (organische) halfgeleiders en transporteigenschappen van organische FETs worden besproken in Hoofdstuk 2. Daarnaast wordt ook besproken hoe deze aspecten worden beïnvloed door de moleculaire regeling binnen het organische bulkmateriaal. Hoewel ideale verpakking van de moleculen delocalisatie van ladingsdragers mogelijk maakt, wordt besproken dat de meeste materialen gelokaliseerde toestanden bezitten, *ergo* lage mobiliteit. Verder wordt het uitgelegd dat het transportmechanisme afhankelijk is van meer redenen zoals contactweerstand op het organisch/metaal grensvlak, ladingsvangst langs het diëlektrische oppervlak en transistorkanaallengte. In het laatste deel worden fabricagemethoden voor het maken van organische nanodraden besproken en wordt de superioriteit van sjabloon-gestuurde methoden uitgewerkt.

Hoofdstuk 3 legt de nanofabricagetechnieken uit die in dit proefschrift worden gebruikt. Het begint met het uitleggen van een nieuwe verplaatsingsmethode van de waterverplaatsing Talbot lithografie (DTL) die patronen van lijnen en punten met een laterale afmeting van 80-120 nm mogelijk maakt. Verschillende lithografie-, ets- en depositiemethoden worden ook besproken in dat hoofdstuk. Verder worden standaardrecepten gegeven die tijdens de fabricage moeten worden gebruikt.

In Hoofdstuk 4 worden arrays met hoge dichtheid van nanostructuren van kristallijn silicium gefabriceerd met behulp van lithografietechnieken van DTL en randlithografie (EL). Eerst worden twee resist-patroonstappen uitgevoerd op siliciumwafers bekleed met siliciumnitride (Si_3N_4) hard-masker. In elke stap wordt het patroon overgebracht naar de Si_3N_4 en nat etsen met kaliumhydroxide (KOH) wordt gebruikt om de hele wafer te structureren. Nadat de wafer in twee orthogonale richtingen is gepatroneerd, wordt overgebleven Si_3N_4 gebruikt voor EL, waar retractie aan de rand van de nanostructuren groei van lokale oxidatie van silicium (LOCOS) mogelijk maakt. Ten slotte wordt het Si_3N_4 verwijderd en wordt silicium geëtsd om alleen binnen de LOCOS hoeken te blijven vanwege het hoge anisotrope etsprofiel van KOH. Uiteindelijke silicium nanostructuren met dimensies onder 15 nm worden gerealiseerd met een potentiaaldichtheid van 10^{10} cm^{-2} . Individuele adressering van deze silicium nanokristallen kan toepassingen vinden in optische detectiesystemen.

Een nanokanaalsjabloon voor het produceren van organische nanodraden wordt in Hoofdstuk 5 gemaakt. Net als in Hoofdstuk 4 omvat de fabricage DTL, nat etsen met KOH en groei van LOCOS. De laatste nanokanalen liggen langs het gehele substraat met openingen onder 10 nm. De sjabloon heeft het potentieel om nog kleinere openingen te hebben met behulp van atomaire laagdepositie (ALD) techniek. Als een proof-of-principle wordt een organische kleurstof in deze nanokanalen gevormd en wordt fluorescentie waargenomen van de nanodraden. Verschillende organische materialen kunnen gevormd worden met behulp van deze sjabloon om hun optische en elektrische eigenschappen te onderzoeken.

In Hoofdstuk 6 wordt een pilaar VOFET gefabriceerd en gemeten. Een organische halfgeleider poly (3-hexylthiofeen) (P3HT) wordt spin-gecoat op een substraat met bodemelektroden en boven in contact gebracht met behulp van de "wedging-transfer" techniek. In eerste instantie heeft het bovenste gedeelte alleen dots waarmee P3HT in pilaren kan worden gepatroneerd. De organische pilaren worden afgedekt via ALD en de elektroden worden via verdamping afgezet. Poortelektroden

bedekten de omtrek van de pilaren niet volledig en sterk verminderd veldeffect waargenomen van deze apparaten. Dit gedrag wordt toegeschreven aan de beschadigde laag rondom het organische polymeer, die zou kunnen ontstaan tijdens het reactieve ionen-etsproces. Het is echter te verwachten dat een andere combinatie van organische halfgeleider- en metaalelektroden met verbeterde poortbedekking betere prestaties zal leveren.

Een andere nieuwe VOFET is ontworpen, gefabriceerd en gekenmerkt in hoofdstuk 7. In dit geval wordt de verticale stapel uitgevoerd op een siliciumsubstraat met hexagonaal geplaatste nano-pilaren met een diameter en een tussenafstand van respectievelijk 80 nm en 250 nm. De pilaren fungeren als één poort om ladingen langs de halfgeleider die naast hen ligt te manipuleren. Hoewel de stapeling bestaat uit een dunne laag van een actieve organische halfgeleider (korte transistorkanaallengte), neemt de bulkstroom af met ordes van grootte met behulp van een isolatielaag op de onderste elektrode. Dit ontwerp maakt het mogelijk om alleen ladingen rond de poortpilaren te injecteren en verhoogt daardoor het veldeffect op het apparaat door het injectievenster zo dicht mogelijk bij de poort te houden. Een dergelijke inrichting kan worden gebruikt om de voetafdruk van transistoren te verkleinen en hun karakteristieken zoals stroomdichtheid en werkfrequentie te verbeteren.

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