A 0.2 - 8 MS/s 10b flexible SAR ADC achieving 0.35 - 2.5 fJ/conv-step and using self-quenched dynamic bias comparator

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Abstract

A 10b flexible SAR ADC is presented incorporating a self-quenched dynamic bias comparator and a self-triggered asynchronous delay line. The ADC is fabricated in 65nm CMOS, occupies 0.04mm^2 and has an ENOB > 9bit and SFDR > 66dB for sampling rates from 0.2 to 8MS/s at supply voltages respectively from 0.7V to 1.3V with a Walden FoM from 0.35 to 2.5fJ/conv-step. Keywords: SAR ADC, flexible, Walden Figure-of-Merit, SNDR, dynamic bias.

Introduction

SAR ADCs have high energy efficiency and are used in many IoT applications and low power radios. For these applications, sample rates vary from 0.1 to 10 MS/s [1-4]. ADCs achieving lowest Walden Figure-of-Merit, FoM_W [1,2] reach that high energy efficiency only at a (few) fixed operating point(s). ADCs [3,4] demonstrating flexibility over supply voltage, V_{DD} or sample rates do not achieve low FoM_W. This work introduces a low FoM_W SAR ADC that demonstrates flexibility in operation over V_{DD} and sample rates.

Main challenges for an energy efficient flexible SAR are: 1) kT/C and comparator noise at small V_{DD} (or full-scale input range, FSIR) 2) distortion due to the (non-linear) sample charge associated with comparator's input and e.g. (sample) switches at large V_{DD} (or FSIR) and 3) switching energy (CV^2) associated with the DAC. Majority voting [6] can be used to address the challenge in 1) but, at low sample rates and requires delay tuning and energy overhead in the delay line controller. Excluding comparator and switch effects, the absolute minimum sampling capacitance, C_S for kT/C limited operation at a $1V_{P\text{-}P}$ input for 10-bit resolution is 100fF, whereas unit cell mismatch and the non-linear (comparator) input capacitance typically requires C_S to be about 250fF for < 1LSB INL/DNL for 10 bit operation [6].

This work achieves an energy-efficient flexible SAR ADC by 1) using a low noise dynamic bias comparator [5] for which the input referred noise scales with V_{DD} to attain a near constant ENOB 2) isolating the comparator from the DAC during sampling thereby preventing distortion due to the non-linear sample charge 3) using a C_S close to the mismatch limit (175fF) and (4) using a low power self-triggered delay line.

Architecture

The SAR ADC uses a self-quenched dynamic bias comparator [5], see Fig.1(a). In [5], the drain nodes of the pre-amplifier continue to discharge even after the comparison is done. However, in this work, a low leakage self-triggered delay line is used (see Fig.1(b)) that resets the comparator as soon as its output is latched thereby preventing any further energy dissipation. The drain nodes of the pre-amplifier do not discharge to ground at the end of comparison, see Fig.1(c) which reduces the reset energy by a factor 2 in our design. At V_{DD} = 0.7V, the input referred noise for the comparator is about 0.7mV (≈ quantization noise) for an integrating capacitance (Fig. 1(a)), C_P = 7fF and the energy consumption of the comparator per SAR cycle is about 55fJ. At V_{DD} = 1.3V, the input referred noise is about 1.1mV and the energy consumption is 400fJ per SAR cycle.

In comparison to the fixed delay line architecture in [1,2,7], our self-triggered delay line allows for scalability in speed wrt V_{DD} and optimizes the energy consumption for each operating point. During sampling, the delay line is reset and the comparator CLK = 0. During conversion, the rising START(N) pulse initiates the Nth-bit comparator operation by making CLK = V_{DD}. As soon as either of the comparator's output reaches V_{DD} and the bit is latched into the output register, the CLK is discharged to ground and the comparator is reset. The duration of the timing signals for this self-triggered asynchronous delay line depends on the comparison time. The energy consumption of the self-triggered delay line controller at 0.7V and 1.3V supply is respectively 60fJ and 450fJ per SAR cycle.

Fig.2 shows the complete SAR ADC. The differential inputs are compared before sampling. Depending on the result, input signal in the range 0 – V_{PK}/2 is sampled on C_{DAC-} and the complimentary input range (V_{PK}/2 – V_{PK}) is sampled on C_{DAC+}. This swapping (logic) of the input signals is similar to [8]. The maximum change in the sample voltage across consecutive sampling instants is reduced by a factor 2 throughout the Nyquist band of input frequencies for our architecture compared to the conventional SAR ADC. This results in a reduced input drive energy for our ADC for a given FSIR and SNR [8]. Additional swapping is performed inside the SAR loop by SWP2 to cancel the comparator offset and to avoid any distortion thereof. Swapper SWP2 is turned OFF during sampling isolating thereby the nonlinear (signal dependent) comparator's input capacitance from the DAC array. The

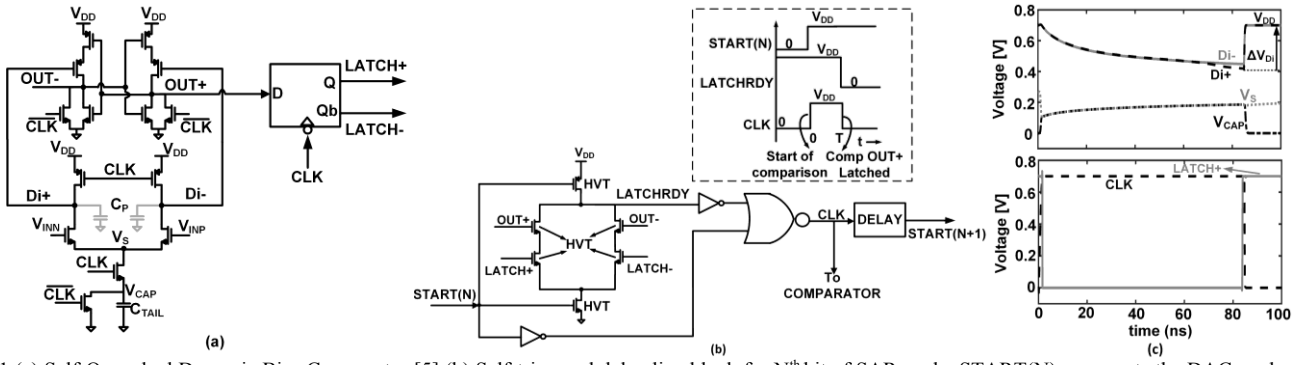

Fig.1 (a) Self-Quenched Dynamic Bias Comparator [5] (b) Self-triggered delay line block for Nth bit of SAR cycle. START(N) represents the DAC ready pulse for the Nth bit. HVT transistors reduce the leakage current for the logic block. The latch is integrated within the delay line controller for self-trigger operation without any area or interconnect overhead. (c) Timing waveforms for 0.7V, 200kS/s SAR operation for near LSB input.

sampled input charge therefore does not include signal dependent (non-linear) components. This allows our architecture to operate over wide range of supply voltage (and FSIR) at a constant resolution and linearity. Improved linearity associated with the input sampling allows the ADC to use a C_S close to mismatch limits. The ADC uses a split monotonic DAC array with single-ended capacitance, C_S = 175fF. The energy consumption of conventionally switching the DAC array is $E_{DAC} = 2 \cdot C_S \cdot V_{DD}^2$. A 3-step charge-discharge sequence [7] is used for the 2 MSBs which yields a factor 2 reduction to result in E_{DAC} = 85fJ for 0.7V and about 360fJ for 1.3V operation.

Measurement Results

Fig.3 shows the die micrograph of the SAR ADC (area: 0.04mm^2) in 65nm CMOS. The peak INL/DNL performance at 0.7V(200kS/s) and at 1.3V(8MS/s) operation is respectively 1LSB/0.8LSB and 1.1LSB/0.5LSB as shown in Fig.4. Fig.5 shows the max. sample rates and FoM_W for the corresponding supply voltage. The FoM_W increases below 0.7V due to ENOB degradation (<9b). In comparison to the flexible SAR ADCs in [3,4] our SAR ADC has the lowest FoM_W over the entire range of operation. Fig.6 shows the FFT of near Nyquist input for 0.7V(200kS/s) and 1.3V(8MS/s) operation. Fig.7 shows the SFDR/SNDR over the range of input frequencies for 0.7V(200kS/s) and 1.3V(8MS/s) operation. Table 1 compares our SAR ADCs with the lowest FoM_W ADCs (< 1fJ/conv-step) [1,2]. At 0.7V our ADC achieves the lowest FoM_W which is 1.2x lower than in [1]. It is to be noted that the measured performance as shown and mentioned in [1] is after a) doing a foreground off-chip calibration (to remove multi-comparator offset) and b) performing a four- time averaged FFT, which are not performed in our measurements. In conclusion our ADC achieves the lowest reported FoM_W at 0.7V, is flexible over a wide range of supply voltage and sampling frequencies with a low FoM_W, and also relaxes the input drive requirements by using 175fF sampling capacitor and sampling only half of the FSIR on each C_S without compromising the dynamic range.

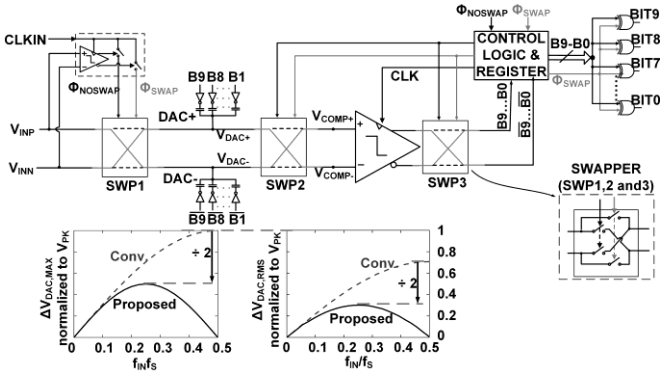

Fig.2 10b SAR ADC architecture with 2x reduction in maximum voltage change at the sampling capacitors. Swapper at the output of the comparator keeps the overall SAR loop convergent. (MATLAB) simulated maximum and RMS change in voltage across the sampling DAC for both the conventional and proposed sampling is shown here.

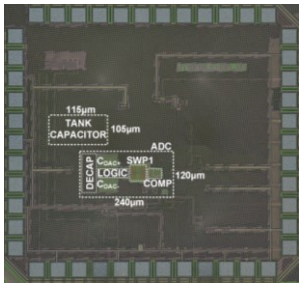

Fig.3 Die micrograph of the ADC in 65nm CMOS.

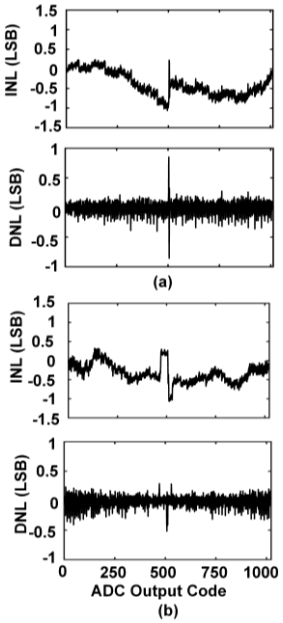

Fig.4 INL and DNL performance at (a) 200kS/s, 0.7V supply and (b) 8MS/s, 1.3V supply.

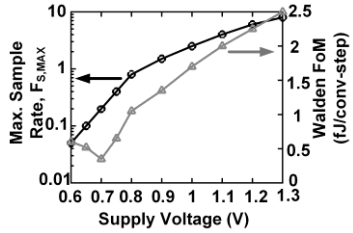

Fig.5 FoM_W and max. sampling rates for 0.65V to 1.3V supply.

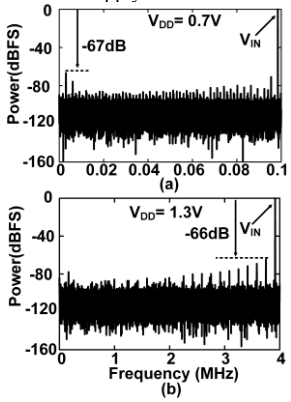

Fig.6 FFT of the near Nyquist input frequency for (a) 0.7V, 200kS/s and (b) 1.3V, 8MS/s operation

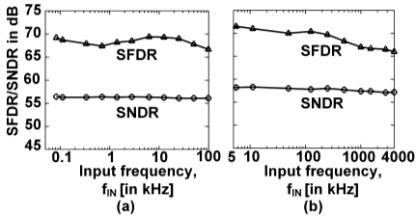

Fig.7 SNDR and SFDR for range of input frequencies for (a) 0.7V, 200kS/s and (b) 1.3V, 8MS/s operation

		This Work	[1]	[2]
Technology		65nm	90nm	40nm
Resolution		10	11	10
Flexible		**Yes**	No	No
Supply Voltage [V]	Min	0.7	0.3	0.45
	Max	1.3		
Sample Rate [MS/s]	Min	0.2	0.6	0.2
	Max	8		
Sample Capacitance, C_S		**175fF**	850fF	850fF
Energy consumption (Power/$f_{S,MAX}$)		0.19pJ @0.7V 1.6pJ @1.3V	0.31pJ	0.42pJ
ENOB [bits]	Min	9.07	9.46	8.95
	Max	9.3		
Walden FoM (fJ/conv-step)	Min	**0.35**	0.44	0.85
	Max	2.5		
Calibration		No	Yes, off-chip	No
Area (in mm^2)		0.04 (incl. decaps)	0.035 (Core only)	0.0065 (Core only)

Table1: Table of Comparison with FoM_W < 1 fJ/conv-step SAR ADCs

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