A 0.06-3.4 MHz 92 μW Analog FIR Channel Selection Filter with Very Sharp Transition Band for IoT Receivers

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***Abstract*—Analog FIR filtering is proposed to improve the performance of a single stage g_m-C channel selection filter for ultra low power Internet-of-Things receivers. The transconductor is implemented as a Digital-to-Analog Converter; allowing a varying transconductance in time, which results in a very sharp FIR filter. The filter is manufactured in 22 nm FDSOI and has a core area of 0.09 mm^2. It consumes 92 μW from a 700 mV supply and achieves $f_{-60\mathrm{dB}}/f_{-3\mathrm{dB}} = 3.8$. The filter has 31.5 dB gain, out-of-band OIP3 of 28 dBm and output referred 1-dB compression point of 3.7 dBm. The filter bandwidth is tunable from 0.06 to 3.4 MHz.**

***Index Terms*—Analog Filters, Low-Pass Filter, FDSOI, Analog FIR Filters, low power, Internet-of-Things, g_mDAC.**

I. Introduction

Integrated Low-Pass Filters (LPFs) are an essential building block in modern RF receivers. In receivers that target Internet-of-Things applications, it is very important to achieve sufficient Signal-to-Noise Ratio (SNR) for minimal power consumption. Furthermore, the frequency spectrum becomes more and more crowded — increasing the demand for channel selection filters with strong rejection and very sharp transition band.

Fig. 1 shows a typical zero-IF receiver, consisting of a Low-Noise Amplifier (LNA), mixer, local oscillator, LPF and Analog-to-Digital Converter (ADC). Traditionally, integrated LPFs are designed using continuous-time g_m-C [1, 2] or opamp R-C structures [3]. These architectures require multiple transconductors to create higher order filtering. However, multiple transconductors means multiple noise sources and a poor power to noise trade-off. Alternatives are the discrete-time analog IIR approaches of [4–6], but they do not achieve sharp filtering.

Very high SNR per mW of power can be obtained by a single g_m-C stage. Unfortunately, a single g_m-C stage provides only first-order filtering, which is insufficient for a channel selection filter. The filter response can significantly be improved by varying the transconductor in time. This provides Analog Finite-Impulse-Response (AFIR) filtering [7], alternatively also called Filter-by-Aliasing [8] when a mixer is included. Previous implementations require very high sample rate [8], cascaded FIR stages [9] or have a power hungry transconductor design [7] and have therefore high power consumption.

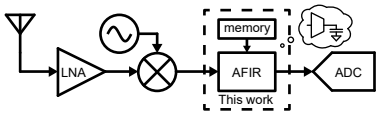

Fig. 1. This work in a RF receiver.

In this work, we propose a low power Analog FIR (AFIR) filter as channel selection filter. It contains a single inverter based g_m-C integrator for maximal SNR per power [10]. The transcoductor is implemented as a Digital-to-Analog Converter: g_mDAC. Its power consumption is significantly reduced by lowering the required sample rate and by implementing it partially thermometer coded. The filter provides very strong filtering while dissipating only 92 μW.

II. Analog FIR Filter

Fig. 2 illustrates the working principle of AFIR filters by comparing it to its digital equivalent. A 6-tap digital FIR filter is shown in Fig. 2a. The input signal $x[n]$ is passed through a delay line with delays z^{-1}. The delayed samples of $x[n]$ are multiplied by an appropriate weight w_a and summed providing the output $y[n]$. The weights w_a represent the impulse response of the FIR filter. $y[n]$ can be downsampled resulting in output signal $y^*[k]$ without introducing significant aliases in-band, when the FIR filter rejection is sufficient. The corresponding timing diagram shows that an output sample of $y^*[k]$ consists of the weighted sum of different time instances of $x[n]$. The straightforward analog implementation is to store the input on multiple capacitors and sum the capacitor voltages while applying the appropriate weighting [9, 11]. However, this becomes very hardware intensive when moving towards a high number of FIR taps.

Fig. 2b shows an alternative approach to implement the same filter. Instead of storing the previous input samples, $x[n]$ is multiplied by *time-varying* weighting coefficient $w[n]$ and accumulated in the integrate+dump block. The output signal $y^*[k]$ is constructed in the same way as in Fig. 2a and therefore the implementation of Fig. 2b has the same filter response.

The proposed AFIR filter is shown in Fig. 2c. It performs a similar operation as its digital analogy (Fig. 2b). The input signal $v_{in}(t)$ is converted to current via transconductance $g_m(t)$. The transconductance $g_m(t)$ varies in time at rate f_w according

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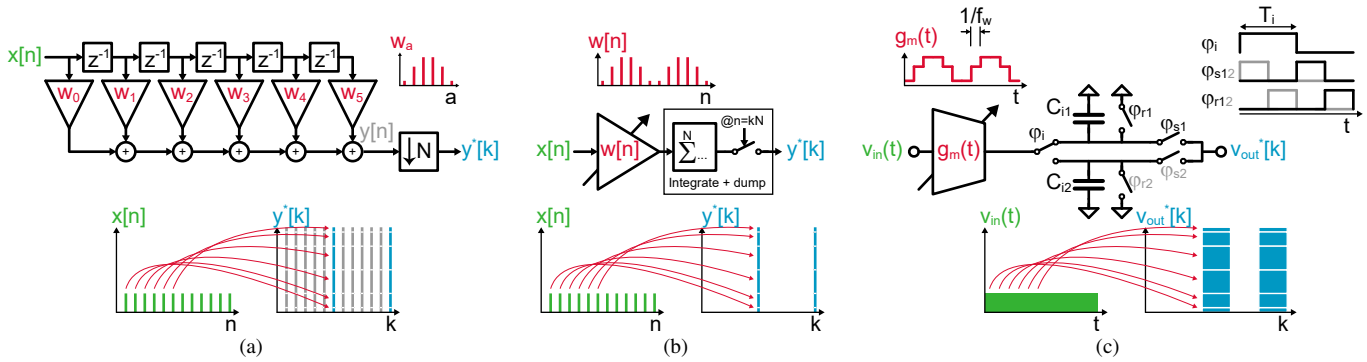

Fig. 2. Comparison of different implementations of 6-tap digital and analog FIR filters. Input signals $x[n]$ and $v_{in}(t)$ are assumed constant for simplicity. (a) Digital FIR with downsampling. (b) Digital FIR with accumulator. (c) Hardware efficient analog FIR.

to the FIR weighting coefficients w_a. The transconductor output current is integrated (summed) on integration capacitor C_{i1} during ϕ_i. The output voltage sample $v^*_{out}[k]$ is sampled during ϕ_s and reset in during ϕ_r. Meanwhile, the input signal is integrated on the other capacitor C_{i2}; providing time for readout and reset. The output samples are thus determined by a weighted summation of previous input 'samples' — similarly as in Fig. 2a and Fig. 2b. However, the windowed integration at f_w introduces an extra sinc pre-filter.

The AFIR transfer function neglecting aliasing is [7]

$$H(f) \approx \underbrace{\frac{\overline{g}_m T_i}{C_i}}_{\text{gain}} \underbrace{\text{sinc}\left(\frac{f}{f_w}\right) e^{j\pi \frac{f}{f_w}}}_{\text{windowed } \int} \underbrace{\sum_{a=0}^{N-1} w_a z^{-a}\Big|_{z=e^{j2\pi \frac{f}{f_w}}}}_{\text{FIR}} \quad (1)$$

where $\overline{g}_m$ is the average transconductance, w_a the weighting coefficients normalized to $\sum w_a = 1$ and N the number of FIR coefficients. The transfer consists of three parts: gain, sinc windowed integration and the FIR filter. Note that the filter characteristic is determined by the weighting coefficients — only the gain is dependent on $\overline{g}_m/C_i$. The AFIR input signal is time-continuous and the output signal time-discrete, so in addition to filtering also aliasing occurs. The output sample rate f_s is significantly lower than the time-continuous input. Fortunately, the very strong filtering characteristic of the AFIR provides sufficient pre-filtering by itself.

The filter bandwidth is inversely proportional — for a given set of FIR coefficients w_a — to the filter delay $1/f_w$ and integration time $T_i = N/f_w$. By doubling T_i, the filter bandwidth is halved. Fig. 2c describes a *single path* AFIR design, which filter characteristic is limited by the fixed relationship between sample rate and bandwidth: $f_s = 1/T_i$. This constraint is broken by interleaving multiple paths. For m paths, this results in an output sample rate

$$f_s = \frac{m}{T_i} \qquad m = 1, 2, 3... \quad (2)$$

III. AFIR Circuit Implementation

The proposed AFIR filter implementation is shown in Fig. 3. It contains two differential time-interleaved paths (A and B) to allow 2 µs integration time for an output sample rate of 1 MHz. The variable transconductor is implemented by a 10 bit pseudo-differential g_mDAC. The AFIR control logic is clocked by a differential 64 MHz clock, resulting in a 128 taps filter.

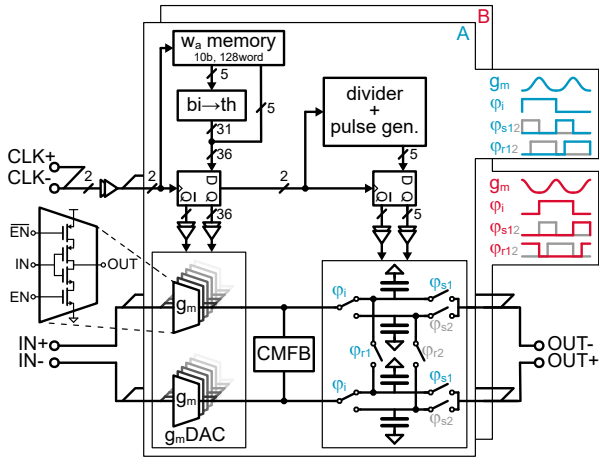

Fig. 3. Analog FIR filter circuit implementation and timing waveforms.

The g_mDAC consists of switchable g_m unit cells [12]. The push-pull architecture provides maximal g_m per current to optimize SNR [10]. The cells are turned on/off via the switches that are controlled by the enable signal EN. In this way, the g_mDAC bias current is proportional to the FIR g_m-code — maximizing SNR per mW of power. The g_mDAC output bias is defined by the common-mode feedback (CMFB) at the voltage of a self-biased g_m-cell.

The FIR g_m-code is provided by a 10 bit, 128 word memory and re-clocked in D-flipflops (DFFs) at 64 MHz. The relatively low update frequency of 64 MHz results in a significant reduction in power consumption compared to previous AFIR designs [7, 9, 11]. However, it results in aliases at integer multiples of 64 MHz. We choose to *allow* these aliases, because they are severely suppressed by the sinc notches of the windowed integration and can easily be made negligible by a first-order pre-filter.

A significant part of the power consumption is in the buffers between the DFFs and the g_mDAC. The g_mDAC is updated at 64 MHz but only turns fully on/off once per 2 µs. Hence, the power consumption of these buffers can be reduced by implementing the g_mDAC thermometer coded. 5 bits are implemented in thermometer code resulting in approximately 2.7× less power consumption of these buffers compared to a fully binary g_mDAC. Additionally, the filter stopband rejection becomes less (timing) mismatch sensitive.

The capacitor control phases are made by dividing the 64 MHz clock plus some pulse generation logic. All these

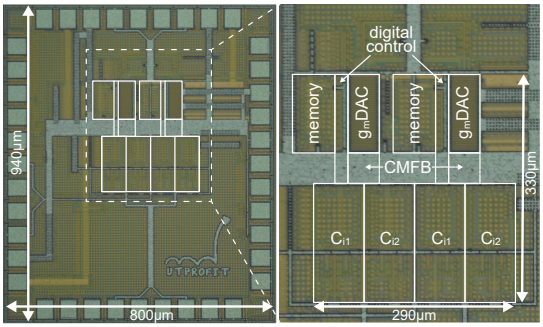

Fig. 4. Chip photo indicating filter blocks.

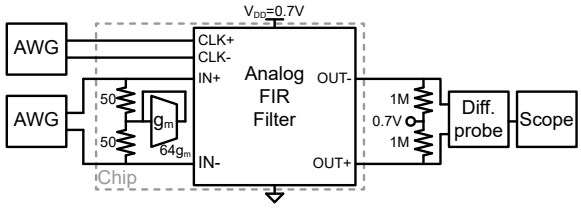

Fig. 5. Measurement setup.

control phases are re-clocked in DFFs to synchronize timing. Changing the filter bandwidth —- by inversely proportionally varying T_i — changes the filter gain, according to (1). In this proof-of-concept, the gain variation can be compensated up to 4x by a variable part of the integration capacitor (implemented differentially, not shown). In the targeted application, the capacitors could be reused as e.g. sampling capacitor of a SAR ADC or the output could be re-sampled on a different capacitor.

The inverter-C implementation allows for a low supply voltage, making the filter very suitable for state-of-the-art and future process nodes. Additionally, the digital power of the filter is low and scales with technology.

IV. Experimental Results

A prototype of the AFIR was designed and fabricated in a 22 nm FDSOI process. The chip operates at a 700 mV supply voltage and has an active area of 0.09 mm^2. The FIR code is a Chebyshev window with code pre-correction — which compensates for charge leakage through the g_mDAC output resistance during integration (ϕ_i); an extension on [13]. Fig. 4 shows the chip photo indicating its major blocks.

A. Measurement Setup

Fig. 5 shows the measurement setup. The input voltage and the 64 MHz clock are provided by Arbitrary Waveform Generators (AWGs) with a differential output. The input common-mode voltage is set by on-chip self-biased g_m-cells. A differential 50 Ω input match is provided to allow characterization of the AFIR up to RF frequencies. The output samples are only available half of the time, because ϕ_s and ϕ_r partially overlap. In this way, the capacitances of the measurement probe and pcb are also reset to avoid an extra undesired IIR filtering by averaging subsequent output samples. The output bias network compensates for the resistive common-mode loss of the probe.

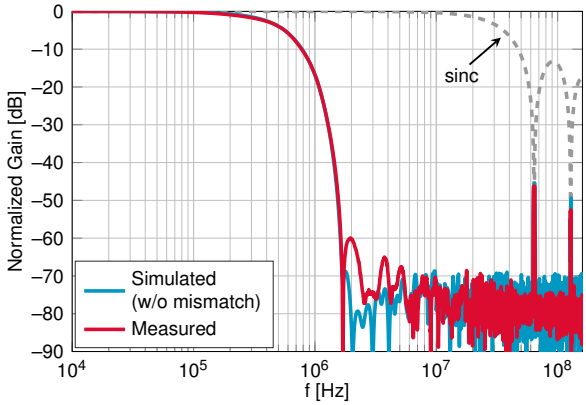

Fig. 6. Measured normalized transfer at a bandwidth of 0.43 MHz.

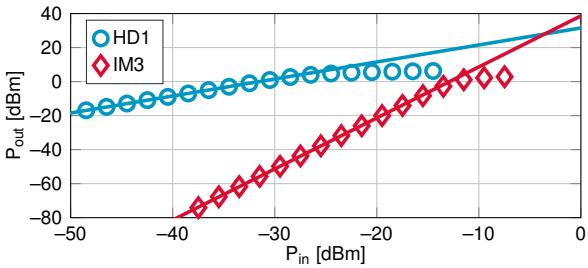

Fig. 7. Measured out-of-band OIP3 and in-band compression.

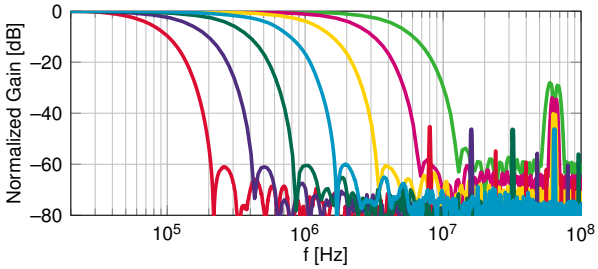

Fig. 8. Filter transfer for different bandwidth settings.

B. Measurement Results

The filter bandwidth is set to 0.43 MHz for all measurements, unless specified otherwise. The measured normalized filter response is shown in Fig. 6. It is very close to simulation, including the very steep roll-off — resulting in a ratio of only 3.8 between the 60 and 3 dB suppression frequencies. The measured stopband rejection of 60 to 75 dB is as expected from extensive mismatch analysis of the g_mDAC. The sinc notches suppress the aliases at 64 and 128 MHz by >45 dB, as expected from (1).

Fig. 7 shows the measured in-band gain and IM3 for out-of-band signals at 5.01 and 9.98 MHz. The out-of-band (OOB) output referred third-order modulation point (OIP3) is 28 dBm and the output referred 1-dB compression point (OP_{1dB}) is 3.7 dBm. Both OIP3 and OP_{1dB} are defined below Table I. The input referred noise level (IRN) is 12 nV/$\sqrt{}$Hz; averaged across 0.01-0.43 MHz.

The total power consumption of the AFIR filter is 92 µW, consisting of: g_mDAC 39 µW, memory 36 µW and digital control 17 µW (including g_mDAC enable buffers). An 'of-the-shelf' memory was implemented; not specially tailored for this design, allowing for further power optimization.

Fig. 8 shows the normalized filter transfer for different bandwidths. The bandwidth is reduced by proportionally low-

TABLE I
COMPARISON SUMMARY

	This work	[6] VLSI'17	[9] JSSC'13	[4] JSSC'14	[3] JSSC'09	[1] JSSC'10	[2] CICC'17	[5] TCAS-I'18
Topology	128-tap AFIR	Analog IIR	Cascaded AFIR	Analog IIR	Opamp RC	g_m-C	g_m-C	Analog IIR
Supply voltage [V]	0.7	1.2	1.2	1.2	0.55	2.5	1.3	1.8
Power cons. [mW]	0.092	0.15	8.4	1.98	3.5	1.26	0.65	4.3
$f_{-3\mathrm{dB}}$ [MHz]	0.06-3.4[a]	0.54	5-26	0.4-30	11.3	2.8	20	0.49-13.3
$f_{-60\mathrm{dB}}/f_{-3\mathrm{dB}}$	3.8	10[b]	1.5[c]	7.8[c]	-	5.9[b]	4.8[c]	7.5[c]
Gain [dB]	31.5	0[c]	41	9.3	0	15	0	17.6
IRN [nV/$\sqrt{\text{Hz}}$]	12	23.3	12	4.57	33	23	15.3	6.54
OP_{1dB}[e][dBm]	3.7	-	-	10	-0.5	-	6.3	12.93
OOB OIP3[f][dBm]	28	55.1	13[d]	21	13	50.6	28.8[d]	32.63
Technology	22 nm FDSOI	130 nm CMOS	65 nm CMOS	65 nm CMOS	130 nm CMOS	90 nm CMOS	180 nm CMOS	180 nm CMOS
Active Area [mm^2]	0.09	0.06	0.52	0.42	0.43	0.5	0.12	2.9

[a] Other specifications are measured at 0.43 MHz (Fig. 6); [b] Extrapolated from figure; [c] Estimated from figure;
[d] In-band; [e] OP_{1dB} = P_{1dB} + Gain - 1; [f] OIP3 = IIP3 + Gain.

ering f_w; at the cost of a more close-in alias (at f_w) and proportionally lower output sample rate f_s, but less digital power consumption. The bandwidth is increased by a proportionally higher f_s for constant f_w; reducing the number of FIR coefficients per T_i. In this way, the power consumption increases by only 10% for a 3.4 MHz bandwidth with respect to the nominal 0.43 MHz. The stop-band rejection and alias suppression reduce. The bandwidth can be tuned from 0.06 to 3.4 MHz — a range of 57×.

C. Comparison

Table I summarizes the filter performance and compares this work to power efficient state-of-art filters with different topologies. This work realizes best power per SNR performance while also providing very steep filtering, good linearity and small active chip area.

V. CONCLUSION

A novel analog FIR filter architecture is proposed as channel selection filter. It consists of a hardware efficient implementation that requires only two pseudo-differential transconductor DACs and four integration capacitors to obtain a 128-tap FIR filter (area: 0.09 mm^2). Power consumption is reduced by allowing for a lower FIR coefficient update rate and by partially implementing the DAC thermometer coded. This results in a best-in-class SNR per power (only 92 µW), while also providing a very sharp transition band ($f_{-60\mathrm{dB}}/f_{-3\mathrm{dB}} = 3.8$) and good linearity (OIP3 = 28 dBm). The bandwidth can be accurately tuned from 0.06 to 3.4 MHz without significantly increasing the power consumption.

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