Integration of Solar Cells on Top of CMOS Chips—Part II: CIGS Solar Cells

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Abstract—We present the monolithic integration of deep-submicrometer complementary metal–oxide–semiconductor (CMOS) microchips with copper indium gallium (di)selenide (CIGS) solar cells. Solar cells are manufactured directly on unpackaged CMOS chips. The microchips maintain comparable electronic performance, and the solar cells on top show an efficiency of $8.4 \pm 0.8\%$ and a yield of 84%, both values being close to the glass reference. The main integration issues, i.e., adhesion, surface topography, metal ion contamination, process temperature, and mechanical stress, can be resolved while maintaining standard photovoltaic processing. A tight process window is found for the manufacturing of CIGS solar cells on the CMOS side of the microchip. More process margin exists for backside integration.

Index Terms—Complementary metal–oxide–semiconductor (CMOS), copper indium gallium selenide (CIGS), energy harvesting, monolithic integration, photovoltaic (PV) cells, scavenging, smart dust, solar cells.

I. INTRODUCTION

AS DETAILED in part I of this paper, the integration of a thin-film solar cell on a microchip may be a compact and powerful solution to the open issue of energy harvesting for autonomous wireless sensor systems ("Smart Dust"). In this part, we consider the integration of copper indium gallium (di)selenide (CIGS) solar cells using a similar experimental approach, as presented for the a-Si cells in part I.

$Cu(In_{1-x}Ga_x)Se_2$ (CIGS) is a semiconducting I-III-VI$_2$ compound with chalcopyrite crystal structure [1]. The absorption coefficient of CIGS is very high: a 1-μm CIGS film suffices for absorption of all impinging light [2]. The technology has reached maturity: CIGS solar panels are now commercially available with efficiencies of about 15% [3].

The monolithic integration of CIGS on complementary metal–oxide–semiconductor (CMOS) is more challenging than that of a-Si. In standard manufacturing processes, the peak temperature (> 500 °C [4]) is (just) too high for CMOS interconnect. Related is the issue of thermal expansion mismatch between the solar cell and the substrate, possibly leading to cracks. Last but not least, high-efficiency CIGS solar cells require sodium concentration of more than 0.5% in the active

layer [5], [6], whereas sodium is known to be the most detrimental contamination in CMOS devices [7].

However, good reasons for pursuing CIGS monolithic integration exist. Of all single-junction thin-film solar cells not employing a monocrystalline semiconductor, CIGS cells exhibit the highest cell efficiency ($20.3 \pm 0.6\%$) and module efficiency ($15.7 \pm 0.5\%$) [3]. The band gap of the CIGS solar cell can be tuned between 1.1 and 1.7 eV by varying the Ga:In ratio [8]. This allows band-gap tuning for maximum efficiency at the indoor light spectrum. The efficiency at indoor light intensity is reportedly larger than 5% [9]. Last but not least, very good long-term reliability and radiation hardness are further reported for this type of thin-film solar cell [10].

First work on the integration of CIGS *material* on top of CMOS was presented in [11]. In our recent paper [12], we presented the first results on monolithic integration of CIGS *solar cells* on top of unpackaged 0.13- and 0.25-μm CMOS microchips.

In this paper, we expand the discussion on process integration issues. Additional experiments are shown to quantify the substrate topography's impact on solar cell performance. We also present new CIGS-on-CMOS integration experiments, including fabrication on a 0.18-μm technology chip. The new experiments show improved photovoltaic (PV) efficiency and higher yield on CMOS chips. This paper starts with a discussion of the integration challenges (Section II), followed by the process integration scheme (Section III). PV performance is documented in Section IV; CMOS performance is discussed in Section V, followed by the conclusions.

II. CIGS INTEGRATION CHALLENGE

For the final microsystem, we want the PV efficiency to be as high as possible and the CMOS chip's functionality to be unaffected. Five integration challenges must be overcome to achieve these goals.

First, good adhesion between the solar cell and the underlying CMOS chip is a necessity. The first PV layer on glass plates is molybdenum. In our previous work [12], we found that Mo deposited by the standard two-stage magnetron sputtering [13] can have good adhesion on glass but adheres poorly on our CMOS chips (using only wet cleaning as surface preparation). In our new experiment, a 10-nm titanium layer was deposited prior to Mo deposition to resolve this problem. The resulting layers passed the Scotch tape test [14].

Second, sodium and copper are necessary constituents in CIGS solar cells. However, these metals exhibit fast diffusion coefficients in intermetal dielectrics and silicon and are active
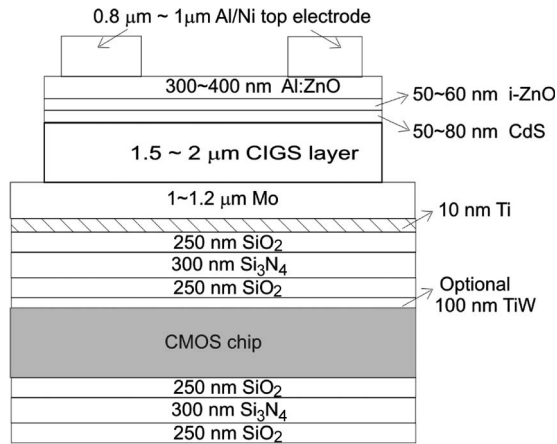
Fig. 1. Schematic view of a CIGS solar cell fabricated on top of a CMOS chip (not to scale). The 100-nm TiW layer is only applied to Cu-PCM chips as an etch-stop layer. Compared to our previous work [12], 10-nm Ti is administered between the top SiO$_2$ and the bottom Mo electrode for better adhesion. In these experiments, no interconnection was made between solar cell and CMOS.

as mobile charge and as band-gap defects [7], [15]. Hence, a diffusion barrier must be administered between the microchip and the solar cell. Si$_3$N$_4$ is widely used as diffusion barrier layer against mobile ions [16], and in our experiments, we have employed 300-nm plasma-enhanced chemical vapor deposition (PECVD) of Si$_3$N$_4$ to this purpose.

Third, the standard CIGS solar cell processing involves necessary plasma processes, which may cause plasma charging damage to the underlying transistors [17]. It is however known that a 150–200-nm dielectric layer can block possible plasma-charging damage [18]; hence, the diffusion barrier layer previously mentioned serves a second purpose.

The peak process temperature is the fourth concern. The highest CIGS efficiencies are obtained using process temperatures of 500 °C–550 °C [19]. CMOS backend interconnect, particularly Al-based interconnect, cannot withstand such temperatures, leading to crack voiding, hillock formation, and corrosion [20]. Some CIGS literature however reports quite good solar cell performance at reduced processing temperature in the range of 310 °C–450 °C [21].

Finally, the added solar cell layer may have intrinsic stress, which will be imposed on the underneath CMOS circuits, thus influencing the performance of the chip [22], [23]. CIGS experiments on a variety of substrates have shown that the mismatch in thermal expansion between substrate and CIGS can lead to CIGS adhesion problems and the cracking of Mo [21].

The Mo-adhesion issue can be monitored by visual inspection, combined with a Scotch tape test. Proper PV performance and unaffected CMOS functionality are the best evidence of the resolution of the other four issues, as detailed in Sections IV and V.

III. Prototype Design and Experiment

In Fig. 1, a schematic cross-sectional view of a CIGS solar cell that is integrated on the front side of a CMOS chip is shown. The solar cell can also be integrated on the backside of the chip.

The experimental process flow is as given in Part I after the CMOS electrical characterization, the chips were passivated, followed by the conventional CIGS solar cell process. After the PV characterization of the realized solar cell, the solar cell stack and the passivation layers were removed from some of the CMOS chips in order to test the CMOS chip again.

The solar cells are deposited on soda-lime glass reference plates, 0.13-μm CMOS chips containing process control modules (labeled Cu-PCM), 0.18-μm CMOS chips containing ring oscillator (RO) structures (labeled Ringo), and 0.25-μm CMOS chips with a fully functional 1.6×1.4 cm^2 mixed-signal CMOS circuit [24] (labeled Timepix). Different from the a-Si solar cell integration presented in Part I, no benzocy-clobutene (BCB) planarization was utilized before passivation, because BCB cannot withstand the peak temperature of the CIGS solar cell process.

A. Passivation Layer Deposition

Before the solar cell integration, a passivation layer is deposited on the chip surface. The layer stack consists of SiO$_2$, Si$_3$N$_4$ and SiO$_2$ deposited by PECVD at 300 °C. A thin TiW layer is added underneath, acting as an etch-stop layer for deprocessing the stack later on without affecting the CMOS upper layers. It was found that the upper layer of SiO$_2$ leads to much better adhesion of the following layers than Si$_3$N$_4$. After the chip passivation, the chips are annealed at 425 °C in N$_2$ ambient to release the abundant H$_2$. A slight change in transistor parameters can be expected from these process steps, because PECVD Si$_3$N$_4$ deposition and the subsequent annealing in nitrogen influence the hydrogen passivation of the Si-SiO$_2$ interface in metal–oxide–semiconductor (MOS) transistors [25].

B. Solar Cell Deposition

The CIGS solar cells were realized by Nankai University using the three-stage co-evaporation process documented in [4] and [26]. Compared to our previous work [12], in the new experiment, first a 10-nm Ti layer is sputtered to improve Mo adhesion, followed by 1–1.2-μm Mo deposition by magnetron sputtering in the same reactor. Then, a 20–30-nm NaF precursor layer was thermally evaporated in order to supply Na to the following CIGS absorber layer, which is necessary for efficient CIGS solar cells [5]. After that, the p-type CIGS absorption layer was co-evaporated by the three-stage method [4] onto the Mo-coated CMOS chips and glass substrate in the same chamber without vacuum break. The n-type buffer layer of CdS was deposited by chemical bath deposition at 80 °C; then, a 50-nm intrinsic ZnO (i-ZnO) layer and 300-nm Al doped ZnO (ZnO:Al) were sequentially deposited by radio-frequency magnetron sputtering as window layers. Finally, the nickel–aluminum top electrode grid was thermally evaporated onto the device.

For this paper, the finished solar cells have an active area of about 0.29 cm^2.

C. Deprocessing of the Solar Cells

After the characterization of the obtained solar cells, the solar cell layers and the passivation layers on some CMOS chips
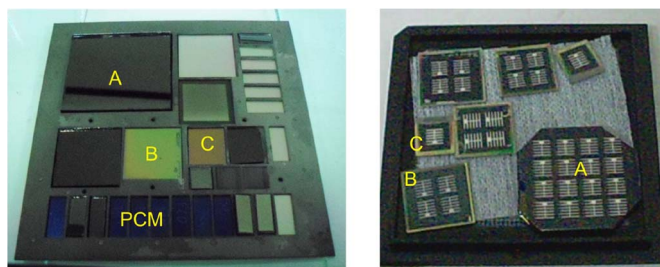
Fig. 2. (Left) 10×10 cm^2 sample holder for different types of samples for CIGS solar cell deposition experiments. (Right) Finished samples with CIGS solar cells on top. In both images, A, B, and C denote the glass reference plates, Cu-PCM chips, and Timepix chips, respectively. Additional test samples are included in the same run.

Fig. 4. HIM image of the CIGS solar cell layers on a Timepix chip. The columnar polycrystalline structure of different layers can be distinguished in the picture.
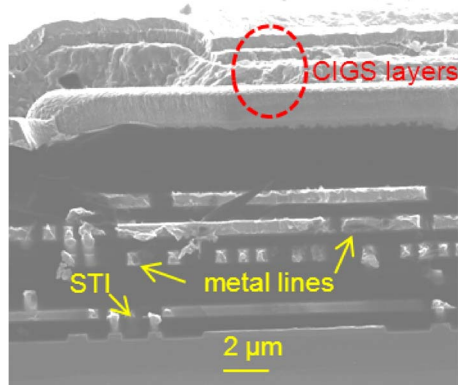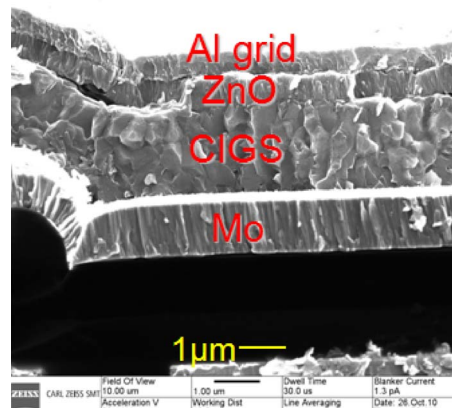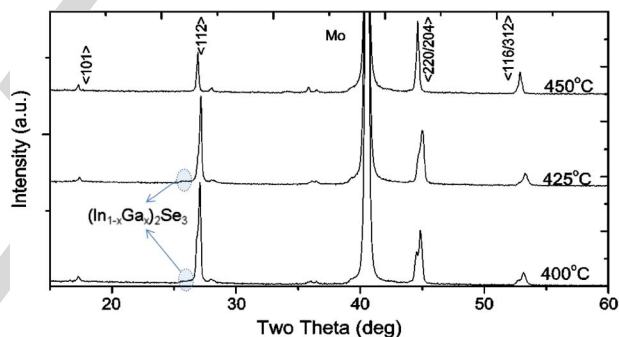

Fig. 3. HIM picture of the CIGS solar cell on top of the Timepix. (Bottom to top) Chip's shallow trench isolation and interconnect are visible, followed by the CIGS solar cell layer stack.

Fig. 5. XRD data of CIGS on glass fabricated at 400 °C–450 °C. A peak around $2\theta = 27°$ is visible in the 400 °C and 425 °C deposited films, indicating the existence of $(In_{1-x}Ga_x)_2Se_3$. For 450 °C, the corresponding $(In_{1-x}Ga_x)_2Se_3$ peak is not present, pointing to improved film crystallinity.

were removed to expose the bond pads of the test structures. For deprocessing, HCl was used to remove the Al-Ni, ZnO:Al, and CdS; fuming nitric acid was applied for etching the CIGS absorber layer and the Mo bottom electrode; BHF was used for removing SiO_2 and Si_3N_4; and hydrogen peroxide was used to remove the TiW.

D. Physical Characteristics of the CIGS Solar Cell on CMOS Chip

Fig. 2 shows the integrated PV cells on different-type CMOS chips and PCMs. On the left-hand side, the chips are visible as mounted into the chip holder prior to postprocessing. The right-hand side image shows the samples after solar cell manufacturing.

Figs. 3 and 4 show helium ion microscope (HIM) [27] cross sections of the CMOS chips with solar cells on top. In Fig. 3, we can see the metal levels of the Timepix chips and the layer-by-layer structure of the CIGS solar cell on top of the CMOS chips. The CMOS has some topography (approximately 1 μm), as visible from the nonplanar solar cell thin films. The figure suggests that the step coverage of the solar cell layers is sufficient to cope with this topography, but electrical results should give more conclusive evidence in this respect.

Fig. 4 illustrates the crystal structure of the Mo, CIGS, ZnO, and Al grid. The Mo and CIGS have a columnar polycrystalline structure. The grain size of the Mo layer is about 60 nm,

as derived from X-ray diffraction (XRD) data using the Scherrer equation. The grain size of the CIGS is well above half a micrometer, which can be observed by top-view HIM microscopy. A detailed analysis is reported elsewhere [28]. These grain sizes depend on the process conditions [29], [30]. The obtained values are suitable for good CIGS solar cell performance.

IV. SOLAR CELL EXPERIMENTAL RESULTS

In this section, we present the solar cell performance, comparing the cells on CMOS with the reference cells on glass. The material properties and the current-voltage behavior under light illumination are compared.

A. Crystallinity and Chemical Composition of the CIGS Layer

The crystallinity and the chemical composition of the CIGS layer of the samples were measured by XRD and X-ray fluorescence (XRF) analysis, respectively.

From Fig. 5, we see in the 400 °C and 425 °C fabricated CIGS solar cells an indication of the existence of $(In_{1-x}Ga_x)_2Se_3$. This is commonly attributed to a lack of thermal activation energy, and a reduced solar cell efficiency may result [12], [31]. For a higher temperature of 450 °C, the

TABLE I
CHEMICAL COMPOSITION BY XRF OF CIGS LAYERS DEPOSITED ON
VARIOUS SUBSTRATES AND AT DIFFERENT TEMPERATURES

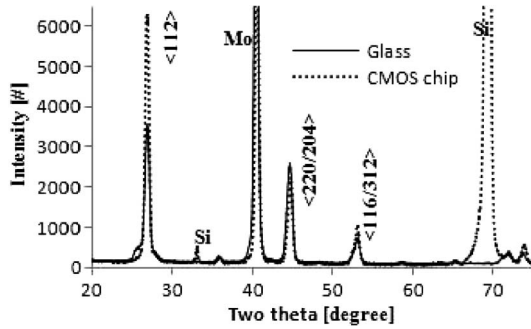| T (°C)	substrate	Cu (at.%)	In (at.%)	Ga (at.%)	Se (at.%)	Cu/ (In+Ga)	Ga/ (In+Ga)
	Expected	22-24	19-20	6-7	50-51	0.88-0.91	0.25-0.27
400	Glass	22.8	18.7	7.6	51.0	0.87	0.29
	CMOS	22.5	18.0	8.2	51.2	0.86	0.31
425	Glass	22.4	18.9	7.5	51.2	0.85	0.28
	CMOS	23.4	18.5	7.1	51.1	0.84	0.28
450	Glass	23.6	20.8	4.8	50.2	0.92	0.19
	CMOS	22.7	21.5	4.4	50.3	0.87	0.17

Fig. 6.   XRD data comparison of CIGS on glass substrate and that on Cu-PCM substrate fabricated at 425 °C in the same run. Except two peaks from the Si $\langle 100 \rangle$ substrate, the diffraction peaks coincide.

225 corresponding $(In_{1-x}Ga_x)_2Se_3$ peak is not present, pointing to
226 improved film crystallinity. The $\langle 112 \rangle$ peak at 450 °C shifts
227 to a lower number, compared with the same peaks at other
228 temperatures. This indicates a lower incorporation of Ga [32],
229 which can be confirmed by XRF measurement of Ga ratio, as
230 shown in the last column of Table I.

231   Fig. 6 shows the XRD data of the CIGS fabricated at 425 °C
232 on CMOS substrate and on glass substrate. Disregarding the
233 two peaks from the Si $\langle 100 \rangle$ substrate, the diffraction peaks
234 coincide. However, the peak ratio between $\langle 220/204 \rangle$ and the
235 $\langle 112 \rangle$ on CMOS is smaller than that on glass, which will result
236 a lower efficiency solar cell on the CMOS chip [33], [34].

237   Table I shows the atomic chemical composition (at.%) of
238 CIGS on various substrates and deposited at various temper-
239 atures. The "expected" row indicates the aimed (i.e., providing
240 best efficiency) composition [33]. In each run (i.e., deposition
241 temperature), the compositions on glass and on CMOS are
242 almost identical and are close to the optimum.

243   From a comparison of the XRD and XRF analyses of the
244 CIGS layers, we conclude that an identical crystallinity and
245 chemical composition can be obtained on CMOS and on glass.
246 However, below 450 °C peak deposition temperature, there is
247 residual $(In_{1-x}Ga_x)_2Se_3$ from the first stage of the three-stage
248 co-evaporation method [4], [31], and the crystal orientation
249 changes; both effects may lead to lower solar cell efficiency.

B. Current–Voltage Behavior of the Solar Cells

251   Current density-voltage (J–V) measurements have been
252 done to characterize solar cells on the reference glass sub-
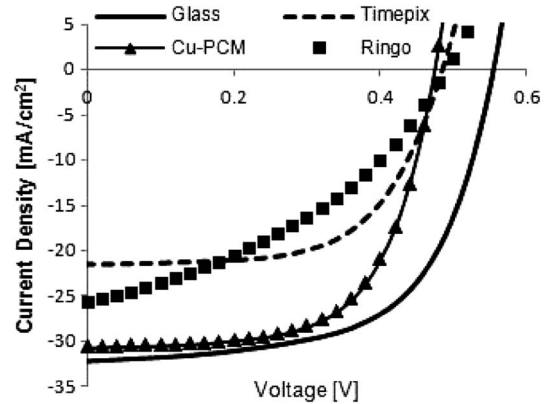253 strate and on the CMOS chips. The measurements were per-

Fig. 7. J–V curves of the highest efficiency solar cells fabricated at 425 °C peak temperature, on glass and on different generation CMOS chips, i.e., Cu-PCM (0.13-μm), Ringo (0.18-μm), and Timepix (0.25-μm).

TABLE II
PARAMETERS OF CIGS SOLAR CELLS ON DIFFERENT SUBSTRATES
AT 425 °C PEAK SUBSTRATE TEMPERATURE

Substrate	η	J_{sc} mA/cm^2	V_{oc} V	FF	R_s Ω cm^2	R_p Ω cm^2
Glass (reference)	10.9%	32.19	0.55	0.61	3.0	238.6
Cu-PCM backside	9.2%	30.74	0.48	0.63	2.8	515.1
Ringo	4.9%	25.65	0.49	0.39	8.0	51.9
Timepix	6.4%	21.48	0.48	0.61	4.2	289.5

formed under standard solar-simulator illumination conditions: 254
100 mW/cm^2 (Air Mass 1.5).   255

Fig. 7 shows the J–V curves of the best-performing PV 256
cells on each substrate type. These samples are processed at 257
425 °C peak substrate temperature in the same run. From the 258
J–V curves, the important parameters characterizing the PV 259
solar cell performance were extracted and listed in Table II. 260
On all types of CMOS chips, efficiencies η of 4.9% or higher 261
are obtained. The solar cell efficiency on Cu-PCM chips ap- 262
proaches that on glass.   263

All three chips exhibit almost identical open voltages V_{oc}; 264
the short-circuit currents (J_{sc}) of the solar cells on Ringo and 265
Timepix chips are however smaller. This might be related to 266
the high topography variation (i.e., step height) initially present 267
on the chip's surface before postprocessing. The Ringo chip 268
has the highest topography variation, with 1.5-μm excursions. 269
Insufficient step coverage of one of the solar cell layers will 270
lead to increasing the cell's series resistance R_s or shunting the 271
layers electrically, i.e., decreasing the parallel resistance R_p and 272
fill factor FF. Indeed, the solar cells on the Ringo chip exhibit 273
both (See Table II).   274

The quality of the CIGS solar cell is related to the substrate 275
temperature during the deposition [34], [35]. This is because 276
a higher substrate temperature implies higher thermal energy 277
available for better activation of the layer-formation process. In 278
the studied temperature range of 400 °C–450 °C, this leads to 279
a better crystal structure of the CIGS layer, as follows from the 280
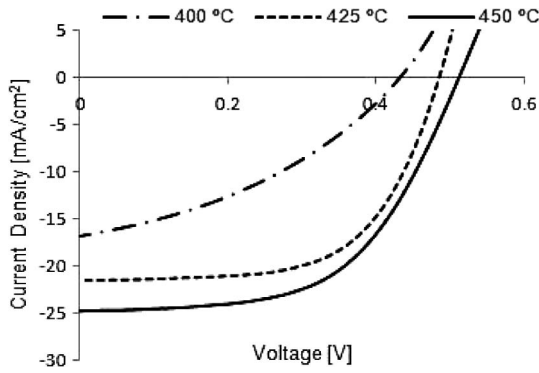XRD results presented in Section IV-A. Fig. 8 and Table III 281

Fig. 8. *J–V* characteristics of solar cells on top of the Timepix chip. With increasing deposition temperature, the solar cell performance improves: both J_{sc} and V_{oc} increase.

TABLE III
PARAMETERS OF CIGS SOLAR CELLS ON TIMEPIX CHIP AT DIFFERENT PEAK SUBSTRATE TEMPERATURES

Substrate T (°C)	η	J_{oc} mA/cm^2	V_{oc} V	FF	R_s $\Omega\,cm^2$	R_p $\Omega\,cm^2$
400	2.7%	16.8	0.44	0.37	13.6	79.5
425*	6.4%	21.48	0.48	0.61	4.2	289.5
450	7.1%	24.72	0.51	0.56	5.53	875.4

TABLE IV
EFFICIENCY COMPARISON OF THE PV CELLS ON GLASS AND ON CMOS CHIP

	Cell 1	Cell 2	Cell 3	Cell 4	average
Glass	6.8%	10.8%	10.0%	9.1%	9.2±1.7%
CMOS	8.2%	8.6%	7.2%	9.2%	8.3±0.8%

confirm improved solar cell behavior at higher deposition temperatures.

C. Efficiency and Yield

Several equal-size (22×22 mm^2) glass and Cu-PCM chips, which have good Mo adhesion due to the 10-nm Ti adhesion layer, were mounted into the chip holder for the solar cell fabrication at 425 °C. The efficiency values of the solar cells on one glass plate and a Cu-PCM chip are listed in Table IV. All efficiencies on CMOS now are higher than the best efficiency reported earlier for CIGS on CMOS (7.1%) [12]. (The CIGS solar cells on CMOS chips in [12] were without the Ti adhesion layer.) Furthermore, the efficiency gap between the CMOS chip and the glass reference has decreased from 1%–5% [12] to 0.9% in the new experiments.

If we consider < 4% efficiency as the failure criterion, the yield on CMOS chips of work [12] was generally less than 50% due to the poor Mo adhesion. The extra Ti layer added in this work, compared with [12], resulted in the improved adhesion of Mo and, therefore, in the higher solar cell yield on CMOS chips. In this paper, the yield on CMOS chips of this work reaches 84% (five bad cells out of 32), and that on glass substrate is 88% (four bad cells out of 32).

In terms of both efficiency and yield, these differences between glass and CMOS chip can be considered marginal.
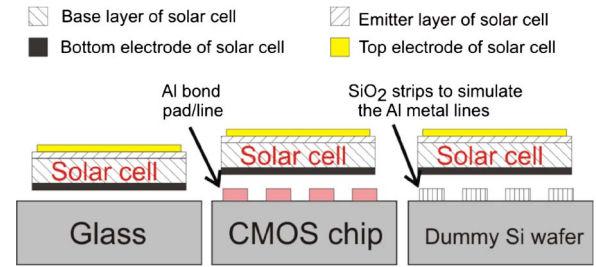

Fig. 9. Schematic diagram of substrates with different surface profile amplitudes. (Left) Glass substrate. (Middle) Standard CMOS chip, with Al bond pads and lines embedded in the Si_3N_4 scratch protection layer. (Right) Dedicated test samples with PECVD SiO_2 strips of different thicknesses (50–550 nm). For CIGS solar cells, Mo is the bottom electrode, and Al is the top electrode.
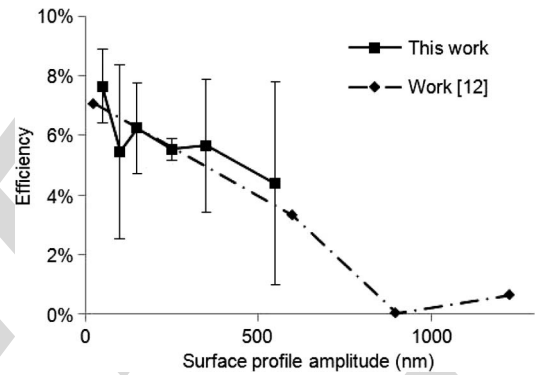

Fig. 10. Efficiency against surface profile amplitude. The previous work presented single measurements; hence, no error bars were determined. All samples are fabricated at 425 °C.

D. Efficiency of PV Cells Versus Chip Topography

As discussed in our previous paper [12] and in Part I, the efficiency of the solar cell is closely related to the surface profile amplitude and the Mo adhesion. Dedicated experiments were conducted to further investigate and quantify this phenomenon.

Fig. 9 shows a sketch of the additionally fabricated test samples (right image) used to investigate the influence of the substrate surface profile amplitude. PECVD SiO_2 stripes are used to simulate typical interconnect topography on CMOS chips. The width and spacing of the SiO_2 strips are 20 μm, giving an area coverage of ~50%. The thickness of the oxide varies from 50 to 550 nm. On each of the test samples, after Ti and Mo deposition, four CIGS solar cells are deposited.

Fig. 10 shows the averaged efficiency of the cells at different surface profile amplitudes (i.e., the thickness of the SiO_2 stripes). A slight gradual efficiency drop seems to occur with increasing topography, quantitatively in line with the earlier findings.

V. CMOS CHIP PERFORMANCE AFTER THE SOLAR CELL INTEGRATION

In this section, the CMOS functionality after CIGS solar cell integration will be addressed. We report on the MOS capacitance–voltage and current–voltage characteristics; the behavior of ROs; and the functionality of the mixed-signal Timepix microchips. In all cases, the same functionality tests
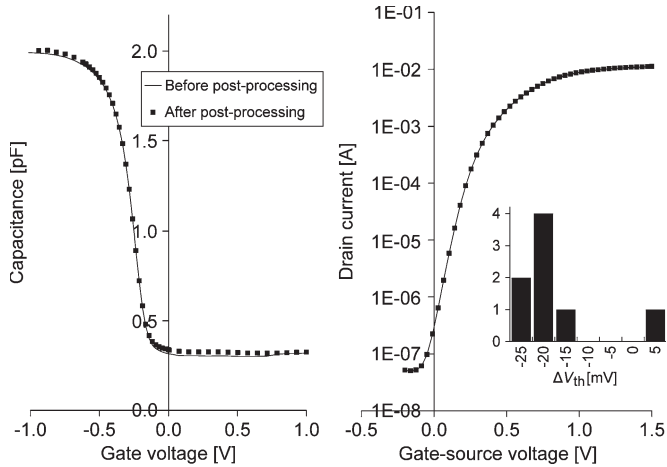
Fig. 11. (Left) C–V curves of a MOS capacitor before and after CIGS solar cell integration on chip's front-side at 400 °C. (Right) I_D–V_{GS} curves of an n-channel MOS transistor before and after the same postprocessing. The inset shows threshold voltage shift statistics of eight transistors.

TABLE V
FUNCTIONAL TESTING OF MOS CAPACITORS AND MOSFETs ON Cu-PCM CHIPS AFTER POSTPROCESSING STEPS. THE *FRONT* ROW STANDS FOR FRONT-SIDE INTEGRATION OF THE CELLS; *BACK* MEANS BACKSIDE INTEGRATION

		400 °C CIGS	425 °C CIGS	450 °C CIGS	450 °C CIGS (no NaF)	450 °C 30 min anneal
ΔV_{FB} (mV)	*Front*	-9	(no data)	-4	-4	-9
	Back	-6	-12	-10	-4	
ΔV_{th} (mV)	*Front*	-21	-39	-26	-26	-20
	Back	-21	-20	-25	-23	
ΔS (mV/dec)	*Front*	-1.4	-1.0	-1.3	-1.3	-1.2
	Back	-1.6	-1.4	-0.4	-1.3	

are carried out before and after solar cell deposition and removal, and compared.

A. C–V and I–V Measurements on Cu-PCM Devices

The capacitance–voltage (C–V) curves of MOS capacitors and the current–voltage (I–V) curves of MOS transistors were measured using a Keithley 4200 semiconductor characterization system and a Karl Suss PM8 low-leakage probe station at the University of Twente. The Cu-PCM devices, with bond pads across the chip, had to be deprocessed before electrical retesting (see Section III-C).

The MOS capacitor area was 1.44×10^{-6} cm^2 with an oxide thickness of 2.2 nm. The capacitance measurements were carried out at a frequency of 1 MHz. The MOS field-effect transistor (MOSFET) under study has a gate length of 130 nm. The transistor source and body were grounded, and the gate and drain potentials were varied for the transistor measurements.

For an illustration, in Fig. 11, we present the C–V and I_D–V_{GS} curves of the individual devices after 400 °C CIGS front-side integration. For all CIGS process conditions, the key device parameters studied are summarized in Table V. It lists the changes in flatband voltage V_{FB}, threshold voltage V_{th}, and subthreshold swing S. Only small changes in the device parameters are observed. They are most likely governed by
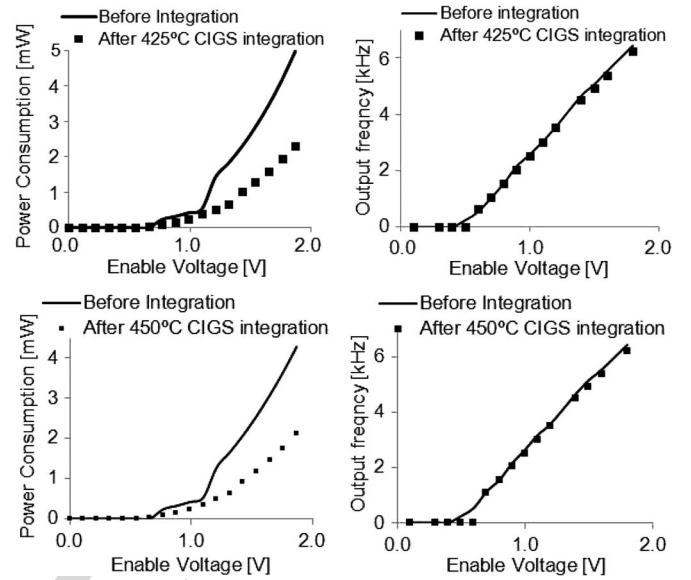

Fig. 12. (Left) Power consumption and (right) output frequency at different enable voltages of the RO before and after CIGS solar cell integration at (top) 425 °C and (bottom) 450 °C peak temperatures. The ring oscillator is read out via an embedded 512-time frequency divider.

the added thermal budget. This is supported by the control experiment where the chips were exposed to the same thermal budget but without CIGS stack deposition (see the last column of Table V).

An experiment where NaF deposition was skipped, to isolate a possible detrimental influence from Na contamination, yielded quite similar results as the others (Table V labeled "No NaF"). Quantitatively, the changes are comparable to packaging-related parameter shifts [22]. From Table V, we can conclude that ionic contamination, if at all present, is at most 10^{10} cm^{-2} (based on the highest found value of ΔV_{FB} [7], [36]). In summary, the 0.13-μm CMOS PCM chip does not show a significant influence of the solar cell integration to device parameters.

B. Functionality of the Ringo Chip

A RO is widely used as a tool to characterize the performance of MOSFETs [37]. In our experiments, the power consumption and the output frequency versus the enable voltage of the 17-stage RO have been measured before and after the solar cell integration by Keithley SCS 4200 and Agilent/HP 54642A oscilloscope. In this case, the solar cell was deliberately placed beside the RO test structure. Hence, no deprocessing of the solar cell was required to do the final CMOS test. The results are shown in Fig. 12.

One can observe that there is little impact of the integration on the RO frequency. However, the power consumption does show a change after postprocessing, likely due to threshold voltage shifts.

C. Functionality of Timepix Chip

The Timepix chip is a mixed-signal CMOS chip manufactured in 0.25-μm CMOS technology. It is designed to be ball-grid connected to a semiconductor sensor layer (e.g., CdTe)

Process Condition		400 ºC CIGS	425 ºC CIGS	450 ºC CIGS	450 ºC CIGS (No NaF)	450 ºC 30 min anneal
Digital functional column	*Front*	254→228	malfunction	malfunction	malfunction	252→252
	Back	253→253	253→253	247→233	(no data)	
Analog functional Column	*Front*	254→212	malfunction	malfunction	malfunction	252→252
	Back	253→252	253→253	247→232	(no data)	

for 2-D X-ray imaging, but in this work, it is utilized in its bare form. It contains an array of charge-sensitive preamplifiers with related in-pixel processing and storage electronics.

The Pixelman software [38] and an automated probe station were employed for functional testing of the Timepix chips at the Nikhef Institute in Amsterdam (NL). The program tests the functionality of the 256 columns of 256 pixels. Each pixel contains 550 transistors. It should be noted that the post-processed chips were of a lower quality category than those normally used. A fraction of the pixels and columns therefore malfunctions before solar cell integration. A summary of the test results is presented in Table VI.

The values listed in the table give the number of columns (out of 256) passing the functionality test before and after postprocessing. Good results are obtained with all backside-processed Timepix chips, with the front-side processed chip at 400 °C and with the reference experiment where the chip is only exposed to the additional thermal budget. Chips with backside-deposited CIGS (up to 425 °C) maintain full functionality.

The chip functionality is however adversely influenced when CIGS solar cells are produced on the front side of the chip. The chip loses part of its functionality at 400 °C and malfunctions entirely at higher process temperatures. Some functionality loss is also observed on the 450 °C backside-processed chips. It is concluded that the process window for front-side integration is very tight; the peak temperature should remain around or even below 400 °C. For backside integration, the allowable peak temperature is about 50 °C higher and matches the required temperature for high-efficiency CIGS cells.

Compared with the results of the Cu-PCM chips, stress-related interconnect failure is a likely cause of the observed functionality loss. The combination of high temperature and mechanical stress may lead to metal line cracking, and Al interconnect (on Ringo and Timepix) is likely more vulnerable than Cu interconnect.

VI. CONCLUSION

We have concluded that CIGS thin-film solar cells can be integrated on CMOS microchips. CMOS functionality can be maintained with both Cu and Al interconnect, as shown on chips from the 0.13-, 0.18-, and 0.25-μm technology generations. In view of mechanical stress, CIGS solar cells are preferably integrated on the chip's backside. If integrated on the front side, the process temperature should be kept around or below 400 °C. At the present state of CIGS technology, this implies a loss in solar cell efficiency.

In case of strong topography of more than a few hundred nanometers, the CMOS IC should be planarized. It must be covered by a diffusion barrier and possibly an adhesion layer, followed by the conventional PV process flow. The single-chip integration scheme shown in this work is suitable for wafer-level processing.

Integrated PV energy scavenging, compared with existing miniaturized scavenging solutions, offers high power, low manufacturing cost, and a broad application range (as light is commonly available). It further offers the advantages of a mature technology.

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