Gate Oxide Reliability and Deuterated CMOS Processing

A.J. Hof, A.Y. Kovalgin, J. Schmitz
MESA+ Research Institute, University of Twente, Enschede, The Netherlands
Tel: +31 53 489 2644; Fax: +31 53 489 1034
A.J.Hof@utwente.nl; A.Y.Kovalgin@utwente.nl; J.Schmitz@utwente.nl

R. van Schaijk, W.M. Baks
Philips Research Leuven, Kapeldreef 75, B-3001 Leuven, Belgium
Rob.van.Schaijk@philips.com; Wilko.Baks@philips.com

1. Introduction

In recent literature [1-7], a controversy has arisen over the question whether deuterium improves the stability of the MOS gate dielectric. It appears as if this controversy finds its origin in the different stages (e.g. oxidation or post metal anneal) deuterium is introduced in the CMOS process. This paper investigates this in detail.
The obtained results show that the hot carrier degradation only benefits from an isotope effect when deuterium is introduced in the post metal anneal. At the same time, charge to breakdown for high quality oxides does not benefit from an isotope effect, regardless the processing stage deuterium is introduced, or the used gate oxide thickness. This is verified on two different sets of wafers fabricated in two different laboratories.

2. Experimental

Two different sets of wafers have been fabricated in two independent facilities. The first set of wafers, fabricated in a university laboratory, consists of 100 mm wafers containing simple MOS capacitors with poly silicon gates. The gate oxide (6 to 9 nm) was grown using an ultra-diluted (partial pressure is 0.7 kPa) H_2O or D_2O ambient at 950 ˚C. The forming gas anneal was performed in a deuterium containing ambient for D_2O grown gate oxides and in a hydrogen containing ambient for H_2O grown gate oxides.
The second set, fabricated in an industrial laboratory, consists of 200 mm wafers containing various test structures, including MOS transistors and MOS capacitors with a drain edge. These devices were fabricated using a 0.18 µm technology.
Gate oxide growth was done in either, an O_2 ambient at 900 ˚C, an ultra-diluted H_2/O_2 ambient at 850 ˚C or an ultra-diluted D_2/O_2 ambient at 850 ˚C. The gate oxide thickness is 7 nm for all wafers in the set. A post oxidation anneal waseither not done, done in a N_2 ambient at 900 ˚C for 30 min or done in a D_2 ambient at 900 ˚C for 30 min. The process was completed after the first metal layer with a forming gas anneal in either a H_2/N_2 ambient or a D_2/N_2 ambient.
Charge to breakdown measurements were performed with a stress current of -100 mA/cm^2 on 121 devices (area is 10x10 µm^2) per wafer for the university set and at 20 devices (area is 50x200 µm^2) per wafer for the industrial set.
On the industrial set, hot carrier degradation was performed at transistors with a gate length of 0.25 µm and a gate width of 10 µm. During stressing, the source and substrate contacts were grounded, the drain voltage was set at 4.5 V and the gate voltage was set at 2.1 V. This corresponds to peak substrate current conditions. Linear input characteristics were measured for a drain-to-source voltage of 0.1 V and threshold voltage and maximum transconductance were extracted.

3. Results and discussion

Measurements on the MOS capacitors of the university set indicate that the Q_{bd} characteristics of the H_2O and D_2O devices are similar (figure 1). A small precaution has to be taken though, since the oxide thickness for the two different precursors do not exactly match, as indicated in the legend of figure 1.
To avoid this problem of thickness mismatch, the Weibull slope and modal (or 63%) Q_{bd} value are extracted from the data in figure 1 using a maximum likelihood estimation (figure 2). The graphs for the Weibull slope overlap, while the difference in the modal Q_{bd} value is small, in favour of the H_2O devices. This is in contrast with the results found in [8] which show a difference in Q_{bd} of at least a factor 2 in favour of D_2O grown oxide.
The above results are verified on the industrial set of wafers (figure 3, 4 and 5). Figure 3 shows that the Q_{bd} for the H_2/O_2 and D_2/O_2 grown oxides overlap, while there is a factor 2 difference in Q_{bd} between the dry oxide and the wet oxides, in favour of the wet oxides. Figures 4 and 5 show that later incorporation of the deuterium also has no effect on the Q_{bd}. Concluding it can be stated that (1) there is a distinct difference in Q_{bd} between the dry oxide and the wet oxides, but no difference between the wet oxides, (2) There is no difference for different post oxidation anneals, even more, the anneal does not have an effect at all, and (3) there is no difference between the forming gas anneals.
To verify that the deuterium is at least ‘electrically active’ at the Si-SiO_2 interface, hot carrier measurements were performed on the university set. The relative change in transconductance is shown in figure 6. The hot carrier degradation of the threshold voltage shows a similar trend, namely, (1) the hot carrier degradation *rate* is not affected by the oxidation, but only by the post metal anneal (2) A post metal anneal in D_2/N_2 increases the stress time needed to create the same degree of degradation with a factor 3.

4. Discussion

The hot carrier measurements confirm that deuterium incorporation during the post metal anneal improves the resistance to hot carrier stress as already proven in literature [8]. This can be explained by a difference in vibration frequency for the bending modes of the Si-H and Si-D bond, as is already done in [9].

However, the hot carrier measurements do not confirm the results obtained by Mitani [4], which indicated that an earlier incorporation of deuterium during the gate oxide growth can also increase the resistance to hot carrier stressing. At the same time the Q_{bd} measurements do not show an influence of the deuterium at all, irrespective of the processing step introduced. This is confirmed on two wafer sets fabricated in two independent laboratories. The idea arises that the deuterium incorporated during early processing steps desorbs and disappears during following high temperature processing, thus eliminating a possible positive effect of the incorporated deuterium.

The improved bulk oxide quality reported in literature [1-5] cannot be confirmed with the results presented in this paper.

The results in this work are obtained for an ultra-diluted ambient to allow for a reasonable oxidation time. This directly improves the gate oxide quality. The reports in literature do not mention the use of an ultra-diluted ambient. This suggests that a high quality grown oxide does not benefit from a deuterium isotope effect.

5. Conclusions

To benefit from a deuterium isotope effect for hot carrier degradation, the deuterium has to be incorporated at the end of the process, to avoid desorption of the deuterium during high temperature processing steps.

The bulk oxide quality is not improved due to a deuterium isotope effect when comparing high quality grown gate oxides.

Acknowledgement

Philips Semiconductors supplied part of the test devices and financially supports this work.

References

[1] H. Kim and H. Hwang, *Applied Physics Letters*, Volume 74, pages 709-710, 1999.

[2] H. Kim and H. Hwang, *Japanese Journal of Applied Physics*, Volume 38, pages L99-L101, 1999.

[3] H. Kwon and H. Hwang, *Proceedings of the 29th ESSDERC*, pages 416-419, 1999.

[4] Y. Mitani et al., *IEDM Technical Digest*, pages 343-342, 2000.

[5] Y. Mitani, *IEEE Transactions on Electron Devices*, Volume 49, pages 1192-1197, 2002.

[6] J. Wu et al., *Proceedings of the 38th IRPS*, pages 27-32, 2000.

[7] D. Esseni et al., *IEDM Technical Digest*, pages 339-342, 2000.

[8] J. W. Lyding et al., *Applied Physics Letters*, Volume 68, pages 2526-2528, 1996.

[9] C.G. Van de Walle and W.B. Jackson, *Applied Physics Letters*, Volume 69, page 2441, 1996.

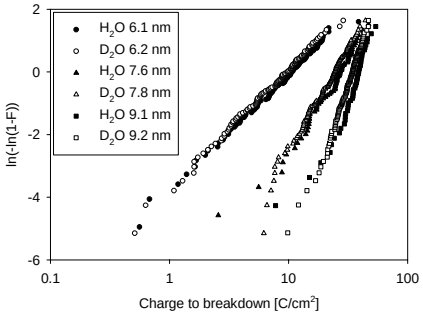

Figure 1: Charge to breakdown characteristics for H_2O and D_2O grown oxides with varying thickness.

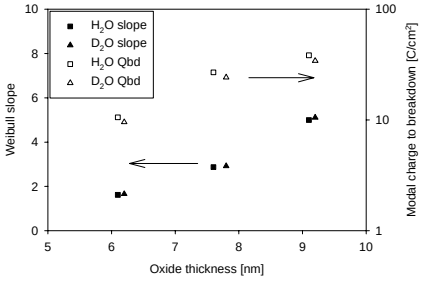

Figure 2: Weibull slope and modal Q_{bd} value extracted from the data in figure 1 as a function of oxide thickness.

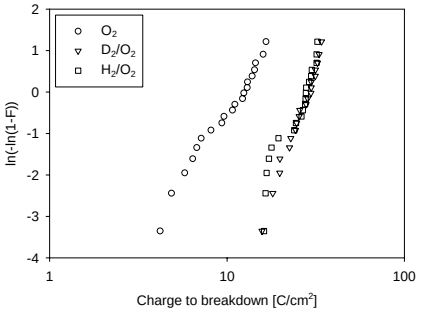

Figure 3: Charge to breakdown characteristics for gate oxides grown in either an O_2, H_2/O_2 or D_2/O_2 ambient. No post oxidation anneal was performed. Post metal anneal was performed in a D_2/N_2 ambient.

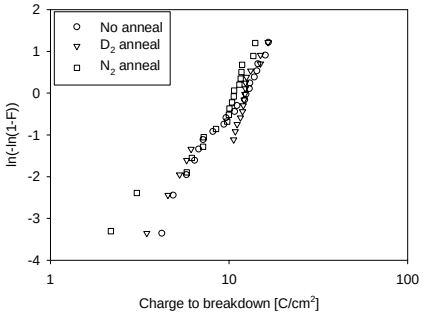

Figure 4: Charge to breakdown characteristics for gate oxides which received either no post oxidation anneal, or a post oxidation anneal in a N_2 or D_2 ambient. The gate oxide is grown in an O_2 ambient. Post metal anneal was performed in a D_2/N_2 ambient.

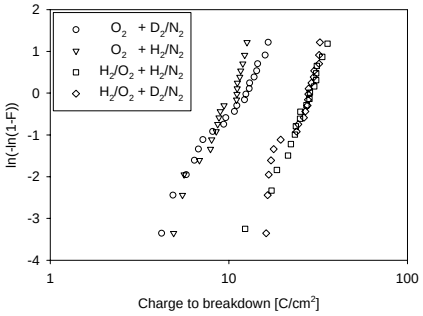

Figure 5: Charge to breakdown characteristics for gate oxides which received a post metal anneal in either a H_2/N_2 or a D_2/N_2 ambient. The gate oxide is grown in either an O_2 or a H_2/O_2 ambient. No post oxidation anneal was performed.

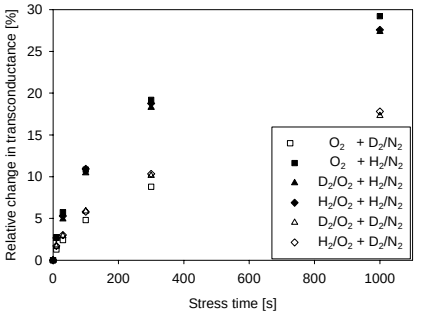

Figure 6: Relative change in maximum transconductance as a function of hot carrier stress time for devices with a gate oxide grown in either an O_2, a H_2/O_2, or a D_2/O_2 ambient and a post metal anneal in either H_2/N_2 or D_2/N_2.