Study of pocket implant parameters for 0.18 μm CMOS

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Abstract

PMOS and NMOS transistors for the 0.18 μm CMOS generation with pocket punch-through stoppers are presented. A detailed study of the dose and angle of the pocket implants is presented, showing that these implant conditions do not affect the long-channel S and V_T, nor the substrate current. A clear optimum is found when threshold voltage rolloff and subthreshold swing are evaluated, leading to the best performance in terms of I_{on}/I_{off} ratio.

1 Introduction

For high-performance logic in the 0.18 μm CMOS generation, the optimisation of the channel profile and the shallow source/drain extensions is a complex issue. The need for high saturation currents and low off-current calls for a low subthreshold swing and high channel mobility, while suppression of short channel effects requires the use of a high channel doping. A conventional channel doping profile can no longer fulfill the requirements of low V_T and good short channel behaviour. Therefore various alternative schemes are under investigation, such as a super steep retrograde well [1]. Self-aligned pockets [2] implanted around the source and drain junctions can also improve the short channel effects while maintaining a low subthreshold swing and low threshold voltage. The main advantages of pocket implants over a super steep retrograde well are, that they are implanted later in the process flow and thus endure less thermal budget (particularly the gate oxide growth); and that they do not influence the long-channel parameters such as threshold voltage, K-factor and subthreshold swing.

The effect of the implant parameters of the pocket implant has so far not been discussed in great detail in the literature. In this paper, we show that the optimisation of this implant in terms of dose and tilt angle is not straightforward. The effect of pocket implants on V_T, subthreshold swing, substrate current, and I_{on}/I_{off} ratio is discussed. Experiments were performed on a 0.18 μm CMOS process which was optimised for low off-current (< 10 pA/μm).
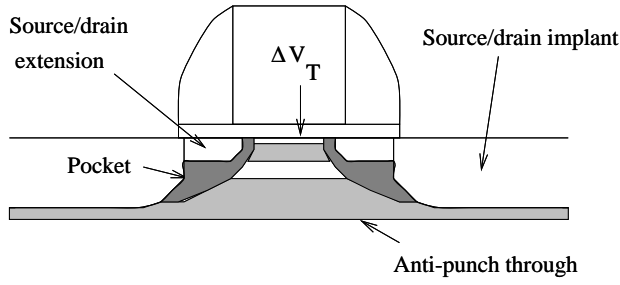
Implant	NMOS	PMOS
Pocket	5E12 B 15 keV 7/25/45°tilt	0/5/8E12 P 50 keV 25°tilt
S/D extensions	3E14 As 15 keV	3E14 B 1 keV

Figure 1: Schematic layout of the transistors, and implant parameters.

2 Results

NMOS and PMOS transistors were fabricated in a 0.18 μm (gate length) process flow featuring advanced LOCOS and electron beam lithography; the process is described in [3]. The device architecture is sketched in Figure 1, together with a table of the implant conditions for the pocket implants and the shallow source and drain extension implants. The gate length was measured after polysilicon etching, using a Hitachi 8820 Scanning Electron Microscope. Subthreshold and saturation characteristics of the 0.18 μm NMOS and PMOS transistor are shown in figure 2.

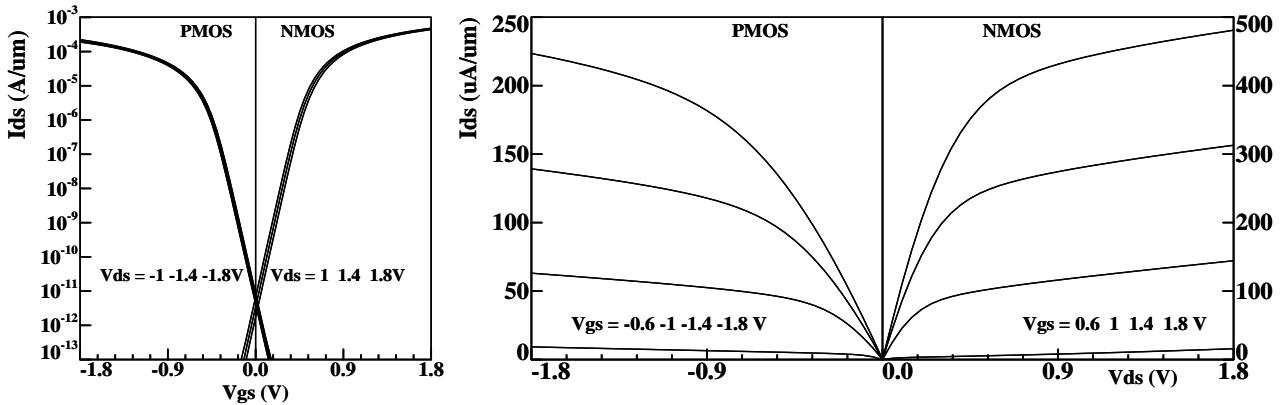Figure 2: subthreshold and saturation characteristics of 0.18 μm devices.

Shallow junctions for the source and drain were formed with As^+ and B^+ yielding effective channel lengths of 130-140 nm. The boron pocket implant energy was determined with simulations to have a peak concentration at the source and drain extension junctions, to minimise the source and drain depletion widths. The impact of tilt angle variation is shown in figure 3 and 4. The 7° tilt angle results in poor short channel behaviour, while the 45° tilt angle gives a high subthreshold swing for the short channel devices (because the pocket implants meet under the gate). As a result the balance between I_{off} and I_{on} becomes less favourable. The intermediate angle of 25° resulted in good short channel behaviour both in terms of V_T-rolloff and S-rollup at the pocket implant energy of 15 keV, resulting in the best I_{on}/I_{off} ratio at the nominal device. As shown in figure 4, the pocket angle has no effect on the I_B^{max}/I_D ratio. This indicates that the pocket implant does not influence the hot carrier degradation. The gate oxide thickness of the NMOS transistors is 4.5 nm.
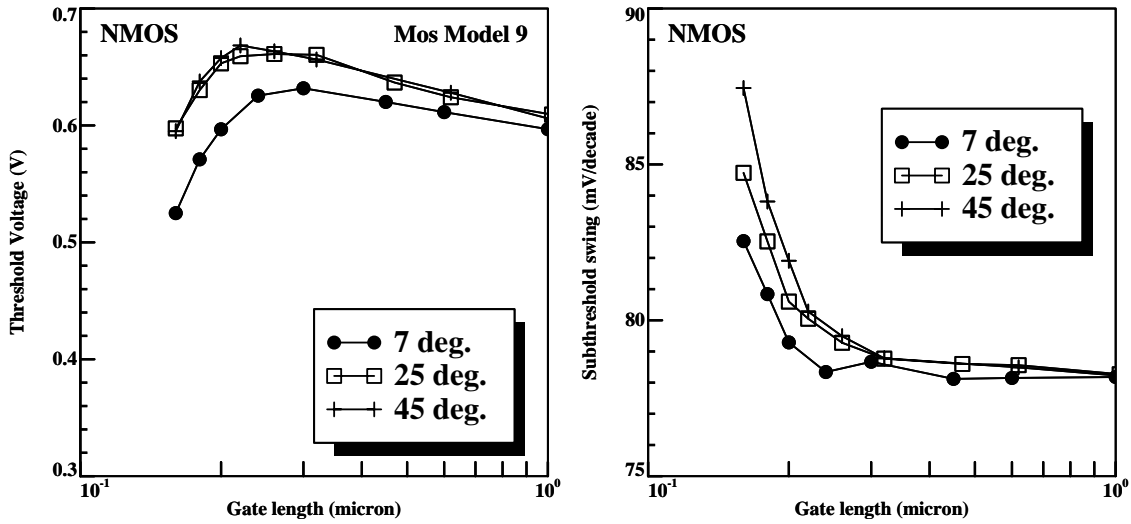
Figure 3: threshold voltage rolloff and subthreshold swing rollup of NMOS devices as a function of the pocket tilt angle.
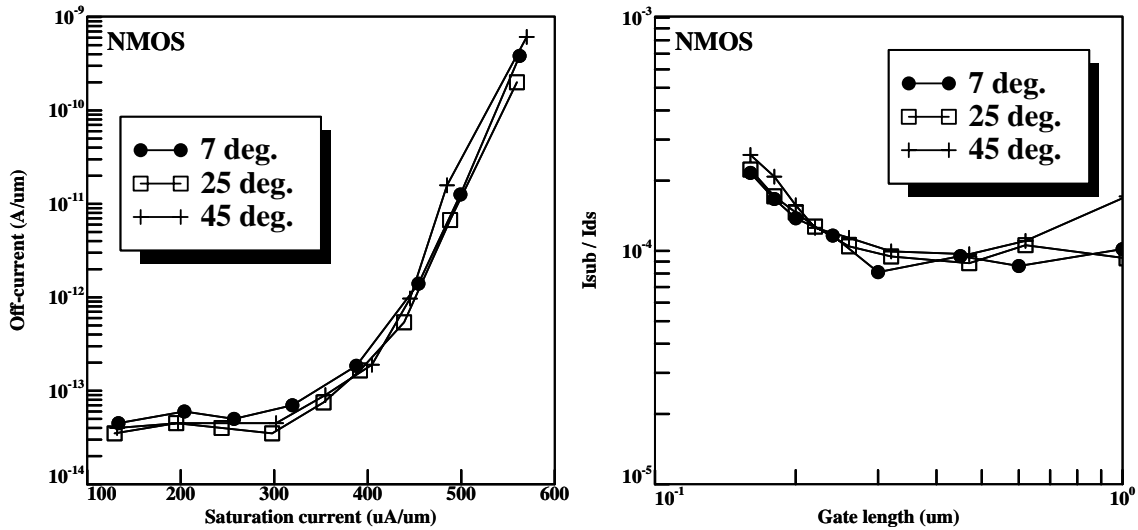

Figure 4: I_{off} versus I_{on} and substrate current of NMOS devices as a function of pocket tilt.

PMOS transistors with phosphorus implanted pockets show similar behaviour. 0.18 μm transistors with $\Delta L= 40$ nm (determined with Mos Model 9 [4]) were fabricated with a thinner gate oxide (4.0 nm) resulting in a saturation current of 225 μA/μm and off-current of 8.5 pA/μm. The pocket implant dose was varied as depicted in figure 5 and 6. The PMOS transistors with the highest dose (8E12) have the best Ion/Ioff ratio because of the strongest suppression of short channel effects. However, these transistors show a reverse short channel effect around the nominal device, and the high peak concentration $> 10^{18}$ cm^{-3} in the channel region results in a large junction capacitance. Therefore the lower dose of 5E12 was considered optimal at the implant energy of 50 keV. Like with the NMOS, the pocket implants do not affect the long-channel threshold voltage. The $I_B{}^{max}/I_D$ ratio is not influenced by the pocket dose as shown in figure 6.
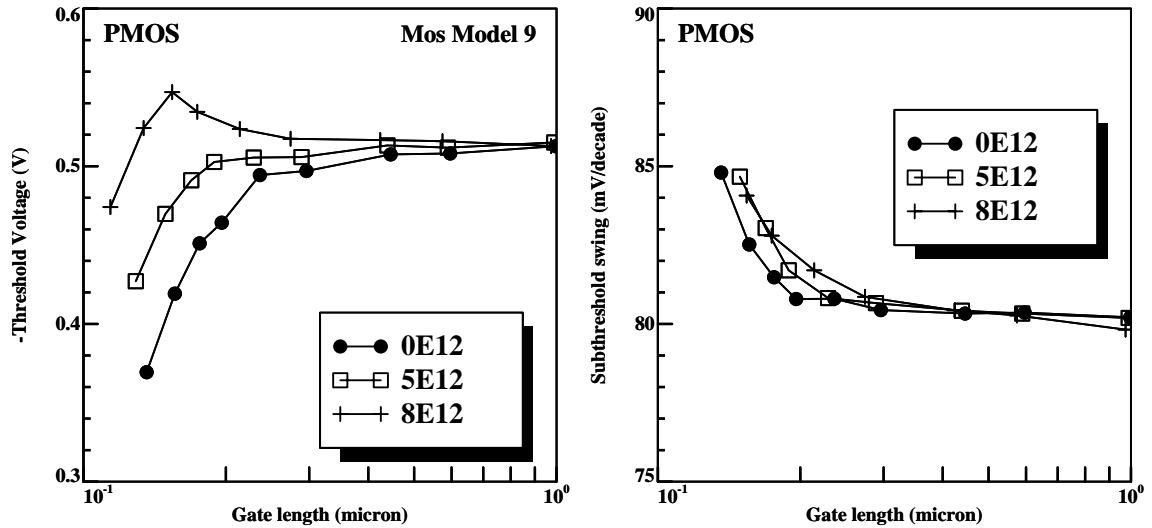
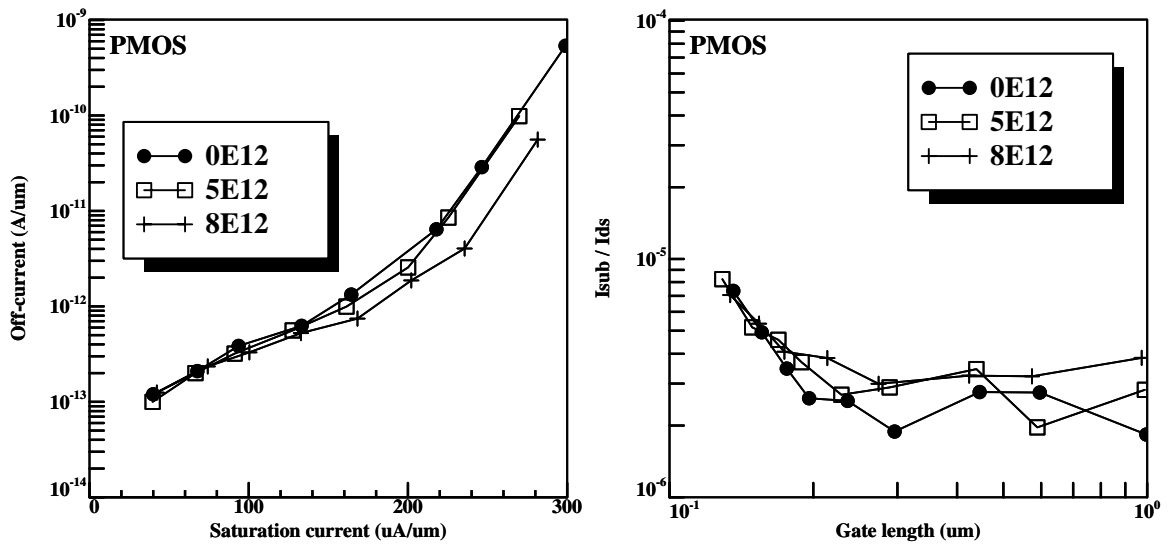Figure 5: V_T-rolloff and S rollup of PMOS devices as a function of the pocket dose.

Figure 6: I_{off} versus I_{on} and substrate current of PMOS devices as a function of pocket dose.

3 Summary

Pocket implanted 0.18 μm gate length NMOS and PMOS transistors with high performance at low off-current have been fabricated. The optimised pocket tilt angle was shown to be 25° with a dosage around 5E12, where a balance is found between V_T-rolloff and S-rollup. This results in a favourable I_{on}/I_{off} ratio: on-currents of 480 μA/μm (NMOS) and 225 μA/μm (PMOS) are achieved with off-currents < 10 pA/μm.

4 References

1. M. Rodder et al., IEDM'95 p. 111.   **2**. T. Hori et al., IEDM'94 Tech. Dig., p. 75.

3. J. Schmitz et al., Essderc'96 proc., p. 329.   **4**. R. Velghe et al., IEDM'93 Tech. Dig. p.485.