Test Structure Design Considerations for RF-CV Measurements on Leaky Dielectrics

J. Schmitz*, F. N. Cubaynes†, R. J. Havens‡, R. de Kort‡, A. J. Scholten‡ and L. F. Tiemeijer‡
*Philips Research Leuven; Presently at the University of Twente, The Netherlands. E-mail: J.Schmitz@utwente.nl
†Philips Research Leuven, Kapeldreef 75, 3001 Leuven, Belgium
‡Philips Research Laboratories, Prof. Holstlaan 4, 5656AA Eindhoven, The Netherlands

Abstract—We present a MOS Capacitance-Voltage measurement methodology that, contrary to present methods, is highly robust against gate leakage current densities up to 1000 A/cm^2. The methodology features specially designed RF test structures and RF measurement frequencies. It allows MOS parameter extraction in the full range of accumulation, depletion and inversion.

I. Introduction

As CMOS device dimensions are scaled below 100 nm, the concurrent gate dielectric thinning leads to progressively higher gate leakage currents. Tunnel current densities around 100 A/cm^2 are foreseen for the near future in some CMOS logic applications [1]. Although this may be acceptable from a functional point of view, such leakage currents complicate fundamental MOS characterization techniques like charge pumping [2], time-dependent dielectric breakdown tests [3] and capacitance-voltage (C-V) measurements [4-8].

Gate leakage affects the measurement of the capacitance-voltage characteristic as well as its interpretation. This can be understood conceptually by considering a simple three-element equivalent circuit for the leaky MOS capacitor as sketched in Fig. 1. The capacitance C is connected in parallel to a (strongly

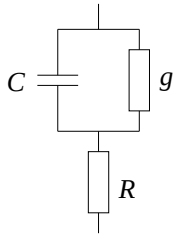

Fig. 1. Three-element equivalent circuit approximation of a leaky MOS capacitor.

bias-dependent) differential conductance $g \equiv \mathrm{d}I/\mathrm{d}V$ arising from gate current. An external resistance R, originating e.g. from gate resistance, is also inevitable. The impedance Z of this three-element circuit and the related quality factor Q can be expressed as

$$Z = \frac{1}{j\omega C + g} + R \tag{1}$$

$$Q \equiv -\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} = \frac{\omega C}{g + R(\omega^2 C^2 + g^2)} \tag{2}$$

The quality factor determines to a large extent if a capacitance measurement at angular frequency $\omega = 2\pi f$ will yield an accurate value. When $Q > 10$, capacitance measurement and analysis is straightforward. For $1 < Q < 10$, careful analysis (with quantification of the parasitic contributors g and R) can still yield a good value of the capacitance, provided that a good model is used; the three-element approximation of Fig. 1, used here for a qualitative illustration, has its limitations [6,8]. For $Q < 1$, the instrument precision is spent on accurate determination of (one of) the resistive components, and the measurement of the imaginary part becomes inaccurate.

The quality factor rises linearly with frequency in the low-frequency range, reaches a maximum Q_{opt} at frequency f_{opt}, and then drops linearly with frequency as sketched in Fig. 2. Taking $\delta Q/\delta\omega = 0$ in equation (2)

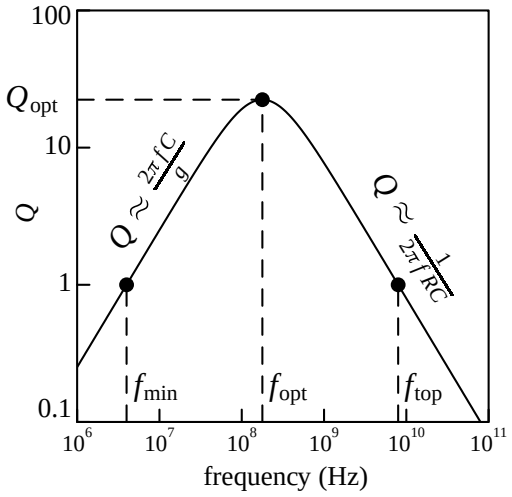

Fig. 2. Frequency dependence of the quality factor Q of the three-element circuit sketched in Fig. 1. For this example, $C = 2$ pF, $g = 50\times10^{-6}\ \Omega^{-1}$, and $R = 10\ \Omega$.

yields the following expressions for Q_{opt} and f_{opt}:

$$f_{\mathrm{opt}} = \frac{1}{2\pi RC}\sqrt{gR(1+gR)} \tag{3}$$

$$Q_{\rm opt} = \frac{1}{2\sqrt{gR(1+gR)}} \tag{4}$$

As long as the measurement instrument limitations (precision, frequency range) do not play a role, a measurement at $f_{\rm opt}$ will lead to the most accurate value for C. To obtain $Q_{\rm opt} \gg 1$, it follows directly from (4) that R should satisfy

$$gR \ll \frac{\sqrt{2}-1}{2} \approx 0.2 \tag{5}$$

This equation shows that the higher the gate leakage (and hence g), the lower the external resistance R must be. This is an important design criterion for RF-CV test structures, as further discussed in the next Section.

When $Q_{\rm opt} > 1$, the quality factor Q is above unity in a frequency range around $f_{\rm opt}$. This frequency range is defined by the minimum measurement frequency $f_{\rm min}$ and the maximum frequency $f_{\rm top}$, as indicated in Fig. 2. Expressions for $f_{\rm min}$ and $f_{\rm top}$ can be readily derived from solving $Q = 1$ in (2):

$$f_{\rm min} = \frac{1-\sqrt{1-4gR(1+gR)}}{4\pi RC} \approx \frac{g}{2\pi C} \tag{6}$$

$$f_{\rm top} = \frac{1+\sqrt{1-4gR(1+gR)}}{4\pi RC} \approx \frac{1}{2\pi RC} \tag{7}$$

The minimum frequency is dictated by the magnitude of the gate leakage g. Typical MOS capacitors as studied in present research and development work suffer from gate leakage to such an extent that measurements in the normal LCR range of 1 kHz – 1 MHz are inadequate. For example, a 10×10 μm^2 MOS capacitor with 10 A/cm^2 gate leakage typically has $C = 2$ pF, $g \approx 50\times10^{-6}\ \Omega^{-1}$, and $R = 10$–$100\ \Omega$ leading to $f_{\rm min} = 4$ MHz. As Q will rise linearly with f above $f_{\rm min}$, a good C-V measurement on such a device is best conducted above 10 MHz.

The highest measurement frequency $f_{\rm top}$ is constrained by external resistance. When excessive gate leakage forces the application of RF measurement frequencies (following equation (6)), the external resistance must therefore be reduced to a minimum to still allow a good measurement of capacitance.

II. Test structure design

Conditions (5)-(7) dictate the layout of a C-V test structure to a great extent. There is design freedom in the choice of device area and the external resistance (influenced e.g. by geometric choices and by impurity distributions in the substrate). While specific capacitance and specific conductance are fixed for a given dielectric (and DC bias), the external resistance in many cases scales with the square root of area (see e.g. [11],[12]). Therefore, a smaller area device will yield an improved $Q_{\rm opt}$ as the product gR decreases. For any reasonable dielectric (with a leakage current density below 1 kA/cm^2), the condition $gR \ll 0.2$ can be met by a careful design of the test structure: abundant, nearby well contacts and a small gate area. (For a sufficiently high total capacitance, several devices with separate well contacts can be connected in parallel, as in [9].) Figure 3 shows a layout used for RF transistors that fulfills these requirements. Once a design

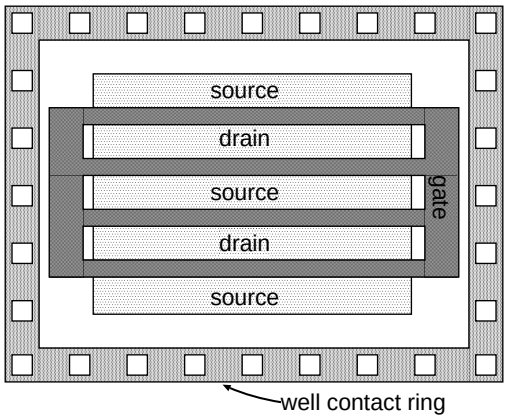

Fig. 3. Top view of the (conceptual) layout of an RF transistor, suitable for RF-CV measurements. Several parallel gates run horizontally across a rectangular active area. The gates are connected at both ends (on field isolation) to metal-1, to the Port-1 bond pad of a ground-signal-ground test structure. The sources are contacted to ground; the drains to Port-2. The entire structure is surrounded by a well connection ring ('guard ring'), connected to ground.

has been created in line with the above considerations, estimates for $f_{\rm min}$ and $Q_{\rm opt}$ can be made, from which it can be readily determined if the test structure is suitable for C-V measurement or not.

III. Device fabrication and characterization

The experimental study of C-V measurements at gigahertz frequencies (RF-CV measurements) is carried out using transistors designed for two-port RF characterization in ground-signal-ground configuration. They consist of many gates connected in parallel, with a layout resulting in very low gate resistance and low well resistance, as described in the previous section. Sub-micron channel lengths are used to suppress channel resistance. The gate is connected to Port 1, drain connected to Port 2. The gate is biased, all other terminals are grounded.

Devices were fabricated in a standard 6-metal 0.12 μm CMOS flow, and in a single-metal CMOS research process. S-parameter measurements in the range 0.1–48 GHz were carried out on-wafer using an HP 8510C network analyzer. The measurements were accompanied by SOLT calibration and open-short de-embedding [10].

IV. Validation of RF-CV measurements

Capacitance-voltage measurements between 0.5 and 10 GHz are shown in Fig. 4. Here, $C_{\rm gg} \equiv {\rm Im}(Y_{11})/\omega$, which is only a good approximation of the MOS capacitance C when the external resistance R is negligible. At the lowest frequencies, the shape of the curve is as expected, with the accumulation behavior of an ultra-thin dielectric and

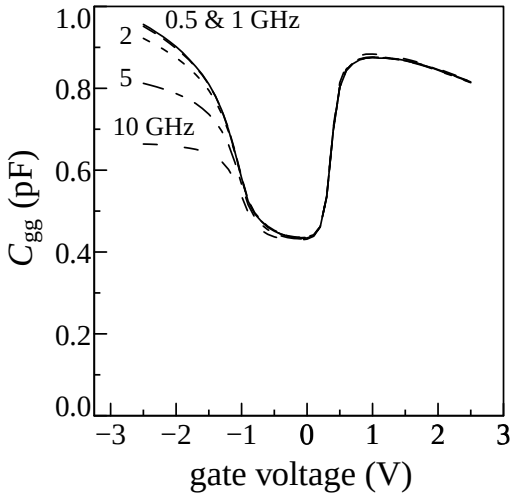

Fig. 4. Left: capacitance-voltage curve of a W/L = 384 μm/0.18 μm NMOS RF transistor as measured at various frequencies, after de-embedding.

inversion capacitance decreasing due to gate depletion. The depletion region around $V_g = 0$ V shows only a moderate decrease in capacitance because this is a sub-micron channel device with significant gate-drain overlap capacitance.

At frequencies above 1 GHz, we observe a drop in the capacitance at accumulation bias. It is accompanied by a downward bend of the real part of Y_{11}: see Fig. 5. This

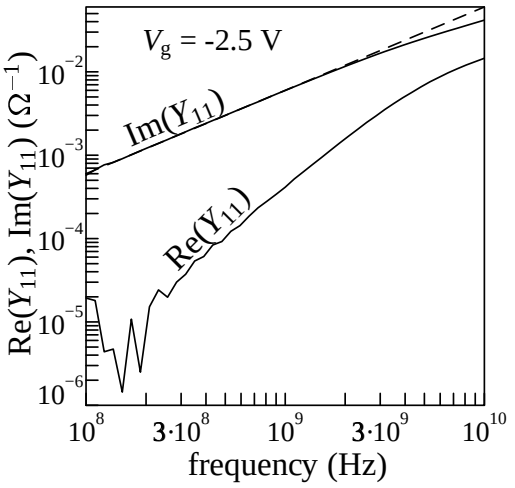

Fig. 5. Real and imaginary parts of Y_{11} as a function of frequency at V_g = -2.5 V, for the measurements shown in Figure 4. The dashed line shows a straight-line extrapolation (corresponding to a capacitor without series resistance), to guide the eye.

is not due to a drop in the MOS capacitance, but rather the signature of a significant external series resistance. The origin is the well resistance R_{well}, which results in a limited response time of bulk holes; see Fig. 6. In this figure, we have explicitly separated the overlap regions, with capacitance C_{ov} and conductance g_{ov}, from the

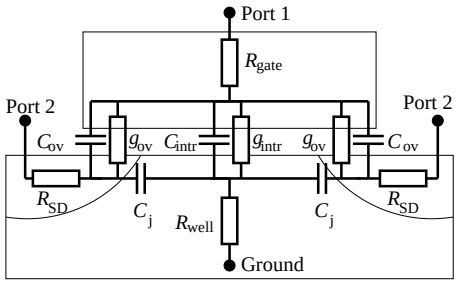

Fig. 6. Cross section of a capacitor (or transistor), with an approximated equivalent circuit in accumulation. All components in this diagram are bias dependent except R_{gate}, R_{SD} and R_{well}.

intrinsic or "channel" region with capacitance C_{intr} and conductance g_{intr}. In accumulation and depletion, charging and discharging of C_{intr} requires holes to move from the "channel" region to the ground connection through R_{well}. This transport is limited by the characteristic delay time $\tau = R_{well}C_{intr}$, which implies (in line with (7)) that the measurement frequency f is restricted to

$$f \ll \frac{1}{2\pi R_{well} C_{intr}} \tag{8}$$

For the transistor under study, $\tau \approx 20$ ps. As a result the depletion and accumulation capacitances of C_{intr} are attenuated at frequencies above 1 GHz.

The observed gate capacitance does not drop entirely to zero due to this series resistance effect, because of the overlap capacitance; and also, because the small signal can pass to Port 2 via C_{intr} and the junction capacitance C_j. In other words, the holes required to charge and discharge C_{intr} can also be supplied from the junction capacitance. Altogether, it is far from trivial to determine R_{well} directly from these measurements because the small signal applied to the gate can follow several paths to ground. Instead, since the C-V measurements at $\leq$ 1 GHz are unaffected by τ, C_{intr} is best derived from those measurements.

For this purpose we measured the Y-parameters of two devices with equal design except for the gate lengths, being 130 and 180 nm. From the difference of the obtained C_{gg} curves, we can establish the C_{intr} of a 50 nm channel segment. The capacitance of this segment is shown in Fig. 7. A C-V model can now be fitted to these data to obtain the required MOS parameters. As an example we fitted MOS Model 11 [13] over the full curve, also shown in the figure. Fit values were: a flat band voltage of -1.07 V, 1.9 nm oxide thickness, an effective gate doping $N_G = 2.6\times10^{20}$ cm^{-3}, and a substrate doping of 1.7×10^{18} cm^{-3} (using no other fit parameters). These values are well in line with the expected values for this 0.12 μm CMOS process.

V. RF-CV and gate leakage

The RF-CV measurement method can cope with a large gate leakage current. We fabricated RF transistors

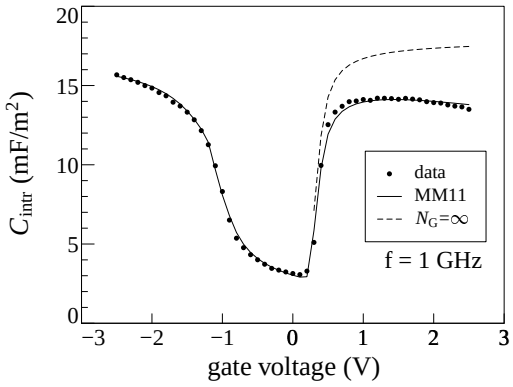

Fig. 7. Area-normalized capacitance of a 50 nm wide channel segment as computed from the difference of a 130 nm and a 180 nm gate length RF transistor. A fit of MOS Model 11 (MM11) to the data is also shown (see text). The dashed line symbolizes the (modeled) inversion capacitance in case of infinitely high gate doping.

with high-leakage dielectrics in a research process flow (based on 0.18 μm CMOS) using a different design of RF structures. These devices unfortunately have a much higher $R_{\rm well}C_{\rm intr}$ product (by design), preventing the correct measurement of accumulation and depletion capacitance in the channel. In inversion however, $R_{\rm well}$ does not play a role while the gate leakage current is at its highest. The external resistance in inversion (being the sum of gate, channel, and source/drain resistances) is well below 1 Ω, which adequately solves the measurement problems discussed in e.g. [14].

Fig. 8 shows the measured inversion capacitance. $C_{\rm intr}$

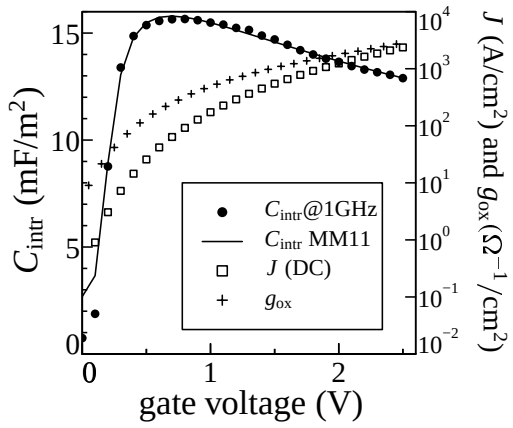

Fig. 8. Inversion capacitance and gate leakage current density of a high-leakage dielectric. The inversion capacitance is correctly measured even when the gate current density exceeds 1 kA/cm^2, as confirmed by the excellent fit with MOS Model 11.

was obtained from the capacitance difference between a 1 μm and a 0.2 μm gate length device. (For this to be meaningful, the threshold voltage difference between these devices must be limited.) No capacitance "roll-off" is observed, as a direct consequence of the GHz frequency. This can be seen from Fig. 9. The figure shows the

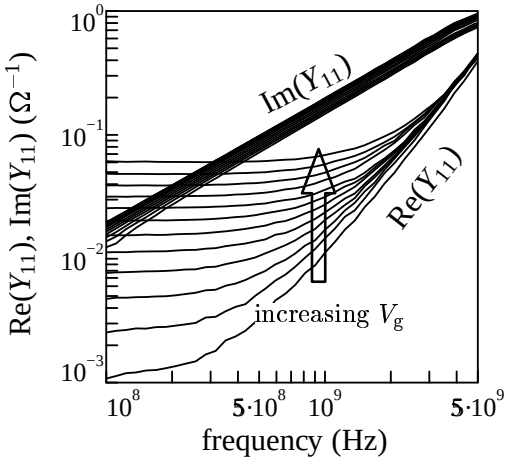

Fig. 9. Real and imaginary components of the input admittance of an NMOS capacitor in inversion. The device has 1872 μm^2 gate area. The gate bias was varied between 0.3 V and 2.5 V in steps of 200 mV. The imaginary parts almost overlap, but due to the exponential increase of gate leakage current with V_g, the real part of Y_{11} changes drastically.

imaginary and real parts of the input admittance (Y_{11}) and the quality factor of a 0.2 μm gate length device, as a function of frequency. The real part of Y_{11} is dominated by the oxide conductance $g_{\rm ox}$ at lower frequencies (horizontal part of the curve) and by the external (differential) resistance $R_{\rm ext}$ at higher frequencies (steeply rising curve). The external resistance is the sum of gate, channel, and drain resistances. As a result, when high gate leakage is present the capacitor quality factor is only larger than unity in a frequency band around 1 GHz, as illustrated by Fig. 10. Note the shape of the quality factor versus frequency, which matches very well the predicted shape when a simple three-element approximation is used.

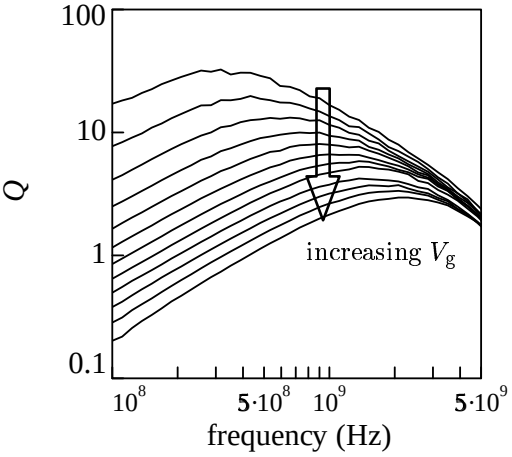

Fig. 10. Capacitor quality factor derived from the measurements in Figure 9.

To assess the validity of the obtained C-V curves for MOS parameter extraction, we fitted MOS Model 11 to

the data, with substrate doping, gate doping and oxide thickness as the only free parameters. The fit results are listed in Table I, for fits obtained on C-V curves taken

f GHz	t_{ox} nm	N_G $10^{20}/cm^3$
0.10	(1.24)	(0.80)
0.21	1.33	0.90
0.48	1.35	0.94
1.0	1.35	0.95
2.1	1.33	0.94
4.8	(1.42)	(1.15)

TABLE I

MOS Model 11 fit results for oxide thickness t_{ox} and gate doping concentration N_G, obtained from C_{intr}-V curves measured at various frequencies. Values in brackets are found with poor convergence of the fitting procedure, coinciding with low quality factors at the higher gate voltages.

at various frequencies. The obtained values for the fit parameters are well in line with the expectations for this process. The MOS Model 11 fit yields an oxide thickness and gate doping level independent of frequency in the range 0.2–2 GHz, while it fits poorly outside that region (due to a low quality factor).

VI. Conclusions

This paper presents the RF-CV methodology, which allows the measurement and analysis of capacitance-voltage curves even in the presence of gate leakage exceeding 1000 A/cm^2. On the basis of theoretical and experimental findings, design guidelines are formulated for RF capacitors. When these guidelines are followed, the appropriate Capacitance-Voltage characteristics are obtained around 1 GHz. These can be used for the extraction of MOS parameters such as (equivalent) oxide thickness, substrate doping concentration, and gate depletion. Since power and functionality requirements restrict the gate leakage in CMOS circuits to typically $\leq$ 1000 A/cm^2, the presented methodology is well suited for the characterization of any dielectric foreseen in future CMOS technologies.

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