A Fully Passive RF Front-end with 13 dB Gain Exploiting Implicit Capacitive Stacking in a Bottom-plate N-path Filter/Mixer

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***Abstract*—A low-power interferer-robust mixer-first receiver front-end that uses a novel capacitive stacking technique in a bottom-plate N-path filter/mixer is proposed. Capacitive stacking is achieved by reading out the voltage from the bottom-plate of N-path capacitors instead of their top-plate, which provides a 2x voltage gain after down-conversion. A step-up transformer is used to improve the out-of-band (OOB) linearity performance of small switches in the N-path mixer, thereby reducing the power consumption of switch drivers. This paper explains the concept of implicit capacitive stacking and analyzes its transfer characteristics. A prototype chip, fabricated in 22 nm FDSOI technology, achieves a voltage gain of 13 dB and OOB IIP3/IIP2 of +25/+66 dBm with 5 dB Noise figure while consuming only 600 μW of power at f_{LO}=1 GHz. Thanks to the transformer, the prototype can operate in the input frequency range of 0.6-1.2 GHz with more than 10 dB voltage gain and 5–9 dB Noise figure. Thus it opens up the possibility of low-power software defined radios.**

***Index Terms*—Passive mixer, N-path filter, CMOS, mixer-first receiver, bottom-plate mixing, capacitive stacking, high linearity, transformer, low power, RF front-end, interference-robust, IoT.**

I. Introduction

THE advent of Internet-of-Things (IoT) has been resulting in the surge of connected devices ($\geq$ 25 billion devices by 2021 [1]) and proliferation of wireless sensor nodes. Massive IoT applications lead to a crowded spectrum, making receivers susceptible to mutual interference. Hence along with cost and power consumption, interference robustness is becoming a major concern for the radios targeting these applications. For example, NB-IoT standard has an out-of-band blocking requirement of -15 dBm at 85 MHz offset [2], [3].

Interferer-robust CMOS RF front-ends report out-of-band (OOB) blocker 1dB compression point $\geq$ 0 dBm and OOB-IIP3 $\geq$ +25 dBm using techniques such as highly-linear LNTAs, passive-mixers, mixer-first RX, N-path filters and feedback cancellations [4]–[16]. LNTAs consume large power to achieve low noise figure and high linearity. Passive mixers and N-path filters employ power-hungry clock-generation circuitry and drivers to drive their large switches. Often, the reported power consumption of these high-performance front-ends are in the range of a few tens to hundred mW.

Low power CMOS receivers typically employ high-Q external filters (e.g., SAW, FBAR) or off-chip and on-chip LC resonant tanks to attenuate the blockers and improve their OOB selectivity [17]–[23]. Recently N-path filters and feedback cancellations [24], [25] are adopted to improve the RF filtering and enhance the linearity performance of the RX. With power consumption $\leq$ 5 mW, these RXs exhibit OOB IIP3 between -20 and 0 dBm. This is at least 20 dB worse than the high-performance interferer-robust receivers.

Our objective is to develop energy efficient interference robust radio techniques suitable for IoT applications and low power software defined radios. In [26], we presented a fully passive N-path filter/mixer architecture that achieves conversion gain and high OOB linearity simultaneously. Bottom-plate mixing is used for its attractive OOB linearity performance [14]. Two low-power techniques were introduced: (1) an implicit capacitive stacking technique which provides 6 dB voltage conversion gain "*for free*" without any active elements; and (2) a step-up transformer before the N-path filter to achieve high linearity at low power consumption. Exploiting these techniques, a fully-passive 1 GHz CMOS RF front-end achieving 13 dB gain and +25 dBm OOB-IIP3 at sub-mW power consumption is realized. Compared to [26], this paper explains the concept and circuit implementation in more depth, analyzes the transfer characteristics, and provides additional simulation and measurement results. Please note that the design specifications such as operating frequency and OOB linearity, are inspired by the NB-IoT standard [2]. However, the proposed work here is a proof-of-concept for the capacitive stacking technique rather than a complete receiver for any specific standard.

The rest of the paper is structured as follows: the concept of implicit capacitive stacking technique in bottom-plate N-path filter/mixer is discussed in Section II. The transfer function of the proposed technique and the linearity benefits due to transformer are presented in Section III. Section IV discusses the implementation details of the proposed fully-passive RF front-end and its measured performance are reported in Section V. Finally, the conclusions are summarized in Section VI.

II. Implicit capacitive stacking - Concept

In this section, we will briefly summarize the fundamentals of bottom-plate mixing and its limitations compared to top-plate mixing. Then we will introduce the concept of implicit capacitive stacking and discuss its principle of operation.

A. Bottom-plate mixing - Fundamentals

CMOS N-path filters [7], [8], [15] are commonly implemented with N passive mixers connected to the top-plate of

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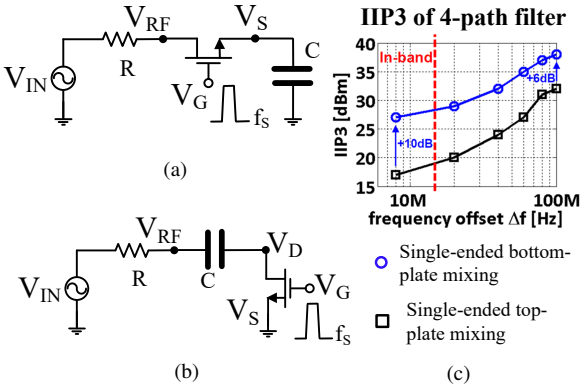


Fig. 1: Switched RC mixer (a) Top-plate mixing, (b) Bottom-plate mixing and, (c) Simulated IIP3 for 4-path singled-ended top-plate and bottom-plate mixing filters [14].

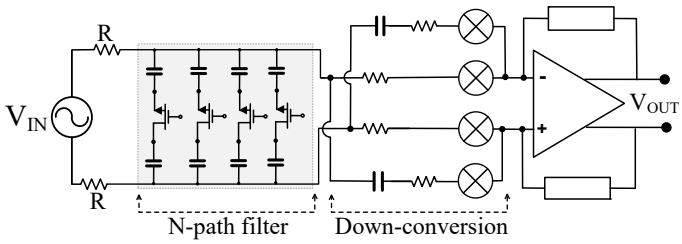


Fig. 2: Differential bottom-plate N-path filter followed by a cross-coupled switch-RC N-path down-conversion mixer [14].

the grounded capacitors on one end and the RF terminal on the other (Fig. 1a). The on-resistance of MOS mixer-switches is heavily modulated by the voltage at its drain and source terminals, i.e., the RF input and the down-converted baseband capacitor voltage. As shown in Fig. 1a, this modulation in switch resistance limits the achievable in-band linearity [14].

The bottom-plate mixing technique ties the RF node to the top-plate of the capacitor while the switch connects the bottom-plate of the capacitor to ground (see Fig. 1b) [14]. The V_S node of the switch is now always grounded and the V_D terminal is also pulled down to ground when the switch is on. Hence V_{GS} of the switch remains constant, thereby reducing the input induced variation in switch resistance. This results in 10 dB higher in-band linearity compared to top-plate mixing (see Fig. 1c) [14]. On the other hand, when the switch is open, the corresponding capacitor becomes floating as it is disconnected from the ground. This complicates the extraction of the baseband voltage from the capacitor. However, still N-path RF band-pass filtering can be realized at the RF nodes. A differential implementation of a bottom-plate N-path filter is shown in Fig. 2, in which the RF voltage from the top-plate of the N-path capacitors is down-converted using a cross-coupled switch-RC network [14].

B. Implicit Capacitive Stacking technique

In reference [14], the filtered RF voltage is sensed at the top-plate of the capacitor before down-conversion. Here we propose to sense the voltage from the bottom-plate of the capacitor instead. Fig. 3a and Fig. 3b compare the proposed idea with implementation in [14]. We will show how this

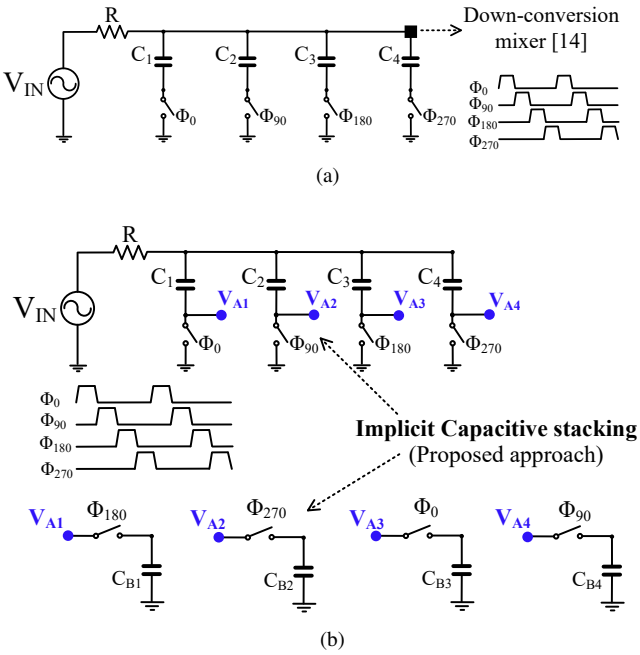


Fig. 3: Voltage read-out options in a bottom-plate 4-path filter (a) Read the top-plate voltage of the mixing capacitors [14] (b) Proposed approach - read the bottom-plate voltage of the mixing capacitors

simple modification results in 6 dB passive voltage gain at down-conversion.

Consider a 4-path single-ended bottom-plate N-path filter with resistor R and capacitors C_1-C_4 of capacitance C, as shown in Fig. 3b. The bottom-plate of these capacitors are connected to capacitors C_{B1}-C_{B4} of capacitance C_B through switches. Assume that the switches are ideal and have negligible resistance. The switches are turned on/off by 4-phase non-overlapping clocks ϕ_{0-270}, switching at a frequency f_{LO}. Suppose that the time constant RC is much larger than T_{on} of clock phases, ϕ_{0-270}, for "mixing region" operation [7]. After a large number of switching cycles, each capacitor stores the average value of the input signal it sees during its on-time.

For simplicity, consider that a sinusoidal signal with frequency f_{in} is applied at the input V_{in}. Let V_{RF} be the voltage at RF node to which the top plate of all the capacitors are connected and V_{C1}-V_{C4} be down-converted voltages stored in the capacitors C_1-C_4 repsectively. For $f_{in} = f_{LO}$, the resultant baseband voltage on each capacitor is a zero-IF signal. Due to 4-phase clocking, the capacitor voltages are related as follows: $V_{C1} = -V_{C3}$ and $V_{C2} = -V_{C4}$ (see Fig. 4). For negligible switch resistance, V_{RF} at any instant is equal to the voltage of the capacitor switched to ground at that particular instant. The voltage wave at V_{RF} can be constructed by time multiplexing the capacitor voltages, as shown Fig. 4. It should be noted that V_{RF} is the band-pass filtered RF output of the bottom-plate N-path filter in [14] with fundamental frequency of f_{in}.

Since the voltage V_{A1} at the bottom-plate of the capacitor C_1 is equal to $V_{RF}(t) - V_{C1}(t)$, its waveform is simply the waveform of V_{RF}, shifted down by DC voltage V_{C1} (see Fig.4). Similarly, voltage V_{A3} at the bottom-plate of C_3 is $V_{RF}(t) - V_{C3}(t)$ and its waveform is V_{RF} shifted up by V_{C3}, since $V_{C3} < 0$ here. Likewise, the voltage waveform at the

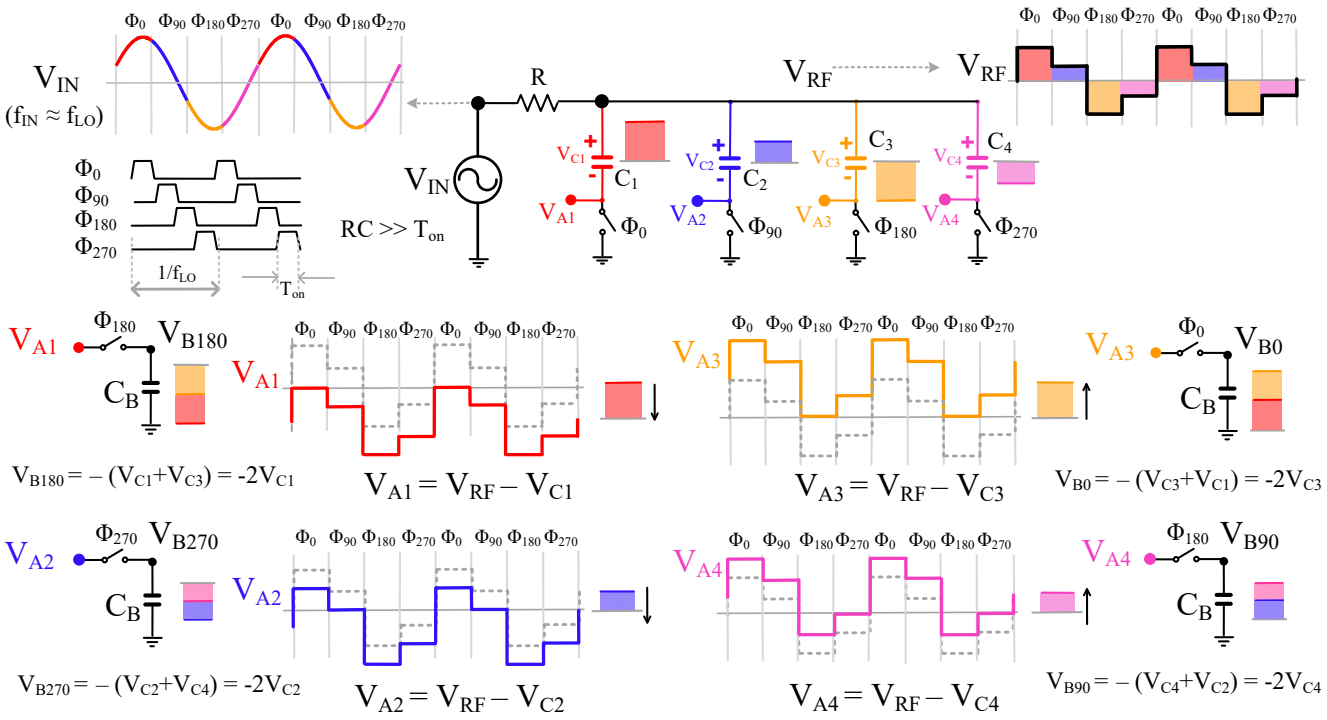


Fig. 4: Voltage waveforms in a 4-path single-ended bottom-plate filter with implicit capacitive stacking

bottom-plate of remaining capacitors can be obtained. Since V_{RF} has a fundamental frequency of f_{in}, so does V_{A1-4}.

Now we will examine the voltage waveform at node V_{A1} at different clock phases. We can see in Fig. 4 that during ϕ_{180}, capacitor C_3 is connected to ground ($V_{A3} = 0$), so voltage V_{RF} will be same as V_{C3}. This makes voltage V_{A1} equivalent to $V_{C3} - V_{C1}$. Since $V_{C3} = -V_{C1}$, we conclude that $V_{A1} = 2 \times V_{C3}$ during phase ϕ_{180}. We can read out this doubled voltage V_{A1} during ϕ_{180} with a switch and a capacitor C_B as shown in Fig. 4. This additional switch down-converts V_{A1} to V_{B180}, the baseband voltage in capacitor C_B. This results in a 6 dB voltage gain compared to V_{C1}. Likewise voltages V_{A2}, V_{A3}, and V_{A4} can be read-out during ϕ_{270}, ϕ_0, and ϕ_{90} respectively while achieving a passive voltage gain of 6 dB compared to their respective capacitor voltages V_{C2}–V_{C4} [26].

What we described above can be seen as "Capacitive Stacking", a technique commonly used in switched capacitor voltage multipliers [27]. However such multipliers explicitly reconfigure a switched capacitor circuit. For example, 2 parallel capacitors are first charged to the same voltage and then reordered to form a 'stacked' series combination, so that the voltage doubles. Switches are used for re-ordering and they introduce parasitic capacitance causing multiplier loss. In contrast, we don't add any extra switches to realize the stacking here. The stacking occurs already in a bottom-plate mixer when we read-out from the bottom-plate of the capacitors. Hence we refer to this technique as *"Implicit Capacitive Stacking"* [26].

On a side note, voltage read-out through capacitors is preferred here for its simple implementation. Any voltage sensing circuit with sufficiently high input impedance in the desired band can be used after the switches [5], [26]. Moreover, we can also read-out from the node V_{A1} during ϕ_{90} and ϕ_{270} but this would result in complex addition ($V_{C1}(-1+i)$ and $V_{C1}(-1-i)$) with comparatively lower gain. Here ϕ_{180} is chosen for reading the node V_{A1}, as it provides real addition $V_{C1}(-1+(-1))$ resulting 6 dB V-V gain [26]. On the other hand, complex addition could be useful for applications such as beam-forming or harmonic rejection.

III. Analysis of the Proposed Front-End

In this section we will analyze the transfer function of the N-path filter/mixer circuit with the proposed implicit capacitive stacking with two main aims: 1) verify the in-band achievable 6 dB voltage gain; and 2) find the frequency dependence of the conversion gain, especially the selectivity of the N-path filtering. We will use a recently introduced simplified analysis for N-path filters/mixers using the adjoint network [28].

A. Transfer function using adjoint network

The bottom-plate mixer circuit in Fig. 3b can be split into two independent kernels, one for the in-phase and one for the quadrature phase signal. Since these kernels have the same configuration, analysis of one kernel will hold for the other. Here we will analyse the quadrature-phase kernel, shown in Fig. 5a, where phases ϕ_{90} and ϕ_{270} periodically switch the capacitors C_2 and C_4 to ground respectively. Capacitors C_{B2} and C_{B4} are the relevant output capacitors. Let the capacitance of C_2 and C_4 be C and C_{B2} and C_{B4} be C_B respectively.

Using the method described in [28], we construct an adjoint network for the Quadrature-phase kernel as shown in Fig. 5b. The passive elements in the kernel are retained in the adjoint network, however they are periodically switched with clocks

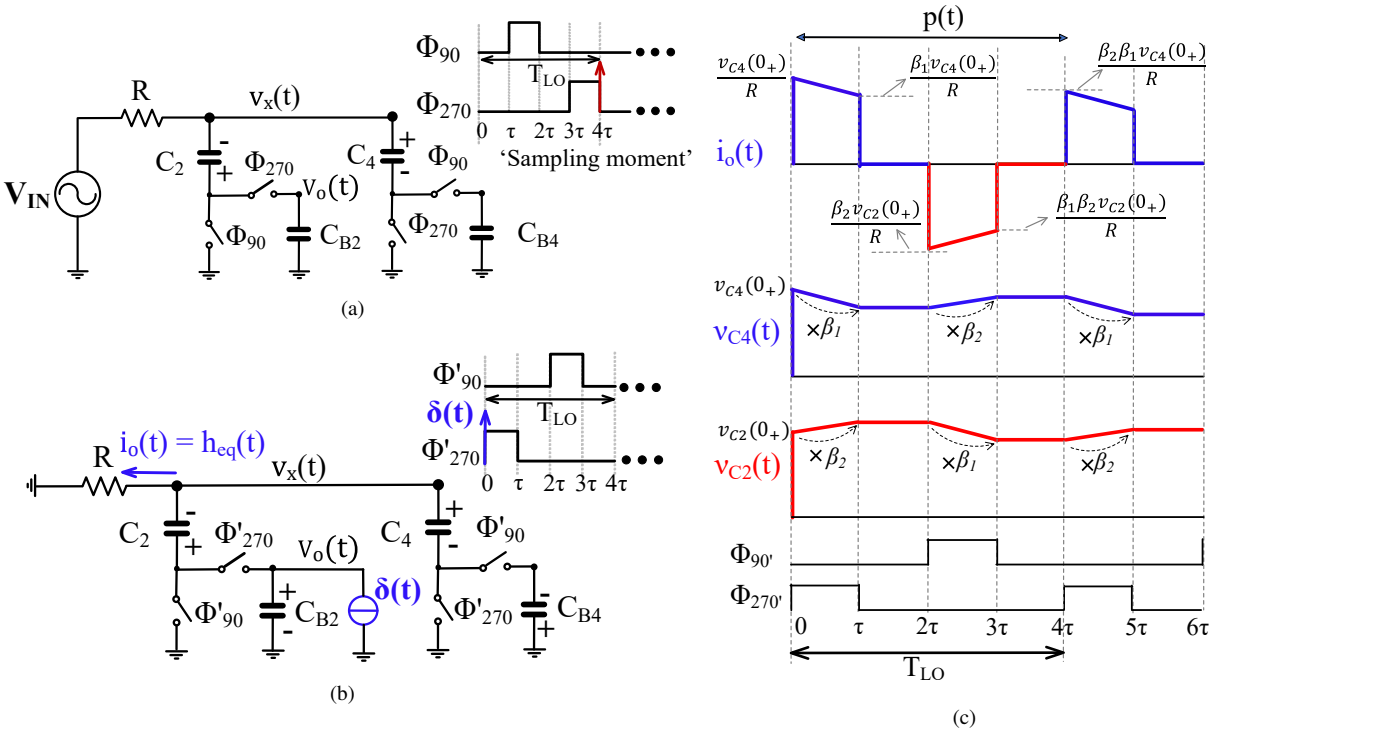


Fig. 5: (a) Quadrature-phase kernel of the 4-path Filter/Mixer with proposed read-out technique, (b) Adjoint network of the kernel with reversed clock phases ϕ'_{90} and ϕ'_{270}, and (c) Voltage and current waveforms in the adjoint network.

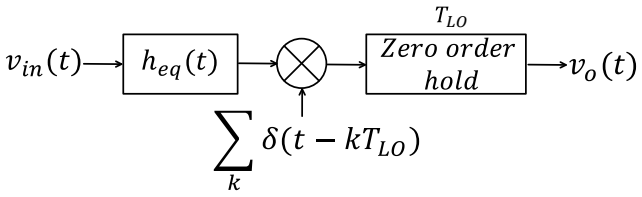


Fig. 6: Transfer function of the proposed mixer using $h_{eq}(t)$.

whose timing waveform is exactly reversed ($\phi_{90} \rightarrow \phi'_{90}$ and $\phi_{270} \rightarrow \phi'_{270}$). The input voltage source is replaced with a short to ground and the output node, $v_o(t)$ is driven by a current impulse, $\delta(t)$. Since the output $v_o(t)$ is sampled at the end of phase ϕ_{270} in the kernel, the current impulse is introduced to the adjoint network at $t = 0_+$ during ϕ'_{270}, as shown in the figure. The resulting current, $i_o(t)$, flowing through the resistance R in the adjoint network is the impulse response, $h_{eq}(t)$ of the linear time-invariant equivalent of the kernel [28]. The complete response of the proposed front-end can be obtained using $h_{eq}(t)$ as shown in Fig. 6.

The current $i_o(t)$ can be given as $v_x(t)/R$ during the phase ϕ'_{270} and ϕ'_{90}. $v_x(t) = v_{C4}(t)$ during ϕ'_{270} and it is equal to $-v_{C2}(t)$ during ϕ'_{90}. For $\tau \leq t < 2\tau$ and $3\tau \leq t < 4\tau$, all the switches in the adjoint network are open, hence $i_o(t) = 0$. The capacitor voltages do not change during these time slots.

Upon application of the current impulse $\delta(t)$, at at $t = 0_+$, the capacitor C_{B2} is charged to $v_o(0+) = 1/C_T$, where $C_T = C_B + C/2$. And the initial voltage across R, $v_x(0+) = v_{C4}(0+) = 1/(C + 2C_B)$. Additionally, $v_{C4}(0+) = v_{C2}(0+)$ since the capacitors C_2 and C_4 are equal and in series.

During ϕ'_{270}, the capacitors discharge through R. Voltage v_{C4} decay exponentially, with a time constant RC_{eq}, where $C_{eq} = C + CC_B/(C + C_B)$. At $t = \tau-$,

$$v_{C4}(\tau-) = v_{C4}(0+)e^{-\tau/RC_{eq}} \equiv \beta_1 v_{C4}(0+) \quad (1)$$

where, $\beta_1 = \exp(-\tau/RC_{eq})$. Similarly, $v_{C2}(\tau-)$ can be expressed as $\beta_2 v_{C2}(0+)$ where,

$$\beta_2 \approx 1 + \frac{C_B}{C + C_B}(1 - \beta_1) \quad (2)$$

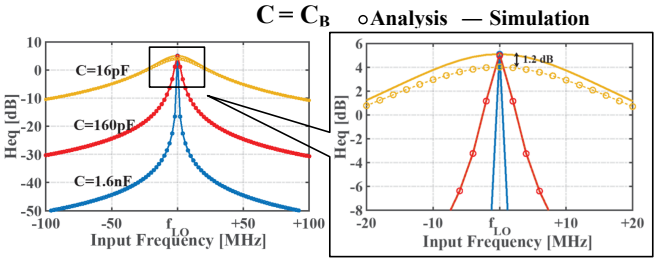
It should be noted that the polarity of v_{C2} is opposite to v_o and v_{C4} and the capacitor C_2 gets charged by the capacitor C_{B2} during ϕ'_{270}. Hence the $\beta_2 > 1$ indicating v_{C2} increase. At $t = 2\tau+$, the positive node of C_2 is shorted to ground and C_{B4} is connected to C_4. Charge redistribution occurs between C_2, C_4,and C_{B4}. It will complicate the transfer function derivation. So to make the analysis simpler, we assume that $C_B \ll C$ and charge distribution at $t = 2\tau+$ has negligible effect on v_{C4} and v_{C2}. Later, we will quantitatively show that this assumption is in practice an acceptable approximation.

Based on the above assumption, $v_{C4}(2\tau+) = v_{C4}(\tau-)$ and $v_{C2}(2\tau+) = v_{C2}(\tau-)$. Further, $v_x(t) = -v_{C2}(t)$, for $2\tau \leq t < 3\tau$. During ϕ'_{90}, v_{C2} decays exponentially with time constant RC_{eq}. At $t = 3\tau-$,

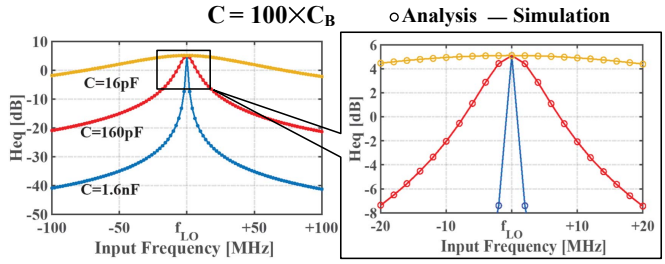
$$\begin{aligned} v_{C2}(3\tau-) &= v_{C2}(\tau+)e^{-\tau/RC_{eq}} = \beta_1\beta_2 v_{C2}(0+) \\ v_{C4}(3\tau-) &= \beta_2\beta_1 v_{C4}(0+) \end{aligned} \quad (3)$$

Using the above analysis, we constructed the waveform of $i_o(t), v_{C4}(t)$,and $v_{C2}(t)$. We denote $i_o(t)$ for $0 \leq t < T_{LO}$ by $p(t)$, as shown in Fig. 5c.

At $t = T_{LO}+ = 4\tau+$, the discharging process repeats with capacitor C_4 connected to ground again and C_2 connected to C_{B2}. However, the initial voltages of v_{C4} and v_{C2} are



(a)



(b)

Fig. 7: Comparison of analytical and simulated $H_{eq}(f)$, for the circuit shown in Fig. 4 with $f_{LO} = 1\,\text{GHz}$ $C = 16\,\text{pF}$, $160\,\text{pF}$ and $1.6\,\text{nF}$ and for (a) For $C = C_B$ and (b) For $C = 100 \times C_B$.

now $\beta_1\beta_2 v_{C4}(0+)$ and $\beta_1\beta_2 v_{C2}(0+)$ respectively. It means that the waveform $p(t)$ repeats every clock period T_{LO} with initial capacitor voltages scaled by a factor $\beta_1\beta_2$. If $h_{eq}(t)$ is the response for $v_{C4}(0+)$ and $v_{C2}(0+)$, then response for $v_{C4}(T_{LO}+)$ and $v_{C2}(T_{LO}+)$ should be $\beta_1\beta_2 h_{eq}(t - T_{LO})$.

Following the approach employed in [28], we can rewrite the impulse response $h_{eq}(t)$ as,

$$h_{eq}(t) = p(t) + \beta_1\beta_2 h_{eq}(t - T_{LO}) \tag{4}$$

In the frequency domain,

$$H_{eq}(f) = \frac{P(f)}{1 - \beta_1\beta_2 e^{-j2\pi f T_{LO}}} \tag{5}$$

From the Fig. 5c, we note that $p(t)$ can be described as a sum of decaying exponentials as shown below,

$$\begin{aligned} p(t) = \frac{v_x}{R}(h(t) - \beta_1 h(t-\tau)) \\ - \beta_2\left(h(t-2\tau) - \beta_1 h(t-3\tau)\right)) \end{aligned} \tag{6}$$

where $h(t) \equiv e^{-t/RC_{eq}} \cdot u(t)$ and $u(t)$ denotes unit-step function. The fourier transform of $p(t)$ is given as,

$$\begin{aligned} P(f) = \frac{H(f)}{R(C+2C_B)}(1 - \beta_1 e^{-j2\pi f\tau} \\ - \beta_2(e^{-j4\pi f\tau} - \beta_1 e^{-j6\pi f\tau})) \end{aligned} \tag{7}$$

where, $H(f) = RC_{eq}/(1 + j2\pi f RC_{eq})$. Finally, $H_{eq}(f)$ can be obtained using (5) and (7).

Fig. 7a and Fig. 7b compares the Spectre simulation results with analytical equation of $H_{eq}(f)$ for $f_{LO} = 1\,\text{GHz}$, $R = 50\,\Omega$, and three different values of $C_B = 16\,\text{pF}$, $160\,\text{pF}$ and $1.6\,\text{nF}$. For the ratio of $C/C_B = 1$, the in-band gain estimation is $1.2\,\text{dB}$ smaller than the simulation results. This is due to our assumption of negligible charge distribution. We find that the difference between simulation and analytical model decreases rapidly with increase in C/C_B ratio. It becomes less than 0.3 dB for $C/C_B > 4$. At out-of-band, the simulation and analytical results are in agreement irrespective of the ratios.

B. Linearity considerations - Impedance up-conversion

N-path passive mixer-first front-ends often use large switches with power-hungry LO drivers to achieve high OOB linearity. In [29], the maximum achievable OOB-IIP3 in a N-path passive mixer/filter is estimated as:

$$V_{IIP3} = \sqrt{\frac{4}{3}\frac{(1+\rho)^4}{\rho^3(2g_2^2 - g_3(1+\rho))}} \tag{8}$$

where ρ is the ratio of switch resistance, R_{sw} to source resistance R_s ($\rho = R_{sw}/R_s$), g_2 and g_3 are calculated from the 2nd and 3rd derivation of $I_D(V_{DS})$. It can be shown that $g_2 = (2V_{OD})^{-1}$ and $g_3 = -(2V_{SAT}^2)^{-1}$, where V_{OD} is overdrive voltage and V_{SAT} is velocity saturation parameter, respectively. According to (8), low ρ or high R_s/R_{sw} ratio results in large V_{IIP3}.

In this work, we propose to increase the R_s/R_{sw} ratio by increasing the source resistance R_s rather than reducing R_{sw} [17], [30]. This allows for achieving good linearity at low power consumption. The principle of using impedance conversion to lower the power consumption is similar to that of matching networks in other low-power RF front-ends [19]–[22]. However, there the primary aim is to exploit voltage gain due to impedance up-conversion and achieve low noise figure at low power. We also target high OOB linearity performance in our mixer-first RX here [26]. Though the voltage gain is a benefit for NF, it increases in-band swing and limits the achievable in-band linearity. A limitation associated with a large R_s is the large signal loss due to unwanted low pass filtering caused by parasitic capacitance at RF nodes [31]. Hence the trade-off between out-of-band linearity and signal loss due to unwanted filtering determines the optimal R_s. Transformers with wide bandwidth are preferred to cover multiple RF bands with tunable N-path filters [26].

IV. Design and Implementation

In this section, we will discuss the design considerations and circuit implementation of a RF front-end with the proposed capacitive stacking technique.

A. Design considerations

In Section III, ideal capacitors and switches are used for the transfer function analysis of implicit capacitive stacking. However, the real capacitor has parasitic capacitance to substrate. Let us qualitatively examine the behavior of the proposed 4-path filter/mixer with parasitic capacitances.

The proposed 4-path filter/mixer with equivalent parasitic capacitance, C_P at the RF input is shown in Fig. 8. The parasitic capacitances of C_{1-4} are always connected to the RF input. Hence the parasitic capacitance of the floating capacitors introduce signal loss by shunting it to ground, i.e., passive low-pass filtering occurs due to R_s and C_P before the N-path

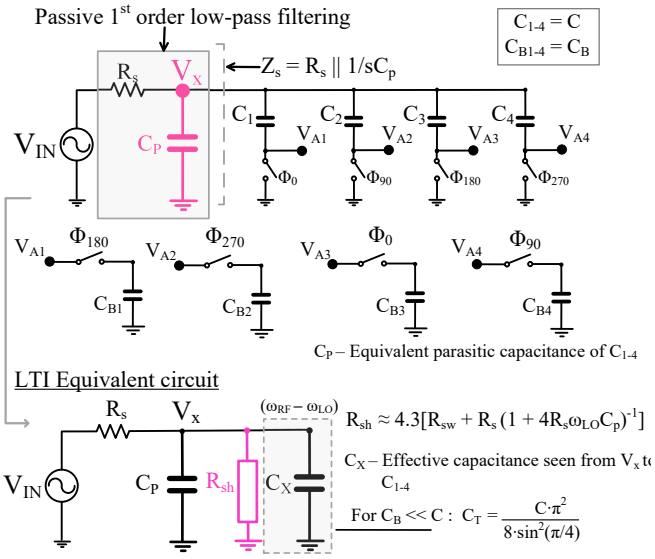


Fig. 8: Proposed 4-path filter/mixer with equivalent parasitic capacitance, C_P and its LTI equivalent model for Z_{in} estimation.

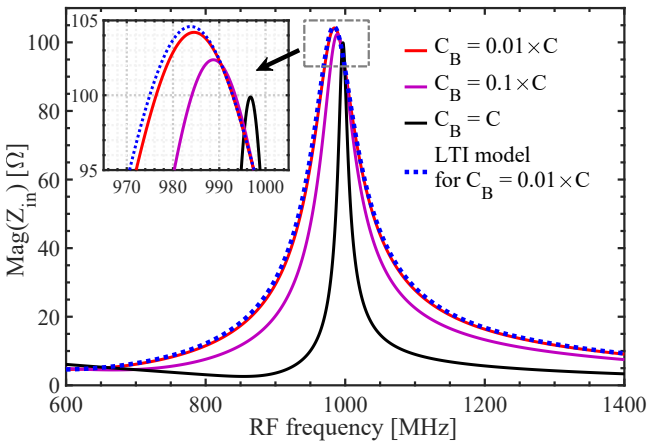


Fig. 9: Input impedance of the proposed 4-path filter/mixer with f_{LO} = 1 GHz, C = 10 pF, C_P =1.2 pF and R_{sw} = 2Ω for 3 different C/C_B ratios and its zoomed version.

filtering. It should be noted that the parasitic capacitance of C_{B1-4} are isolated from the RF input through mixer switches. Hence they cause no signal degradation at the RF input and do not contribute to C_P. On the other hand, the parasitics of the mixer switches will contribute to C_P. However, employing a step-up transformer will significantly reduce the size of the switches in this design. Hence for the discussion here, C_P will be the equivalent parasitic capacitance of C_{1-4}.

Besides input signal attenuation, C_P also shunts the harmonic content of the up-converted baseband signals stored in the capacitors. This adds up to the signal loss and is usually accounted by a harmonic shunt impedance, R_{sh} [6]. Since the mixer switches see a frequency-selective source impedance (Z_s), the R_{sh} depends on the input frequency as discussed in [29] [31].

$$R_{sh}(\omega_{LO}) = 4.3\left(R_{sw} + \frac{R_s}{1+4R_s\omega_{LO}C_P}\right) \tag{9}$$

As shown in Fig. 8, an LTI equivalent model for the proposed 4-path filter/mixer can be developed using the principles elaborated in [6]. The adequacy of the LTI equivalent circuit will be discussed for two scenarios: (1) $C_B \ll C$ and (2) $C_B \approx C$. When $C_B \ll C$, the capacitors C_{B1-4} has negligible loading effect on C_{1-4}. This means C_{1-4} loses negligible charge to C_{B1-4} when they are connected together. It causes C_{1-4} to behave similar to mixing capacitors in the N-path bottom-plate filter, analyzed in [14]. Hence, the effect of C_{1-4} can be quantified using an equivalent up-converted capacitance C_X in the LTI equivalent circuit. For second scenario , as C_B increases, it takes significant charge from C_{1-4}. Nonetheless, C_B still settles to $2\times V_C$, albeit at a slower rate. Hence the signal loss at zero-IF remains almost identical to the previous case with $C_B \ll C$. However by loading C, C_B increases the effective capacitance seen from the RF input compared to Case : $C_B \ll C$ and reduces the RF-bandwidth resulting in more selective filtering. It implies that the LTI equivalent circuit in Fig. 8, can be re-used provided C_X is adjusted to accommodate the loading effect of C_{B1-4} on C_{1-4}. On the other hand, for Z_{in} at $f_{RF} = f_{LO}$, the LTI equivalent circuit described is sufficient for both the scenarios with the frequency-dependent R_{sh}, given in (9).

The adequacy of the LTI equivalent model for Z_{in} estimation is verified through simulation results presented in Fig.9. The Z_{in} estimated from LTI equivalent model is compared with that of proposed 4-path filter/mixer for 3 different C/C_B ratios. The circuit is simulated at 1 GHz f_{LO} with C =10 pF, C_P = 1.2 pF, and R_{sw} = 2 Ω. C_X in the LTI equivalent circuit is calculated for the case: $C_B \ll C$. From the results, we see that Z_{in} at $f_{RF} = f_{LO}$ is close to the LTI estimation for all the 3 ratios. As expected, for the ratio C/C_B =1, the Z_{in} is much narrower upholding the inference that C_X increases with C_B. Interestingly, a right shift in peak Z_{in} is also noticed with increase in C_B. This means C_B re-distributes the charge on C_{1-4} and C_P to reduce the phase shift introduced due to charge sharing between C_P and C_{1-4}.

Exploiting the LTI equivalent model, we infer the following design insights.

1) At $f_{RF} = f_{LO}$, Z_{in} is approximately equal to R_{sh}. This means impedance matching at f_{LO} depends on the magnitude of R_{sh}, which in turn is determined by R_s and C_P. Hence, parasitic of C_{1-4} should be optimized to achieve desired impedance matching at f_{LO}.
2) C and C_B defines the bandwidth of the transfer function and Z_{in}. C_B can be used to orthogonally define the bandwidth with negligible effect on the Z_{in}.
3) Step-up transformers increase the effective source impedance, R_U, seen by the mixer switches. As a result, it increases the OOB linearity of the filter/mixer as it lowers the R_{sw}/R_U ratio. However, it simultaneously lowers the parasitic pole $1/C_P R_U$. This means gain degradation is possible if the parasitic pole is lower than f_{LO} despite the voltage step-up. In short, impedance up-transformation through a step-up transformer limits the operating frequency range. For higher frequency operation, the parasitic pole $1/C_P R_U$ should be pushed away to avoid gain degradation.

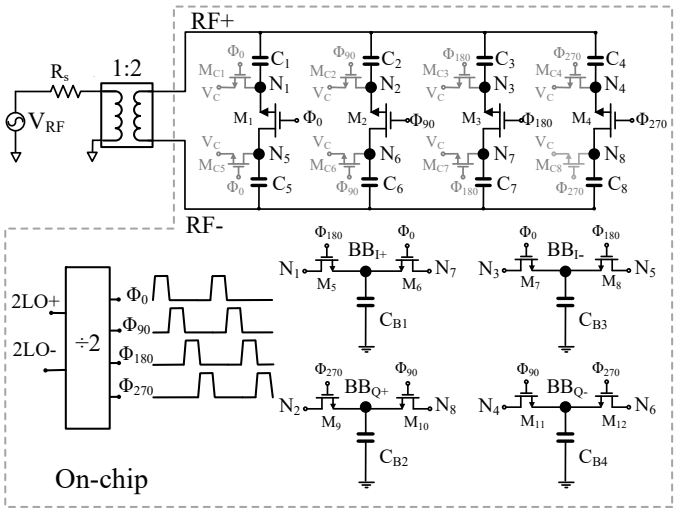


Fig. 10: Complete architecture of the implemented RF front-end

4) Mixer switches can be sized up to provide low switch resistance and increase the OOB linearity at the cost of power consumption [29].

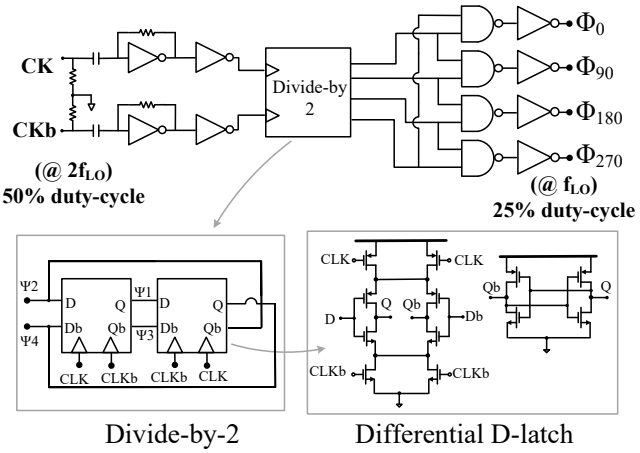
As mentioned in the Section I, inspired by the NB-IoT standard, we chose the operating frequency, f_{LO}, in the range of 0.7 – 1.0 GHz [2]. Such f_{LO} also facilitate us to experiment with multiple "off-the-shelf" transformers. Further we chose a step-up transformer with turn-ratio 1:2 to achieve >20 dBm OOB IIP3 while targeting ≤1 mW of power at f_{LO} =1 GHz.

B. Bottom-plate N-path filter with bottom-plate read-out

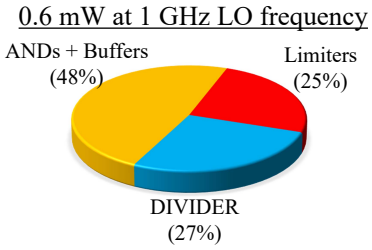
The circuit schematic of the fully-differential implementation of the proposed RF front-end is shown in Fig. 10. It is composed of an off-chip transformer, a differential 4-path bottom-plate filter with the proposed read-out circuit and a 4-phase LO generator. With no other active circuitry, clock drivers determine the total power consumption of the RF front-end. An off-chip transformer is preferred for its low insertion loss which is good for NF.

All the mixer switches ($M_1 - M_{12}$) in the front-end are implemented with NMOS transistors of $W/L = 9.6\,\mu m/20\,nm$. When turned on, these switches provide a differential resistance of 38 Ω. For these transistors, V_{OD} = 0.302 V and V_{SAT} = 0.248 V. Employing this in (8), the front-end should achieve an OOB-IIP3 of +24 dBm with a 1:2 step-up transformer. The simulation results also report similar OOB IIP3 of +25 dBm with these small switches. NMOS switches $M_{C1} - M_{C8}$ with 4× smaller W/L are used to periodically reset the dc common-mode level of mixer switches from an external supply V_C [14].

All the capacitors are Metal-oxide-metal (MOM) capacitors with Metal 7 as top-layer and Metal 3 as bottom-layer to reduce the total parasitic capacitance to substrate. Based on QRC extraction, the parasitic capacitance is about 1.3% of the MOM capacitance. Parasitic capacitance of C_{1-8} together with source impedance provides unwanted low-pass filtering resulting in signal loss and causes Z_{in} degradation [31]. To reduce the signal loss and achieve desired impedance matching at f_{LO} = 1 GHz, C_{1-8} is chosen to be 6.4 pF in this design. Switches $M_5 - M_{12}$ isolate C_{B1-4} and their parasitic capacitances from the RF terminal when they are turned off. C_{B1-4} determines the shape of Z_{in} at out-of-band frequencies and the -3 dB bandwidth of RF-RF transfer gain, $f_{-3\,dB,RF}$. Using the transfer function given in (5), we estimated that a 15 MHz IF bandwidth is desirable to achieve filtering and >+20 dBm IIP3 at 80 MHz. Hence, we chose C_{B1-4} to be 4.2 pF so that together with load capacitance of the measurement probe, a 30 MHz $f_{-3\,dB,RF}$ is realized.



(a)



(b)

Fig. 11: Multiphase LO generation – (a) Implementation and (b) Power consumption breakdown

C. Multiphase LO generation

All the switches are driven by 4-phase non-overlapping 25% duty-cycle clocks, generated using on-chip frequency divider and multi-phase generator. As shown in Fig. 11a, the clock generation circuitry employs divide-by-2 circuit to generate 50% duty-cycle quadrature clocks from an input differential clock at $2f_{LO}$. These 50% duty-cycle quadrature clocks are ANDed with each other to generate 25% duty-cycle non-overlapping quadrature clocks at the same frequency. Equal rise and fall time in LO buffers ensures the shape of LO pulses throughout the propagation and maintains the desired duty-cycle. For similar rise and fall time, PMOS and NMOS transistors in LO buffers should have equal driving capability. In conventional CMOS process, the PMOS should be typically 2-3× larger than the NMOS to achieve equal driving strength, i.e., $W_p \simeq 3W_n$, assuming minimum gate length L for all the transistors. This results in an input capacitance, $C_{in} = 4W_nL$. On the other hand, GF22 nm FDSOI uses SiGe channel in the PMOS transistors to achieve driving capability similar to that

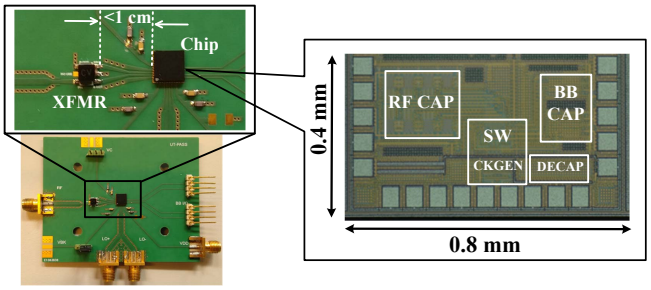


Fig. 12: Die Micrograph in 22 nm FDSOI CMOS and PCB showing short-traces (<1 cm) between transformer and chip.

of NMOS. This means equal W/L and $C_{in} \approx 2W_nL$, i.e., $2\times$ smaller than that of conventional process, resulting in lower power consumption. Fig. 11b shows the power consumption breakdown of multi-phase LO generation circuit.

V. Measurement Results

The chip photo of the receiver prototype, implemented in GF22 nm FDSOI CMOS technology, is shown in Fig. 12. The total- and active area of the chip are 0.32 mm^2 and 0.23 mm^2 respectively. The chip is mounted on 5x5 QFN40 package and assembled on a Printed Circuit Board (PCB) for measurement. It consumes 0.4 - 0.78 mW of power in the frequency range 0.6 - 1.3 GHz, all due to the dynamic power dissipation in the divider and the switch-drivers.

An off-chip $0.2-1.4$ GHz transformer (Minicircuits TC4-14X+), with turn ratio 1:2, is used as balun at the chip RF input. As shown in Fig. 12, transformer and chip are placed together in the PCB to minimize the path loss. All the measurement results include the insertion loss of the transformer. Measured insertion loss of the transformer is shown in Fig. 13a. The transformer achieves ≤ 1 dB insertion loss upto 0.9 GHz and then the loss degrades to 3 dB at 1.3 GHz.

An external buffer-amplifier (TELEDYNE LECROY AP033 Active Differential Probe) with high input impedance is used at the baseband to drive the 50 Ω measurement equipment without loading the capacitors. It also serves as active balun with differential input and single-ended 50 Ω output.

A. Gain, S11, and NF

From the theory, the 1:2 step-up transformer and implicit capacitive stacking contributes 6 dB voltage gain each to the front-end. Additionally, the maximum input impedance of the front-end is designed to be between 90 and 100 Ω. This results in $1-2$ dB extra voltage gain, compared to 50 Ω matched condition. Together, the front-end should achieve 14 dB gain ideally. Figure 13c shows the simulated and measured RF-to-baseband voltage conversion gain and S_{11} for a LO frequency of 1 GHz. The front-end achieves a conversion gain of 13 dB and a $f_{-3\,\text{dB,RF}}$ of 27 MHz. Ideal matching and minimum S_{11} will occur at the frequency where the input impedance of the front-end is a complex conjugate of the source impedance. Bondpad capacitors and the parasitic capacitance of C_{1-8} results in complex source impedance with negative imaginary component at the RF input [6] [31]. The baseband capacitance on up-conversion provides positive reactance for frequencies lower than LO at the RF input, facilitating complex conjugate match in one of those frequencies. Hence, the S_{11} minimum shifts to a frequency in the lower sideband of the LO, as observed in the Fig. 13c. Similarly, the peak gain frequency will also shift to the left of LO due to parasitic capacitance. However the amount of frequency shift is governed by the transfer function and it is different from the S_{11} shift [32]. Both shifts can be compensated using complex feedbacks [6], though not implemented here.

Figure 13b shows the measured voltage conversion gain and S11 as a function of RF frequency for LO$= 0.6-1.3$ GHz. The gain degrades from 14 dB at $f_{LO} = 0.9$ GHz to 9 dB at 1.3 GHz. This degradation is due to insertion loss of the transformer, shown in Fig. 13a and the parasitic substrate capacitance of the C_{1-8} connected at the RF terminal. The increase in insertion loss versus frequency is reflected in the measured noise performance in Fig. 13a. A 5 dB NF achieved at 0.6 GHz LO degrades to 9 dB at 1.3 GHz.

B. Linearity performance

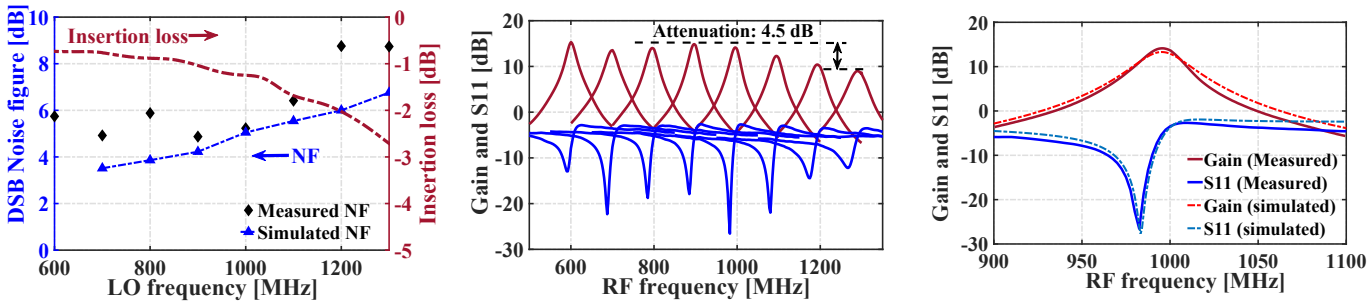
Linearity of the front-end is characterised using two-tone intermodulation tests. For IIP2 measurements, test tones are introduced at $f_1 = f_{LO}-\Delta f$ and $f_2 = f_{LO}-\Delta f+5$ MHz and for IIP3 measurements, they are introduced at $f_1 = f_{LO}-\Delta f$ and $f_2 = f_{LO}-2\Delta f+5$ MHz. In both scenarios, the resulting IM2 and IM3 products will be seen at a constant baseband frequency of 5 MHz, well within the 16 MHz $f_{-3\,\text{dB,BB}}$. The measured IIP2 and IIP3 performance as a function of relative frequency offset $\Delta f/f_{-3\,\text{dB,BB}}$ for $f_{LO} = 1$ GHz is shown in Fig. 14a. For far-off interferers with $\Delta f/f_{-3\,\text{dB,BB}} = 10$, the proposed front-end achieves an out-of-band IIP3 of +25 dBm and IIP2 of +66 dBm. Measurement results confirm the OOB-IIP3 estimation of (8). Thus, it validates the two-fold benefits of impedance upconversion discussed in Section III. *Simultaneous improvement in the noise figure due to in-band voltage gain and increased OOB-IIP3 due to high R_s/R_{sw} ratio* [26].

For near-by interferers ($\Delta f/f_{-3\,\text{dB,BB}} = 1$), the front-end achieves an IIP3 of +10 dBm and IIP2 of +44 dBm. It also achieves an in-band 1dB gain compression point (CP1dB) of -7.5 dBm. Such high in-band IIP3 and CP1dB is possible due to the fully-passive implementation. The linearity performance of the front-end across the operating frequency range is presented in Fig. 14b.

C. Blocker tolerance

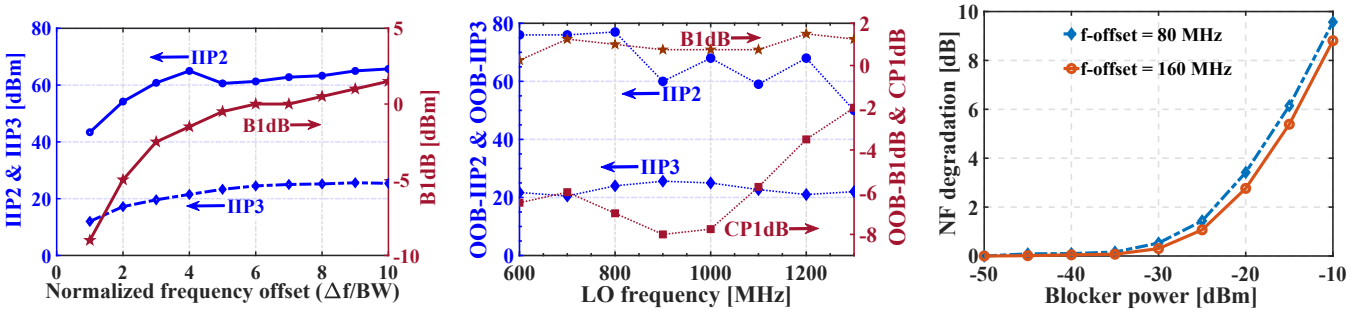
To evaluate the blocker tolerance of the proposed front-end, we measured out-of-band Blocker 1 dB compression point, B1dB and Blocker noise figure. Fig. 14a shows the measured B1dB as a function of the relative frequency offset ($f_{\text{blocker}}/f_{-3\,\text{dB,BB}}$), for $f_{LO} = 1$ GHz. The desired signal is introduced at 998 MHz ($f_{\text{BB}} = 2$ MHz) and the blocker signal power is measured for 1 dB gain degradation of the desired signal. For blockers located at 80 MHz offset ($5 \times f_{-3\,\text{dB,BB}}$), the front-end exhibits a B1dB of -1 dBm.

Figure 14c shows the measured NF-degradation as a function of blocker input power for $f_{LO} = 1$ GHz. The measurement reports that NF degrades by 5 dB for a -15 dBm



(a) (b) (c)

Fig. 13: (a) Measured insertion loss of the transformer; and simulated and measured inband noise figure for multiple LO; (b) Measured gain and S_{11} vs. RF for multiple LO; (c) Simulated and measured gain and S_{11} vs. RF for LO =1 GHz.



(a) (b) (c)

Fig. 14: (a) Measured linearity performance: IIP3, IIP2 and B1dB vs. relative frequency offset $\Delta f/f_{-3\,\mathrm{dB,BB}}$; (b) Measured Linearity performance (IIP3, IIP2, and B1dB at $\Delta f/f_{-3\,\mathrm{dB,BB}} = 10$) and in-band CP1dB for multiple LO frequencies; (c) Measured NF degradation due to blockers for f_{LO} = 1 GHz. (DSB-NF = 5 dB for no blockers).

blocker located at 80 MHz away from f_{LO}. Since the measured B1dB (-1 dBm) is higher than -15 dBm, it is clear that the NF degradation is largely due to LO phase noise from the on-chip multi-phase generation. Since sub-mW power consumption is targeted here, the LO phase noise is not as good as high-performance RXs [9] [16]. On the other hand, the achieved blocker NF of 10 dB for a -15 dBm blocker is competitive with other sub-mW RF front-ends. For example, the 1.15 mW RX, reported in [24], achieves a blocker NF of 13.7 dB for a -20 dBm blocker located at 50 MHz offset.

D. LO leakage

Any mismatch between the mixer switches and LO buffers results in asymmetric leakage of LO signal from gate to the drain terminal of the switches [33]. Imbalance between the differential terminals of the transformer will also contribute to LO leakage in this implementation. Hence, careful layout is carried out and dummy transistors are used to improve the matching. To account for process variation, LO leakage is measured for 4 different samples. As shown in Fig. 15, the proposed RF front-end achieves < -70 dBm LO leakage across the operating frequency range.

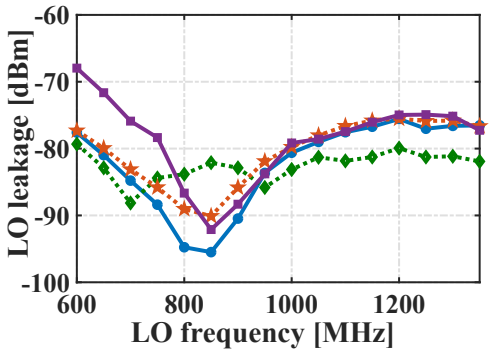
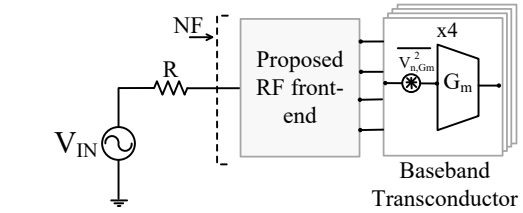


Fig. 15: Measured LO leakage at RF port (for 4 different samples.)

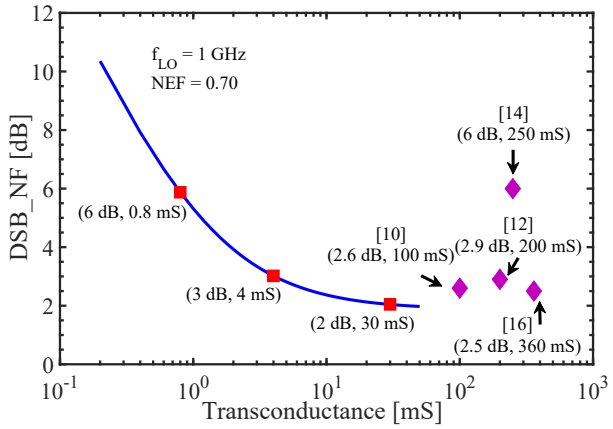
E. Performance Comparison

Performance summary of the proposed RF front-end and a comparison with state-of-the-art mixer-first front-ends is shown in Table I. From the table, it is clear that this work achieves comparable OOB linearity with $\geq 10\times$ lower power than several high-performance mixer-first front-ends. On the other hand, when compared to other sub-mW RF front-ends in Table II, the proposed work shows $\sim$20 dB improvement in the OOB IIP3 while exhibiting competitive noise figure of 5 dB.

Admittedly, additional baseband amplification and channel filtering will be needed in practice to adopt this architecture in a low-power RX, at the cost of power. To achieve 6 and 3 dB NF, the proposed front-end requires 0.8 and 4 mS of transconductance respectively, at the first baseband stage after the front-end. Assuming $\mathrm{gm/I_d} = 10$ (biasing in strong inversion



(a)



(b)

Fig. 16: Design set-up to estimate the Noise figure of the complete front-end and (b) Simulated DSB NF vs. Transconductance at the 1^{st} stage of baseband circuitry.

for linearity), this leads to a current consumption of 320 μA and 1.6 mA of current respectively, for 4 baseband transconductors. It is much less compared to baseband circuitry in other state-of-the-art mixer-first front-ends, shown in Fig. 16b. We estimated these numbers using the simulation setup illustrated in Fig.16a, similar to the methodology described in [10]. On the other hand, the baseband amplifiers may degrade the in-band linearity performance of the proposed front-end. For out-of-band linearity, the design of baseband amplifiers is relaxed by the 20 dB attenuation provided by the proposed RF front-end and facilitates competitive linearity performance. Another way to improve linearity might be the use of LC resonant tanks instead of transformers to achieve impedance up-conversion. The band-pass behavior of LC resonant tank improves the out-of-band blocker attenuation at the cost of noise [29] and flexibility in operating input frequency.

VI. Conclusion

This paper described and analyzed implicit capacitive stacking in a bottom-plate N-path filter/mixer which results in 2× voltage gain in a fully-passive switch R-C circuit. Passive voltage gain facilitates low noise figure at the cost of additional capacitor area. Further, an off-chip step-up transformer with 1:2 turn ratio is employed to achieve 6 dB voltage gain and high OOB linearity with small mixer switches. A 600 μW fully-passive RF front-end achieving 13 dB gain, 5 dB NF and +25 dBm OOB-IIP3 is demonstrated, opening up a possibility for highly-linear RX for low power IoT and software defined radio applications.

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TABLE I
RESULT SUMMARY AND COMPARISON WITH HIGH-PERFORMANCE MIXER-FIRST RECEIVERS

Features	**JSSC10 [6]**	**RFIC15 [11]**	**ISSCC15 [12]**	**RFIC16 [30]**	**JSSC18 [16]**	**This Work**
Technology	65 nm	65 nm	65 nm	65 nm	45 nm SOI	22 nm FDSOI
Frequency [GHz]	0.1 - 2.4	2 - 3	0.1 - 1.5	0.03 - 0.3	0.2 - 8	0.6 - 1.3
Power (Analog) [mW]	30	8.2	11@1.5 GHz [a]	36	50	0[b]
Power (Digital - Clock) [mW]	7.2 - 39.6	19.2 - 67.2		7.2 - 10.1	6 - 240	0.4 - 0.78
Gain [dB]	40 - 70	7.5	38	21-36	21	9 - 14
BB BW [MHz]	10	3 - 10	2	2 - 40	10	16
DSB-NF [dB]	3 - 5	2.5 - 4.5	2.9	6	2.3 - 5.4	5 - 9
OOB IIP3[dBm @ Δf/BW]	25 @ 10	26 @ 33.3	10 @ 15	41 @ 20	39 @ 8	25 @ 10
OOB IIP2[dBm @ Δf/BW]	56 @ 10	65 @ 33.3	47 @ 15	90 @ 20	88 @ 8	66 @ 10
B1dB [dBm @ Δf/BW]	10 @ 10	3 @ 33.3	N.A.	11 @ 27.5	12 @ 8	1 @ 10
LO leakage [dBm]	<-65	<-60	N.A.	N.A.	<-65	<-70
Supply [V]	1.2/2.5	1.2	0.7/1.2	1.2	1.2	0.8
Active Area [mm^2]	0.75	0.23	0.028	0.8	0.8	0.23
Matching Network / Balun	None	Off-chip 180°Hybrid Coupler[c]	None	Off-chip 180°Hybrid Coupler[c]	Off-chip 180°Hybrid Coupler[c]	Off-chip XFMR 1:2[d]

N.A. Not Available [a] Power consumption breakdown is not available [b] No integrated baseband [c] Coupler provides 100 Ω at differential RF input [d] Turn ratio

TABLE II
COMPARISON WITH LOW-POWER RF FRONT-ENDS

Features	**RFIC12 [19]**	**JSSC14 [24]**	**JSSC15 [21]**	**TMTT18 [22]**	**ESSCIRC18 [25]**	**This Work**
Technology	65 nm	65 nm	130 nm	28 nm	28 nm	22 nm FDSOI
Frequency [GHz]	2.45	0.43 - 0.96	2.4	2.4	2.4	0.6 - 1.3
Power [mW] / Supply (V)	0.4 / 0.8	1.15 / 0.5	0.6 / 0.8	0.64 / 0.8	0.58 / 1	0.4 - 0.78 / 0.8
Gain [dB]	27.5	50	55.5	50	19	9 - 14
BB BW [MHz]	N.A.	N.A.	2	1	3.6	16
DSB-NF [dB]	9	8.1	15.1	6.5	11.9	5 - 9
OOB IIP3 [dBm @ Δf/BW]	-21 @ N.A.	-20.5 @ N.A.	-15.8 @ 2.5	0.9 @ 10	3.3 @ 13.9	25 @ 10
Active Area [mm^2]	0.24[a]	0.2	0.25	0.25	N.A.	0.23
Matching Network	On-chip LC Q=5	None	Off-chip LC	Off-chip LC Q=50	On-chip XFMR 1:4[b]	Off-chip XFMR 1:2[b]

N.A. Not Available [a] including inductor [b] Turn ratio

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