Minority Carrier Tunneling and Stress-Induced Leakage Current for p⁺ gate MOS Capacitors with Poly-Si and Poly-Si_{0.7}Ge_{0.3} Gate Material

V.E. Houtsma*, J. Holleman*, C. Salm*, I. R. de Haan*, J. Schmitz†, F. P. Widdershoven† and P.H. Woerlee†*

* MESA Research Institute, University of Twente, P.O.Box 217, 7500AE Enschede, The Netherlands.

† Philips research Laboratories, Prof. Holstlaan 4, Eindhoven, The Netherlands.

1. Introduction

The integrity of ultra-thin oxides is a major concern for further downscaling of the gate oxide thickness. Stress-Induced Leakage Current (SILC), soft-breakdown (SB) and the increase of temperature acceleration of time-to-breakdown (TDDb) limits the downscaling of gate oxide thickness [1,2,3]. Gate oxide reliability has been studied mainly for n⁺-doped poly-Si gate devices. The degradation of PMOS gate dielectric is also a major concern. Recently, first reports on the conduction (I-V), SILC and degradation mechanisms in p⁺ gate devices are presented [4,5,6], however a complete understanding is still not available. In this paper the I-V conduction mechanism for gate injection, SILC characteristics and reliability of PMOS capacitors with p⁺-gate material on 5.6, 4.8 and 3.1 nm oxide thickness are studied. P⁺-gates with poly-Si and poly-Si_{0.7}Ge_{0.3} are used to study the influence of gate workfunction on gate current and SILC current. A new accurate model based on Minority Carrier Tunneling (MCT) from the gate is proposed for the I-V and SILC characteristics at -V_g. TDDb data are presented and discussed.

2. Experimental results and Discussion

I-V measurements are performed on gated diode structures for both gate bias polarities. Fig 1 displays the J-E characteristics of the unstressed p⁺ poly-Si and poly-SiGe capacitors (5.6 nm) for substrate and gate injection conditions (n⁺ shown as reference). The oxide field was obtained by integration of the low frequency (10 kHz) C-V curve (gated-diode). The onset of conduction at -V_g occurs at significantly higher oxide field (1.5×) than for +V_g condition. Note the difference between poly-Si and poly-SiGe for -V_g. Carrier separation technique was used in [7] to show that electron injection from the gate is dominating the tunnel current. Hole tunneling from the substrate is negligible for thicker oxides (>4 nm) (Fig 2). In Fig 3 J-E characteristics of MOS capacitors on 4.8 nm oxide with different RTA temperature are shown for -V_g. For increasing RTA temperature the J-E characteristics shift to higher oxide fields. For thick oxides (> 4 nm) there are two possible mechanisms for electron injection from the gate (Fig 2). The first possibility is valence band tunneling (VBT), however a FN expression ($\phi_b = 4.2$ eV) can not be used to fit the I-V curve at -V_g (see Fig 3) [4,8]. A second possibility is tunneling of minority carriers (MCT), i.e. electrons from the conduction band of the gate. A first order model of MCT was developed based on the Esaki-Tsu tunneling formula [9] (Table 1). The difference in energy between the Fermi level in the gate and the conduction band edge at the SiO₂ interface is gate voltage dependent due to gate depletion. The potential drop over the gate depletion layer V_{poly} is estimated from the measured C-V curves. Calculated J-E characteristics with N_a = 3·10¹⁹ cm⁻² (poly-Si and poly-SiGe) of MCT agree reasonable with measurements (Fig 4,5). This indicates that MCT is important for the gate doping used in our devices. Refining the MCT model also requires inclusion of non-uniform injection (doping level varies over grain) and the limited generation of carriers available for tunneling. The latter effect is observed in Fig 6. High frequency C-V curves on 4.8 nm oxide thickness show no sharp onset of inversion (Fig 6), hence carrier tunneling out of the gate occurs at a higher rate than that of carrier generation. This indicates that V_{poly} which is an important parameter for MCT, can be determined with limited accuracy only. The dependence on RTA temperature (Fig 3) is also explained using MCT. Gate doping at the SiO₂ interface increases with increasing RTA and a higher oxide field is needed for the same current. For very thin oxides (<4 nm) a third contribution to the I-V curve at -V_g is observed. Carrier separation measurements show that holes can tunnel from the substrate to the gate (Fig 7). This current increases strongly with electrical stress, hence it is interpreted as trap assisted hole tunneling (HTAT). This hole current increases strongly with decreasing oxide thickness and can be important for degradation of ultra-thin oxides, since hot holes are no longer needed to trigger the breakdown process [10]. This is also important for very thin oxide n⁺ gate devices at -V_g condition and as MCT for +V_g.

SILC characteristics and results are discussed below. Electrical stress has been applied on A = 4.0·10⁻⁴ cm² MOS capacitors on 5.6 nm oxide thickness using constant current stress (CCS) conditions of J = ±0.1 mA/cm². SILC was measured in a similar way as in [2]. In Fig 8 and 9 the J-E characteristics of p⁺ poly-Si and poly-SiGe gate devices are shown after various stress intervals. For -V_g injection SILC becomes apparent at much higher E. Furthermore the field dependence is different from that at +V_g. At comparable oxide field SILC is orders of magnitude smaller for -V_g stress than for +V_g stress. This is different from n⁺-poly gate devices where SILC is almost symmetric with gate polarity [2]. SILC is assumed to be due to trap-assisted tunneling (TAT) and it is observed that SILC is proportional to the neutral trap density created during stress [11]. Fig 10 shows the gate and source current of p⁺ gate MOSFETs on 4.8 nm gate oxide before and after MCT stressing. Note that after stressing an increase of source current (+I_s) is observed which flows from the source/drain to the gate and is most likely due to HTAT. The quantum yield (corrected for HTAT) before and after MCT stressing is given in Fig 11. It can be observed that the electrons in the SILC process after MCT stress lose an energy of 1.0-1.5 eV, as was also observed for n⁺ gate devices [9]. A model based on inelastic TAT was developed similar to that in [9] to model the SILC current under FN, MCT and VBT injection conditions. The +V_g SILC after +V_g stress can be described well under FN injection assuming a neutral trap density of N_{trap} = 6·10⁹ cm⁻² (Fig 12). For -V_g stress the SILC current at -V_g is caused by TAT of valence band electrons for E < 7 MV/cm (N_{trap} = 3.6·10¹⁰ cm⁻²), since gate depletion is reduced. For high oxide fields TAT of conduction band electrons is the dominant conduction mechanism with N_{trap} = 7.2·10¹⁰ cm⁻² (Fig 13). This increase of neutral traps (10×) for -V_g stress is most likely due to the higher oxide field at -V_g during stress using the same stress current (CCS). This is confirmed by Fig 14 and 15 where the SILC characteristics are measured for +V_g and -V_g after opposite stress polarity conditions. For +V_g an increase of SILC is observed (10×), while at -V_g SILC is significantly reduced. The reduced SILC for poly-SiGe could be a result of reduced boron incorporation in the gate oxide or a lower oxide field at the same stress current (CCS). TDDb data of ultra-thin gate oxides with p⁺ gates are shown in Fig 16 for 4.8 nm gate oxides under constant voltage stress (CVS) conditions of V_g = -6.5 V. An increase of TDDb with increasing RTA temperature is observed, due to a decrease of tunneling current during stress at a fixed gate voltage. This shows that CVS is also preferable for p⁺ gate devices. In summary, a new accurate model based on MCT from the gate is proposed for the I-V and SILC characteristics at -V_g for p⁺ gate devices. The difference in tunneling mechanism (+V_g: FN versus -V_g: MCT) strongly influences the gate oxide integrity for p⁺ gate devices.

Fig 1: J-E measurements of unstressed poly-Si and poly-SiGe gate MOS capacitors. Dashed line poly-SiGe, solid line poly-Si

Fig 2: Schematic representation of the three possible tunneling mechanisms for p⁺ gate devices

Fig 3: J-E characteristics of p⁺ poly-Si gate devices on 4.8 nm gate oxide. The RTA temperature is varied from 1010°C to 1070°C.

Tunneling parameters

$$J_a = \frac{n_s m_s k T}{2\pi^2 \hbar^3} \int_0^\infty T_{\text{tunnel}}(\phi_b - E, x, E_a) \cdot \ln \left[1 + \exp \left(\frac{E_f - E}{kT} \right) \right] dE$$

$$\text{MCT: } E_f = E_s + qV_{\text{poly}}; \phi_b = 3.1 \text{ eV}$$

$$\text{VBT: } E_f = 0, E \rightarrow -E; \phi_b = 4.2 \text{ eV (Si), } 3.98 \text{ eV (SiGe)}$$

SILC parameters:

$$J_{\text{in}} = \sigma (1-f) N_{\text{ot}} J_a(\phi_b, \phi_{\text{trap}}, E_{\text{ox}})$$

$$J_{\text{out}} = \sigma f N_{\text{ot}} J_a(\phi_{\text{trap}} + E_{\text{relax}}, \phi_{\text{anode}}, E_f = 0, E_{\text{ox}})$$

$$J_{\text{SILC}} = J_{\text{in}} = J_{\text{out}}$$

Table 1: Simulation parameters used to model conduction and SILC current in p⁺ gate devices.

Fig 4: Modelled and measured J-E characteristics for p⁺ poly-Si gate devices on 5.6 nm gate oxides.

Fig 5: Modelled and measured J-E characteristics for p⁺ poly-SiGe gate devices on 5.6 nm gate oxides.

Fig 6: High frequency C-V characteristics (gated-diode) of p⁺ poly-Si gate devices on 4.8 nm gate oxide. The RTA temperature is varied from 1010°C to 1070°C.

Fig 7: Carrier separation measurements on p⁺ gate devices with 3.1 nm oxide thickness. A large increase of hole current is observed with increasing electrical stress.

Fig 8: Measured J-E curves before and after stress (100 μC/cm² to 1 C/cm²) for p⁺ poly-Si gate material on 5.6 nm gate oxide thickness.

Fig 9: Measured J-E curves before and after stress (100 μC/cm² to 1 C/cm²) for p⁺ poly-SiGe gate material on 5.6 nm gate oxide thickness.

Fig 10 : Gate and source/drain currents of PMOSFETs on 4.8 nm gate oxides before and after MCT stressing.

Fig 11: Measured quantum yield of p^+ gate devices before and after MCT stressing. An energy loss of 1.0-1.5 eV is clearly observed.

Fig 12: Modelled and measured SILC at $+V_g$ for p^+ poly-Si gate devices on 5.6 nm gate oxide thickness (see Fig 8).

Fig 13: Modelled and measured SILC at $-V_g$ for p^+ poly-Si gate devices on 5.6 nm gate oxide thickness (see Fig 8).

Fig 14: Measured J-E curves before and after stress for p^+ poly-Si gate material on 5.6 nm gate oxide thickness. Stressing takes place under opposite gate bias polarity.

Fig 15: Measured J-E curves before and after stress for p^+ poly-SiGe gate material on 5.6 nm gate oxide thickness. Stressing takes place under opposite gate bias polarity.

Fig 16: TDDDB measurements on p^+ poly-Si gates on 4.8 nm gate oxides at $V_g = -6.5$ V. The RTA temperature is 990°C and 1070°C.

3. References

- [1] D. J. Maria et al., *Apl. Phys. Lett.* Vol 74 1999 pp 1752
- [2] J. De Blauwe et al., *IEDM Tech. Digest*, 1996 pp 343
- [3] J. H. Stathis et al., *IEDM Tech. Digest*, 1998 pp 167
- [4] C. Salm et al., *Electron Dev. Lett.* Vol 19 1998 pp 213
- [5] Y. Shi et al., *Electron Dev. Lett.* Vol 19 1998 pp 391
- [6] V.E. Houtsma et al., to appear in *Electron Dev. Lett.* July 1999
- [7] V.E. Houtsma et al., to appear in *Microelec. Eng. (INFOS99)*
- [8] J. -L. Ogier et al., *Proc. ESSDERC96*, 1996 pp763
- [9] S. Takagi et al., *IEDM Tech. Digest*, 1996 pp323
- [10] K. Schuegraf et al., *Int. Rel. Phys. Sym. Proc.* 93, 1993 pp7
- [11] D. J. Dimaria et al., *J. Appl. Phys.* Vol78 1995 pp 3883