A High- T_c 4-bit Periodic Threshold Analog-to-Digital Converter

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Abstract— Using ramp-type Josephson junctions a 4-bit periodic threshold ADC has been designed, fabricated and tested. Practical design constraints will be discussed in terms of noise immunity, flux flow, available technology, switching speed etc. In a period of four years we fabricated about 100 chips in order to bring the technology to an acceptable level and to test various designs and circuit layouts. This resulted in a basic comparator that is rather insensitive to the stray field generated by the analog input signal or variations in mask alignment during fabrication. The input signal is fed into the comparators using a resistive divider network. Full functionality at low frequencies has been demonstrated.

I. INTRODUCTION

In this contribution we will describe the development of an analog-to-digital converter (ADC) intended to operate at gigahertz frequencies. To do this in high- T_c technology is not an easy feat and a major effort was required to arrive at a state where circuits consisting of 10-20 junctions and several passive elements could be made with some yield. Before we will go into more detail concerning the circuit design, layout and fabrication technology some important circuit parameter requirements will shortly be discussed in section II. In section III we will describe the basic technology to fabricate junctions as well as other circuit elements and wiring. Section IV is devoted to the junctions, their properties and ways to improve them. This is followed by the design, layout, fabrication and testing of the basic comparator in section V. There we also discuss weaknesses in the design and technology. Section VI is devoted to an improved design of the basic comparator and a description of the 4-bit flash-type ADC and some test results. The article will be concluded with section VII where we discuss the prospects of HTS digital applications at gigahertz frequencies.

II. PARAMETER REQUIREMENTS

At present there are no real thin film tunnel junctions available in HTS technology. By real we mean that both Cooper pairs as well as quasiparticles tunnel directly from one electrode to the other. This results in the absence of a quasiparticle branch in the current-voltage characteristics (IVC) having a steep slope at some gap voltage and a low leakage current below it. Consequently the junctions are basically non-latching although some hysteresis may be present that can be deliberately used in circuit design. Therefore single flux quantum (SFQ) logic [1] or series array interferometer logic has to be applied [2]. Here we will focus on the use of SFQ logic as this is also of necessity if we want the circuits to operate at high temperatures and high speeds and nevertheless keep the dissipation low [3].

For circuits having only a few devices dissipation is not a matter of great concern, but in order to compete with semiconductor circuits, high speed is of prime importance.

We will discuss the junction parameter requirements in the light of thermal noise immunity, prevention of flux flow, switching speed, SFQ operation, circuit complexity and chip yield.

Thermal noise immunity is a matter of great concern and requires a junction technology with very high critical current densities. For example, basic Nb/AlOx technology for circuits to operate at 4 K employs junctions with $J_c \approx 1 \text{ kA/cm}^2$. In order for an HTS circuit to operate at 40 K with the same noise immunity a ten fold increase in J_c is needed. To fabricate such junctions without shorts in a reliable and reproducible way is not an easy feat. Furthermore, it also poses restrictions on the junction size, especially because all useful junctions so far are more or less one dimensional in nature. If the junction width is too small the critical current will be too low, resulting in a Josephson coupling energy not much larger than the thermal energy and, hence, the device will be noisy. If it is too large the size of the Josephson vortex will be too small compared to the junction width and it will start to flux flow. The latter probably leads to undesired switching characteristics and basic superconductive electronics modelling tools cannot be used. Further details of this discussion can be found in [4]. A critical current in the range 25-100 μA is considered to be sufficient at 40 K for small scale circuits.

The switching speed is not of great concern. Given an $I_c R_n$ product of 1 mV the SFQ pulse width is about 2 ps, which is fast enough for most applications. Given an I_c of 50 μA this leads to a junction normal state resistance R_n of 20 Ω . For wider junctions R_n , of course, reduces but in any case it is not too far removed from the transmission line impedance of 50 Ω that is used in the microwave community.

For SFQ operation the normalized loop inductance β_L should be around 0.5 and hence $L = 159/I_c$ pH where I_c has been expressed in μA . For $I_c = 50 \mu\text{A}$ this leads to a value for L of about 3 pH. Using an order of magnitude formula for inductance's this in turn leads to a linear dimension of about 2 μm . If inductors have to be fabricated with an error margin of 10% this puts a heavy burden on the lithography and subsequent structuring. However, by using ground planes these difficulties can be avoided. Therefore we decided to use microstrip line inductors where accuracy was needed. For an 11 μm wide line running at 100 nm over a groundplane the inductance is 0.07 pH/ μm . Furthermore one has to make sure that the kinetic inductance of the line is either negligible or has been taken care of.

Finally we will address circuit complexity and operating margins in relation to chip yield. For the RSFQ logic family Hamilton and Gilbert [5] made an extensive analysis

how to optimize the design of 6 basic circuits, i.e. JTL, AND, OR, XOR, NOT and splitter with respect to their critical margins. Such an optimization may lead to a doubling of the margins and hence is quite important. The weakest spot is the XOR circuit and for a $1\text{-}\sigma$ parameter spread of 25%, a value not uncommon for an HTS technology, the yield is only 10%. In general a $1\text{-}\sigma$ parameter spread of one-fourth of the critical margin is required to obtain a yield close to 100%. At present there are hardly any reliable data on the $1\text{-}\sigma$ parameter spread of the various HTS technologies, but even if we use the value of 12% that Miller et al. [6] mention as the near term goal, then a circuit of 15 junctions has only a 50% yield. However, even small improvements in the technology are rewarded. Reducing the $1\text{-}\sigma$ parameter spread to 10% leads to a circuit with 100 junctions with a 50% yield. As critical margins improve with $I_c R_n$ product [6] it is worthwhile to put effort in obtaining higher values, as we have done. There are, however, also other factors that influence the circuit yield, like occurrence of shorts, grains that reduce J_c etc. that are not taken into account in yield calculations.

III. RAMP-TYPE TECHNOLOGY

Since the discovery of high temperature superconductive (HTS) materials rapid progress has been made with the growth of multilayer thin films using a variety of deposition techniques. In our group we employ rf-magnetron sputtering as well as pulsed laser deposition and as HTS the work horse material $\text{YBa}_2\text{Cu}_3\text{O}_y$ (YBCO) or one of its close relatives from the 123 cuprate family like DyBCO. For the insulating layers we used PrBCO, or its Ga-doped variant $\text{PrBa}_2\text{Cu}_{3-x}\text{Ga}_x\text{O}_y$ and materials like YSZ, SrTiO_3 , CeO_2 , NdGaO_3 or sometimes even combinations of them. Furthermore, substrates like MgO, LaAlO_3 , NdGaO_3 , YSZ, SrTiO_3 , and sapphire are used. As barrier materials we rely on PrBCO or its Ga-doped variant with various amounts of doping, i.e. $x = 0.05, 0.1$ and 0.4 .

Given the high anisotropy of the commonly used HTS materials special techniques are required to make wire crossings. Sharp edges are not allowed as they induce grains with different orientation in subsequent film growth. As a result the current carrying capability of the top wire will be reduced substantially. Furthermore, in a multilayer technology film growth should be rather smooth, otherwise short circuits may easily occur, but also the growth of grains that reduce the J_c of top electrodes or wiring layers. To date a wide variety of deposition techniques are available that, at least in principle, are able to fulfil the basic requirement of smooth film growth.

For the development of the ADC mainly off-axis rf-magnetron sputtering from single stoichiometric targets of 5 cm diameter was used. Substrates were glued with Ag-paint to a stainless steel heater block and outgassed in ambient at 150°C . Thereafter the heater was brought into the sputter chamber via a load lock and outgassing was continued at deposition temperature until a background pressure of 1×10^{-6} mbar was reached. Sputtering was performed

using a 13.56 Mhz rf-power source operating at 90W. As sputtering gas we typically use from 10-20 Pa of an $\text{Ar}:\text{O}_2 = 1:1$ mixture to which a trace of water vapor ($\approx 0.1\%$) was added in order to increase the reactivity of the plasma. The latter has a profound influence on the stability of the sputtering process over the lifetime of the targets. However, water vapor cannot be used with all materials, an example being CeO_2 that tends to react. After 20 minutes of presputtering the substrate was brought into position by stepper motors, which also adds to the reproducibility of the process. Deposition rates were typically 70-90 nm/hr, depending on pressure and substrate position. Finally the samples were cooled down in about one hour to room temperature in 200 mbar of O_2 . Great care is needed to grow thin films of active device quality. As a rule of thumb for a 100 nm thick film surface roughness, as measured by an atomic force microscope (AFM), should be below 2 nm rms. This also influences the choice of substrate material so, for instance, LaAlO_3 , which is often used for passive device fabrication, could not be used. Due to its twinning and the way it is polished the surface has a terrace-like structure that may induce the growth of c-axis in-plane domains.

Once the basic growth processes are controlled well enough we are ready to perform the next step in the fabrication process, i.e. the etching of ramps that are needed for cross overs, Josephson junctions and via contacts. They are made using standard photolithography and a Kaufman Ar-ion beam etching gun. Typically the ion beam is incident at an angle of 45° with the sample surface resulting in ramp angles of $18\text{-}22^\circ$ using a beam voltage of 500V and current of 10 mA. The etch rate for RBCO is about 0.6 nm/sec and for SrTiO_3 0.4 nm/sec. Due to the fact that the resist etches faster than the layers two opposing ramps may be etched simultaneously although they are slightly different. By rotating the substrate over 180° in plane between ion pulses both ramps may even be made symmetrical. Next the resist is stripped by ultrasonic stirring in acetone and rinsing in isopropanol. Then the substrates are again glued to the heater block and re-entered in the etching chamber. This chamber is connected to the sputtering chamber via a load lock system. In order to promote epitaxial growth of subsequent layers, both on the ramps as well as on layers that have been covered by resist, we remove some 20 nm of material by ion beam etching. Using subsequently lower etching voltages surface damage on ramps may be minimized. This was evidenced from the measurement of the J_c 's of ramp contacts. Starting with a reduction of one to two orders of magnitude with respect to a virgin thin film, it turned out that contacts with a J_c reduction of less than 2 could be obtained. Inspection with HRTEM does not show any indication of remaining damage. Immediately after this cleaning procedure the sample is brought back into the sputtering chamber in order to grow subsequent layers. In the case of a ramp contact this is a top superconducting electrode, for a cross over it is an insulator like PrBCO, SrTiO_3 or CeO_2 followed by the top

electrode and for a Josephson junction it is a thin PrBCO tunneling barrier followed by a top electrode.

Finally the circuit is given its shape using a resist stencil followed by ion beam etching and a metallization step using a lift-off dc-sputtering process with a 8 nm Ti adhesion layer and a 100 nm Au layer. Electrical contacts are made by ultrasonic bonding of 25 μm Al-wire on the metallized pads.

Not all substrates can be used equally well with this ramp-type technology. Both MgO [7] as well as YSZ [8] support only graphoepitaxy, i.e. the c-axis of RBCO is always pointing perpendicular to the local surface rather than joining the direction of the substrate lattice. In the latter case this is caused by the formation of a BaZrO₃ interface layer. As a result of this graphoepitaxy grains with different c-axis orientation may occur leading to reduced J_c 's of top electrodes and even Josephson junctions may be formed in that way. The latter results in an IVC showing several switching steps. Again this reduced the number of substrates that can be used to fabricate complex electronic circuits. So far only SrTiO₃ and NdGaO₃ remained from the list that we started with, where the best results from the point of view of reproducibility were obtained with the former. This is however also a matter of effort that has been put into it. Probably due to its tendency to support a-axis oriented growth or Ga-diffusion to the interface, films on NdGaO₃ are usually rougher, but careful optimization of growth conditions and the use of a buffer layer like CeO₂ may overcome this problem. From the microwave point of view SrTiO₃ is, of course, a terrible substrate although by using a ground plane its influence may be made to vanish at the penalty of increased complexity. However, this complexity is not different from that of logic circuits in Nb/Alox technology.

IV. RAMP-TYPE JUNCTIONS

To date a great variety of junction types has been presented in literature. However, systematic data are usually lacking especially if reproducibility comes into play. As we do not intend to give an overview we will restrict the discussion mainly to the ramp-type junctions made in our group. The main problem we encountered at the start of the ADC project in June 1992 was film roughness giving rise to shorts in microstrip lines, excess currents in junctions and a large parameter spread. By carefully optimizing the growth conditions of the RBCO layers, thereby reducing their a-axis oriented content to a minimum, these problems could be greatly reduced. The junctions with a 10 nm thick PrBCO barrier (thickness is nominally as inferred from sputter time and along the c-axis, which in turn is perpendicular to the substrate) exhibited a J_c of $10^3 - 10^4$ A/cm² at 40 K. This can be seen in Fig. 1 where the critical current density is plotted as a function of the nominal barrier thickness for two temperatures and two doping levels. It is also clear that Ga-doping has no effect on J_c , this also holds for doping levels not shown in the figure. However, the normal state resistance R_n increases with doping. These facts combined

Fig. 1. The critical current density J_c plotted as a function of the nominal barrier thickness d for two temperatures and two Ga-doping levels x .

lead to an increase in $I_c R_n$ product to 10 mV at 4 K and 1 mV at 40 K with $x=0.4$.

Another way to increase the critical current density and the $I_c R_n$ product is a further reduction in barrier thickness d . Due to the anisotropy in the growth of the barrier material this may lead to the formation of pinholes and an increase in parameter spread. More work will be required to find a way out. For further details the reader is referred to [9].

The 1- σ parameter spread that we estimate for a large number of junctions with varying barrier thicknesses and including junctions with Ga-doped PrBCO barriers is about 20%. This includes run-to-run variation in deposition conditions, variation in layer thickness over an area of 5 mm x 6 mm (we use 10 mm x 10 mm substrates), the use of several different substrate materials etc.

Returning to the properties of the ramp-type junctions that are presently available one might ask if their dynamics can indeed be described by the RSCJ-model. As far as we can tell from data in literature that appears indeed to be the case for the IVC's of good HTS junctions including noise rounding effects. Data from our own junctions have been published in [10]-[12]. Furthermore we estimate that about 75% of our junctions with a barrier thickness > 10 nm are quite homogeneous and show a nice Fraunhofer-like pattern if we measure I_c as a function of an applied magnetic field. However, there is some sensitivity to flux trapping as was observed using a low temperature scanning electron microscope in Tübingen [13].

V. DESIGN, LAYOUT AND TESTING OF THE BASIC COMPARATOR

After a literature survey we decided to base the design of the comparator of the ADC on the quasi-one junction SQUID (QOS) first proposed by Ko et al. [14]. It has the advantage of high input signal bandwidth, i.e. several GHz, in comparison with earlier designs. Our first design and implementation took place in the first half of 1992 [15]. The circuit was designed for an input signal bandwidth of about

1 GHz and checked by simulations using realistic parameters. However, due to microshorts between ground plane and microstrip inductor, the circuit could not be tested. After subsequent improvements in technology, we were able to demonstrate that the basic comparator could be made to work properly. Its layout is given in Fig. 2, where J_0 is

Fig. 2. Layout of the QOS comparator.

the quantizer junction, L the loop inductor, J_s the sense junction, C a capacitor to introduce hysteresis in the sense junction, I_a the input signal current. The bottom strip is used for the sample pulses I_p as well as the output voltage. Actual contact to the ground strip is made via a wide junction on one of the ramps. A typical threshold curve is given in Fig. 3.

Fig. 3. Measured threshold curve of the QOS comparator.

It is recorded by a home made measurement instrument that feeds adjustable sampling pulses into the junction J_s and senses the output voltage V_{out} . This is done by a sensitive amplifier and the sampling pulse height is adjusted in such a way that the junction barely switches. Hence, the sampling pulse height records the switching threshold. For more details concerning the design and testing of the basic comparator the reader is referred to [4]. Besides the basic comparator we also implemented a variant of Bradley [16] in which a third junction J'_s together with capacitor is introduced. This edge-triggered version is preferred because it gives a considerable reduction in effective aperture time of a multi-bit ADC.

In total we fabricated some 20 chips with these comparators in order to get some systematic data on reproducibility etc. In this way some weaknesses in the design and the fabrication process could be detected. As can be seen in Fig. 2 the top electrode of the quantizer junction is rather narrow and hence contributes significantly to the loop inductance. Slight variations in mask alignment thus have a marked influence on the loop inductance. As the precision of an ADC depends on the conversion from input current to flux in the loop, which is quantized, this variation is a thing to be reduced. Furthermore, for a multi-bit

converter, the current carrying capability of the top wiring should be several times the critical current density of the quantizer junction. The narrow top electrode of this junction is the limiting factor in the current carrying capability of the top wiring, especially because on the ramp current also has to flow in the c -axis direction. Stray fields from the loop inductor influence the critical current densities of the junctions in the comparator. This effect can be observed in the measured threshold curve in Fig. 3. Instead of being purely periodic two kinds of modulation are visible. The amplitude is modulated due to the influence of the stray field on the quantizer junction and the modulation of the dc level stems from the sense junction. Nevertheless, we carefully checked that the basic comparator is accurate enough for a 4-bit ADC and could be made with sufficient reproducibility in our laboratory setting.

VI. DESIGN AND TESTING OF A 4-BIT ADC

Notwithstanding the fact that the basic comparator we used, whether it is based on Ko's design or Bradley's design, was accurate enough and could be produced with sufficient reproducibility to be able to fabricate a few working 4-bit ADCs, we decided to make a major change in layout and in accompanying technology. Our objective was to reduce the influence of stray fields from the loop inductor and to crank up the current carrying capability of the top wiring. After considering several variants it was decided to go for the layout given in Fig. 4. As can be seen the input

Fig. 4. Improved layout of the QOS comparator.

current I_a no longer flows through the narrow top electrode of the quantizer junction J_0 . Furthermore the stray fields from the loop inductor L may now be shielded from the actual junction area by the top electrodes. However, the fabrication process is more complicated. In the first step we deposit a base electrode layer on a substrate. This is followed by a second step in which the base electrode is defined by a resist stencil and ramp etched. In the third step the sample is thoroughly cleaned including etching and annealing followed by an in situ deposition of an insulating layer. In the fourth step this insulating layer is structured leaving behind rectangular electrode islands with exposed ramps on two opposing sides and insulated ramps on the other sides. In the fifth step after cleaning and annealing the junction barriers are deposited immediately followed by the top electrode layer. The final structuring is performed

in the sixth step followed by the formation of contact pads for bonding.

Upon closer inspection of this layout the reader might ask why the leads connecting the pads with the circuit are not running above a ground plane. In that case the isolated ramps would not have been necessary and furthermore the whole circuit would have been separated from the substrate, so even SrTiO_3 could be used. Given the fact that presently the best results are obtained on this substrate, it would have been an obvious choice. The reason for this lies primarily in the quality of the insulating layer that we use. The longer the lines are, the higher the risk of short circuits to ground or the influence of resistive coupling between microstrip and groundplane. Presently with PrBCO or Ga-doped PrBCO we do not dare to take that risk, CeO_2 could not be used due to the water vapor in our sputtering process and SrTiO_3 which we could use from an insulating point of view is useless at high frequencies anyhow. More work needs to be done to come up with the right insulator or a change in deposition process in order to be able to use CeO_2 .

In order to arrive at an ADC, once the basic comparator is given, we also need to fabricate the input signal divider and the clock circuitry. Various alternatives have been considered, but already from the beginning of the project, knowing something about the technological hurdles that had to be taken, we were convinced that simplicity was required. Therefore, it was decided to use an external clock signal without additional junctions on the chip. Their reproducibility was our major concern at that time. Furthermore, it was decided to use a resistive input signal divider and direct coupling to the comparators as opposed to the use of inductors and transformers. It would have been nice if the resistive divider could be integrated with the HTS circuits, but after studying several alternatives it was decided to use commercially available SMD resistors. In our Nb/Alox technology Pd resistors are used, so we did have experience in thin film resistor fabrication, but we did not trust the required contact between a normal metal like Pd or Au etc. and YBCO. An alternative is the use of a metallic perovskite having the correct lattice parameters, or to use doped YBCO having a T_c below the operating temperature of the circuit. Lack of time and manpower prevented us from really pursuing this route.

For the final phase of the ADC project four sets of masks were made. One containing 13 QOS structures in order to test the latest technology, one for an ADC to be used with off-chip resistors, one with an ADC based on comparators according to Ko and one with an ADC based on Bradley-type comparators. In the latter room is also made for the extra resistors that are needed for edge-triggered sampling.

About 10 chips, each containing 4-8 comparators were prepared and tested. In the first two only a 100 nm thick PrBCO layer was used as insulator. However, the insulating properties turned out to be insufficient, probably due to some pinholes. Therefore we decided to use an additional very thin SrTiO_3 layer resulting in eight working

chips. A typical threshold curve recorded at 25 K is depicted in Fig. 5, where up to eight full periods can be observed. The period is constant over the whole dynamic

Fig. 5. Threshold curve of improved QOS comparator recorded at 25 K.

range, but slowly decreases for increasing temperature, as a result of the temperature dependence of the London penetration depth. Modulation was observed up to 70 K.

It is clear that in the new design the number of periods is more than sufficient for a 4-bit ADC (the maximum number of periods we observed was 30) and 8-bit converters can certainly be based on them. Several of the 4-bit ADC chips using Bradley's design were fully functional as we observed from low frequency (1 kHz) tests of all comparators on them. The precision of the inductors is adequate for a 4-bit converter without corrections.

VII. DISCUSSION

The 4-bit flash-type ADC that we designed, fabricated and tested is an interesting circuit to explore the limits of a given HTS technology and to formulate requirements for further development. Given the fact that the technology is still immature various trade-offs had to be made in design and subsequent fabrication. In section II we discussed parameter requirements for SFQ-type of circuit operation. From the noise point of view the technology should be able to produce Josephson junctions with $J_c = 10^4 \text{ A/cm}^2$ at an operating temperature of 40 K and preferably higher with increasing complexity or operating temperature. To make such junctions with a $1-\sigma$ parameter spread of 10% or less is not an easy feat. In the case of ramp-type junctions, besides the barrier material used, thickness variations primarily induced by the anisotropic growth are the limiting factor. Our present limit is about 10^4 A/cm^2 with a $1-\sigma$ parameter spread of about 20%, reducing J_c results in a smaller spread and vice versa. Accurate data on this relationship are not available, too many factors play a role, although we try to use protocols for each process step. However, junctions with 10^5 A/cm^2 are feasible but probably require a different, maybe cubic, barrier material. World-wide over ten different materials have been used even including a tri-layer barrier. As yet no clear favorite has turned up, but in our opinion an insulator is preferred in order to arrive at an acceptable $I_c R_n$ product. For the near future we will explore Ga-doped RBCO until something better will become available. This is not because we expect any improvement in J_c , but to explore if a direct tunnel junction can be made having a quasiparticle branch in its IVC that

is suitable for THz mixing. At the same time such hysteretic junctions could be useful in the readout of SFQ circuits. Furthermore, these junctions would have the highest possible $I_c R_n$ -product for a given HTS material. This not only improves critical operating margins of digital circuits and hence circuit yield, but it also facilitates interfacing to CMOS circuits. Less junctions are required to convert HTS signal levels to CMOS signal levels. A high $I_c R_n$ product will also lead to breathtaking speed of operation, 20 mV results in an SFQ pulsewidth of 0.1 ps and hence THz clock frequencies may be used.

The present state of the art for our technology allows for circuits with 10-20 junctions, several microstrip inductors and SMD resistors with a yield of about 20-30%. The comparators exhibit a high degree of linearity that we estimate to be at least two decades and input signal bandwidth of 1 GHz as designed and simulated. Our highest clock speed at the moment is about 5 MHz so we could not test this. Higher frequencies are possible by reducing the value for the normalized loop inductance β_L of the comparators at the cost of sensitivity and precision. This may be avoided at the cost of greater complexity [17],[18]. The degree of complexity that we achieved is sufficient to explore various alternatives and the basic SFQ family of logic circuits including a simple shift register and a signal level converter. Clock speeds are comparable to that of Nb/Alox technology, i.e. several hundred GHz. Presently missing in the technology are integrated resistors, long transmission wiring with groundplane, hysteretic junctions and a $1-\sigma$ parameter spread sufficient for LSI integration. More work is needed to explore the various solutions to these problems that are ultimately governed by material science issues. This holds for optimization of fabrication processes as well as materials choices as only a small fraction of available and potentially interesting materials have been investigated so far.

VIII. SUMMARY

In this contribution an overview has been presented of the efforts we undertook to fabricate an HTS 4-bit periodic threshold ADC. Ramp-type junction fabrication and multi-layer technology have been improved considerably, leading to an acceptable yield for circuits having 10-20 junctions. Circuit layout has been optimized in order to minimize parameter spread, reduce the influence of stray fields, and to maximize dynamic range.

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