A Low-Voltage Mobility-Based Frequency Reference for Crystal-Less ULP Radios

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***Abstract*—The design of a 100 kHz frequency reference based on the electron mobility in a MOS transistor is presented. The proposed low-voltage low-power circuit requires no off-chip components, making it suitable for application in wireless sensor networks (WSN). After a single-point calibration, the spread of its output frequency is less than 1.1% (3σ) over the temperature range from −22 °C to 85 °C. Fabricated in a baseline 65 nm CMOS technology, the frequency reference circuit occupies 0.11 mm^2 and draws 34 μA from a 1.2 V supply at room temperature.**

***Index Terms*—Charge carrier mobility, CMOS analog integrated circuits, crystal-less clock, low voltage, relaxation oscillators, ultra-low power, wireless sensor networks.**

I. Introduction

WIRELESS sensor networks (WSN) need radios that are small, cheap and energy efficient [1]. The largest fraction of the energy consumed in each node of a WSN is spent in idle listening to the channel, waiting for data packets [2]. Reduction of the energy wasted in idle listening is usually obtained by duty-cycling the network nodes, i.e., by putting them into a sleep mode for a significant fraction of the time. This task requires a synchronization algorithm to ensure that all nodes observe simultaneous sleep and wake-up times and, consequently, each node must be equipped with a time reference to enable such synchronization. A high accuracy time reference allows the receiver to accurately predict the timeslot used by the transmitter, and to employ, consequently, a lower duty-cycle. Frequency accuracies of a few ppm can be achieved by crystal-controlled oscillators (XCOs), but these are bulky external components. In order to realize miniature WSN nodes, accuracy must be traded for the sake of integration.

The tradeoff between integration and time/frequency accuracy is also present in the RF front-end. While commercial communication systems require high frequency accuracy, radios for WSN can be optimized to relax such specifications and so frequency accuracies of only a few percent are needed [2], [3]. Furthermore, the power available to the time reference is limited to tens of μW, since it is always on, and its supply voltage is limited to a few volts to be compliant with typical WSN energy sources, such as batteries and energy scavengers [4], [5].

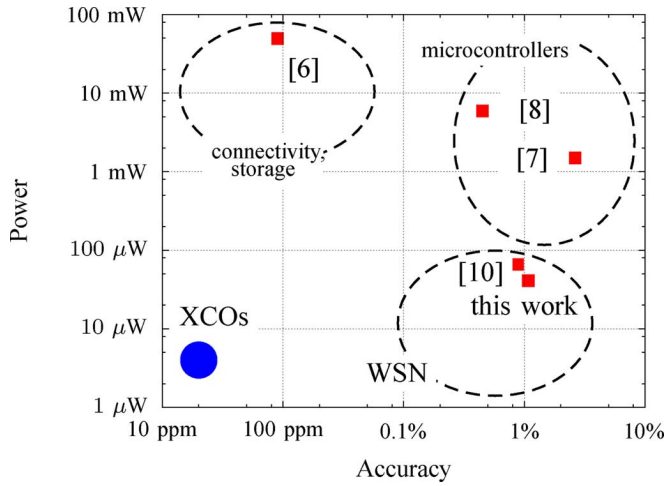

Fig. 1. Comparison among fully integrated oscillators that can replace XCOs in various applications; XCOs point is given as reference.

Recently, much work has been devoted to implementing fully integrated frequency references in standard microelectronic technologies. The current state-of-the-art is illustrated[1] in Fig. 1. *LC* oscillators [6] can provide accuracy and phase noise performances comparable to XCOs; however, their power consumption typically exceeds 100 μW due to the limited Q of integrated inductors and the possible need for high-speed frequency dividers. The accuracy of the compensated ring oscillator in [7] is high enough for WSN applications, but its power consumption is in the mW range. A very stable physical effect, i.e., the thermal diffusivity of bulk silicon, can be exploited for use in frequency references [8]; however, this requires the silicon substrate to be heated and thus requires the dissipation of a few mW. The performance of trimmed RC oscillators may also be suitable for use in WSN nodes [9], [10].

An alternative way of realizing an accurate fully integrated oscillator is by employing charge mobility as a reference [11]. Mobility is less sensitive to process variations than other parameters, such as polysilicon resistance or oxide capacitance, and its standard deviation is less than 2% at room temperature for the

Manuscript received November 30, 2008; revised March 10, 2009. Current version published June 24, 2009. This work was supported by the European Commission in the Marie Curie project TRANDSSAT–2005-020461.

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Digital Object Identifier 10.1109/JSSC.2009.2020247

[1]In this prototype chip, some non-critical circuits have been implemented off-chip. As such, Fig. 1 only reports the power dissipation of the on-chip circuitry.

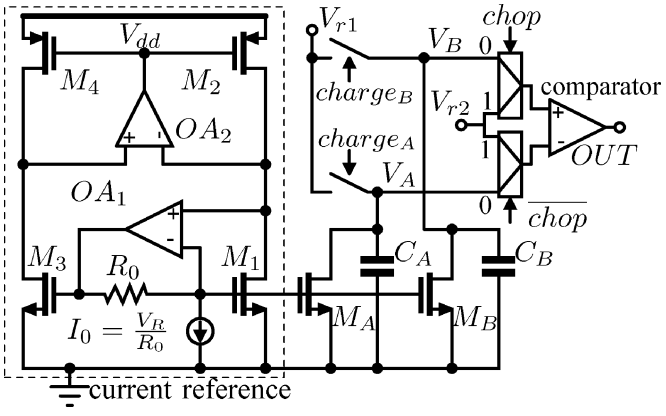

Fig. 2. Mobility-referenced oscillator.

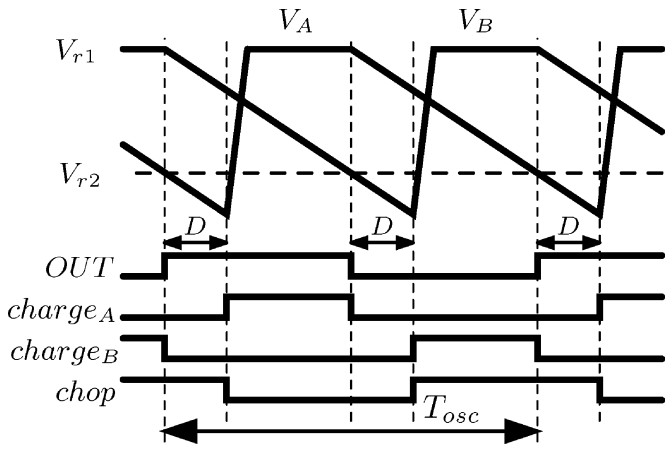

Fig. 3. Oscillator waveforms.

adopted process. Although the temperature dependence of the mobility is large (approximately $T^{-1.5}$), it is well defined and can be compensated for. The effect of process spread can then be removed by a single room-temperature trim.

This paper describes a fully integrated oscillator referenced to the electron mobility, and which is suitable for WSN applications [12]. The oscillator is based on a current-controlled relaxation oscillator, in which the current is proportional to the mobility. Experimental validation of this approach is provided, resulting in a frequency spread of less than 1.1% after a one-point calibration and dissipating only 41 μW. The circuit is presented in Section II, experimental results are shown in Section III, temperature compensation strategies are discussed in Section IV, and conclusions are given in Section V.

II. Circuit Description

A. Oscillator Structure

A simplified schematic of the oscillator is shown in Fig. 2. It consists of a current reference, two current mirrors M_1–M_A and M_1–M_B, two capacitors C_A and C_B and a comparator. The drain current of M_1 is mirrored by M_A and M_B with a gain of four and, as explained in the next section, is given by

$$I_1 = \frac{I_A}{4} = \frac{I_B}{4} = \frac{\mu_n C_{\rm ox}}{2}\frac{W_1}{L_1}kV_R^2 \tag{1}$$

where μ_n is the electron mobility, $C_{\rm ox}$ is the gate capacitance per unit area, k is a constant determined by the ratios of the dimensions of matched transistors and V_R is a reference voltage. In the previous equation and in the rest of the paper, the symbols I_x, W_x and L_x are used for the drain current, width and length, respectively, of transistor M_x. As shown in the timing diagram in Fig. 3, C_A and C_B are alternatively precharged to V_{r1} and then linearly discharged by M_A and M_B. When the voltage on the discharging capacitor drops below V_{r2}, the output of the comparator switches and the linear discharge of the other capacitor starts immediately, while the recharge is delayed by D. The delay D ensures that non-idealities of the comparator do not affect the slope of the discharge at the crossing of V_{r2} and it is not critical, as it does not influence the period $T_{\rm osc}$. The delay D and the signals driving the switches are generated by a digital circuit not shown in Fig. 2.

By inspecting Figs. 2 and 3, the period and frequency of oscillation can be easily determined, and from (1):

$$T_{\rm osc} = \frac{2C}{I_A}(V_{r1} - V_{r2}) \Rightarrow f = \frac{1}{T_{\rm osc}} = \mu_n k \frac{C_{\rm ox}\frac{W_1}{L_1}}{C}\frac{V_R^2}{V_{r1} - V_{r2}} \tag{2}$$

where $C = C_A = C_B$. C_A and C_B are MOS capacitors operating in inversion, in order to obtain a ratio $C_{\rm ox}(W_1/L_1)/C$ which is independent of the effect of temperature and process variations on $C_{\rm ox}$. If the reference voltages V_{r1} and V_{r2} are obtained from a bandgap reference, the residual frequency variations will be due to the spread[2] and temperature dependence of the mobility and of the voltage V_R. The latter can be used as a control voltage to compensate for the effects of temperature variations and process spread, or it can be derived from a voltage reference like V_{r1} and V_{r2}. Further details on the use of V_R to compensate for temperature variations are given in Section IV.

The two multiplexers at the input of the comparator are driven by the signal *chop*, shown in Fig. 3, to mitigate the effect of comparator offset. Thus, with an offset V_{os} at the comparator input, the output is switched when $V_A = V_{r2} - V_{os}$ or $V_B = V_{r2} + V_{os}$ and the total error in the period is given by

$$\frac{\Delta t}{T_{\rm osc}} \cong \frac{V_{os}}{2(V_{r1} - V_{r2})}\left(\frac{\Delta C}{C} - \frac{\Delta I}{I_A}\right) \tag{3}$$

where $\Delta C = C_A - C_B$ and $\Delta I = I_A - I_B$. Hence, if the capacitors and current mirrors are well matched, the resulting error is small. Since the oscillator is intended to operate at relatively low frequencies, good matching can be obtained by increasing device area without significantly affecting oscillator's performances.

B. Current Reference

The operation of the circuit in the dashed box in Fig. 2 can be understood by noting that M_2, M_4 and OA_2 constitute a

[2]Geometric factors in (2) (W_1, L_1 and the area of capacitors C_A and C_B) are also affected by process spread. However, their effect on $T_{\rm osc}$ can be neglected if sufficiently large devices are employed.

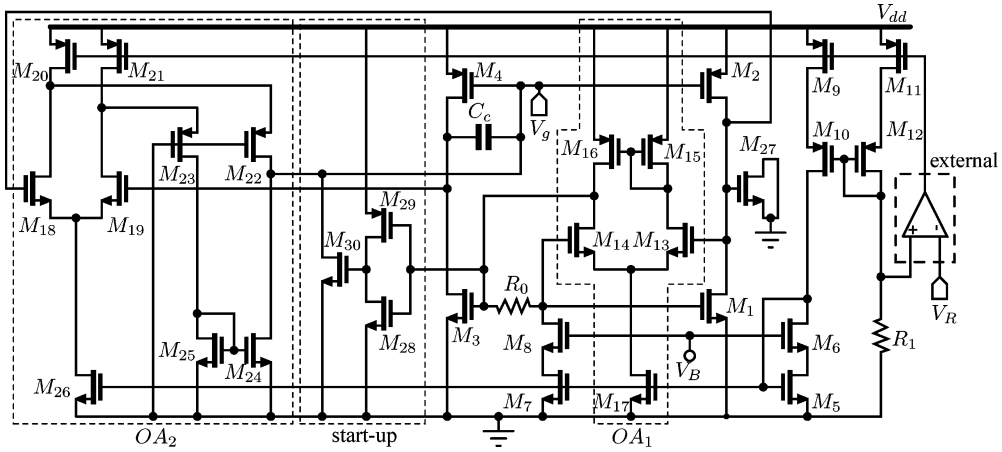

Fig. 4. Complete schematic of the current reference.

low-voltage current mirror and that M_1 is effectively diode-connected through OA_1 and R. Using the square-law MOS model, it is possible to derive [13]

$$I_1 = \frac{\mu_n C_{\rm ox}}{2}\frac{W_1}{L_1}\frac{V_R^2}{\left(\sqrt{\frac{n}{m}}-1\right)^2} \tag{4}$$

where $n = (W_4/L_4)/(W_2/L_2)$ and $m = (W_3/L_3)/(W_1/L_1)$ and, with reference to (1), $k = \left(\sqrt{n/m}-1\right)^{-2}$. Equation (4) is valid under the assumption that M_1 and M_3 are biased in strong inversion. It is also preferable to bias M_2 and M_4 in strong inversion in order to reduce the error due to mismatch in the current mirror gain n. The addition of OA_1 and OA_2 to the basic structure constituted by M_1–M_4 increases the power consumption but at the same time reduces the requirement on voltage headroom (avoiding for example the diode-connection of M_4) and consequently reduces the minimum required voltage supply. Moreover, OA_2 increases the output impedance seen at the drain of M_4, which mitigates the effect of voltage supply variation on the current reference output and hence the output frequency.

The complete schematic of the current reference is shown in Fig. 4. The current source I_0 is implemented by the unity-gain cascode current mirror M_5–M_8. The value of I_0 is fixed by the current mirror M_9–M_{12} and by the external opamp,[3] which forces a voltage drop V_R on R_1, so that $R_0 I_0 = R_0/R_1(W_9/L_9)/(W_{11}/L_{11})(W_7/L_7)/(W_5/L_5)V_R = V_R$. Resistance values ($R_0 = 200\ \text{k}\Omega$, $R_1 = 20\ \text{k}\Omega$) are chosen as a tradeoff between resistor area, current consumption and the contribution of the parasitic currents through R_1.[4]

The start-up circuit and the implementation of the opamps are shown in the dashed boxes in the figure. A folded cascode structure is adopted for OA_2 to reduce its systematic input offset. Since OA_1 must provide an output quiescent current I_0, it is biased with $I_{17} = I_0/2$ and it is dimensioned such that $W_{13}/L_{13} = W_{14}/L_{14}$ and $5W_{15}/L_{15} = W_{16}/L_{16}$. Both input pairs, M_{13}–M_{14} and M_{18}–M_{19}, are biased in weak inversion to allow the input common mode of the opamps to be equal to V_{GS1}.

The stability of the whole circuit can be guaranteed by ensuring the stability of the two negative feedback loops, i.e., the one constituted by OA_1 and M_1 and the one constituted by OA_2 and M_4, and of the positive feedback loop formed by M_1, M_2 and the low-voltage current mirror. The first negative feedback loop can be modelled as the cascade of OA_1 in buffer configuration through R_0 and the common-source amplifier M_1. The bandwidth of OA_1 is much larger than the frequency of the pole associated to the output impedance of M_1, since OA_1 is biased with a larger current (with reference to Fig. 2, $I_0 = 1\ \mu$A and $I_1 = 125$ nA in the nominal case as it will be shown in Section III) and MOS capacitor M_{27} is added at the drain of M_1. Miller compensation is used for the second loop, employing capacitor C_c across M_4. A fringe metal capacitor is needed to implement C_c because the voltage headroom available between gate and drain of M_4 is not enough to bias a MOS capacitor. Assuming that the DC open-loop gain of the two negative loops is high enough, the open-loop gain of the positive feedback loop $A_{\rm loop}(f)$ at DC can be approximated as

$$A_{\rm loop}(0) \approx \frac{1}{n}\frac{g_{m3}}{g_{m1}} = \frac{1}{n}\sqrt{\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}}\sqrt{\frac{I_3}{I_1}} = \sqrt{\frac{m}{n}} \tag{5}$$

where g_{m1} and g_{m3} are respectively the transconductance of M_1 and M_3 in Fig. 4. The loop is stable under the condition that $A_{\rm loop}(0) < 1$ and that $A_{\rm loop}(f)$ is monotonically decreasing, i.e., no peaking occurs in the frequency response of the loop. Since the negative feedback loops interact with the M_1–M_4 loop, their phase margin should be large enough not only to ensure stability of the respective loops but also to prevent such peaking. In the presented circuit, the phase margins of the two loops were designed to be larger than 45° in the worst case (process corners and temperature).

To avoid coupling digital noise to the gate of M_1 via the output mirrors M_1–$M_{A,B}$ of Fig. 2, the current is mirrored to M_A and M_B using the node V_G and additional pMOS and nMOS mirrors (not shown in Fig. 4).

[3]An external opamp (LTC1053) is used only for testing purpose.

[4]Note that a pad with large ESD protection diodes and an external opamp are connected to one end of R_1. The parasitic current through R_1 is the sum of the leakage currents of the ESD diodes and of the input bias current of the opamp.

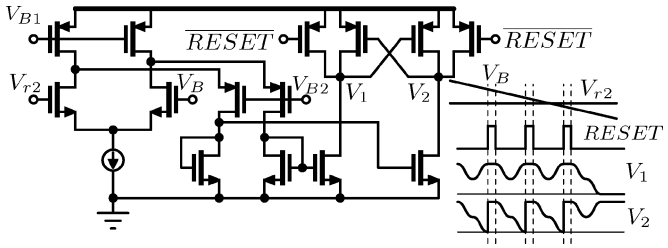

Fig. 5. Simplified schematic of autolatch comparator for $chop = 0$.

C. Comparator

The delay of the comparator must be negligible with respect to the oscillation period T. This requires high gain and large bandwidth in the case of an open-loop topology, or a very small hysteresis in the case of a Schmitt trigger implementation. To overcome this problem, within the constraints of a very tight power budget, a comparator with novel architecture, called an *autolatch comparator*, was introduced. Its schematic is shown in Fig. 5 for the case when $chop = 0$ together with some waveforms. The core of the circuit is a dynamic latch. When a comparison is needed, a digital circuit resets the latch and then enables it. As long as V_B has not crossed V_{r2}, V_1 goes periodically to V_{dd} and V_2 to ground. The signal on V_2 is inverted and delayed through a chain of inverter gates to generate the *RESET* signal. V_1 and V_2 are then pulled up to V_{dd} and, after a delay, *RESET* goes low. This cycle is repeated until V_B crosses V_{r2} and V_1 goes low. In this case the output is represented by the voltage on V_1. When $chop = 1$, the logic takes care of generating *RESET* from the appropriate node and chooses the right output node. The latch is preceded by a folded preamplifier to prevent kickback noise appearing on oscillator's capacitors.

The delay of the comparator can be adjusted by controlling the period of the described cycle. Simulations show that the delay is less than 13 ns in the worst case (process and temperature) with a total average current of 30 μA at 1.2 V supply. Low power is achieved by keeping the devices small, so as to minimize their parasitic capacitance. Small devices have high flicker noise, but the offset compensation technique described in Section II-A also reduces the effect of flicker noise.

III. Experimental Results

The oscillator has been realized in a baseline TSMC 65 nm CMOS process. The circuit occupies 0.11 mm^2 and uses only 2.5 V I/O thick oxide MOS devices. The 1.2 V thin oxide devices were avoided because of their high gate leakage current, which is significant in this circuit and which represents a significant fraction of the drain current for very long devices [14]. Most of the area of the circuit is occupied by the current reference and by the oscillator's capacitors[5] (Fig. 6). The layout of the current reference has been optimized for transistor matching; particular care has been devoted to reduce systematic mismatch due to topography related errors [15] and to reduce mechanical strain associated with metal chemical mechanical polishing (CMP) dummy structures [16], [17]. To deal with the first effect, asymmetries in the surroundings of matched transistor arrays are located more than 10 μm away from the active devices. This precaution significantly increased the area of the current reference and was adopted to minimize additional sources of inaccuracy in this test chip; a substantial fraction of this area can probably be saved in a future redesign. In cases where dummy metal structures *had* to be included above arrays of matched transistors (to satisfy metal-density rules), such structures were manually drawn to minimize the mismatch due to the additional stress. For flexibility in testing, all the reference voltages (V_{r1}, V_{r2} and V_R) were provided externally. For a nominal oscillation frequency of approximately 100 kHz, the reference current is $I_1 = 125$ nA for $C \cong 6$ pF, $V_R = 0.2$ V, $V_{\rm ref1} = 1$ V and $V_{\rm ref2} = 0.6$ V. A low frequency was chosen to reduce the impact of parasitic effects, such as comparator delay. The total current consumption with 1.2 V supply voltage is 34.3 μA (18.9 μA for comparator and logic; 14.4 μA for current reference; 1 μA through pin V_{r1}). Note that to minimize the effect of ESD pad leakage and opamp bias current (about 1 nA worst-case), the current in R_1 is relatively large (10 μA). If the reference voltage V_R were integrated on chip, this current would be negligible. The current consumption can also be strongly reduced by using a less accurate, or perhaps a duty-cycled, comparator. Since the aim of this chip was to investigate the feasibility of the proposed concept, it was optimized for accuracy rather than for low current consumption. In a fully integrated version, the reduced current through R_1 will compensate, at least partially, for the extra current required by the voltage reference and the temperature compensation circuitry [18], [19].

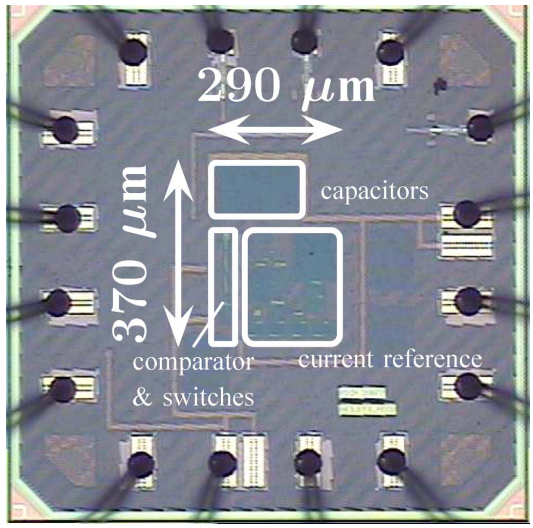

Fig. 6. Die micrograph of the test chip.

Long-term jitter measurements for an output frequency of 100 kHz are reported in Fig. 7, together with lines showing the extrapolated thermal and flicker noise components. Period jitter is 52 ns (rms) and is dominated by comparator thermal noise. After a large number of periods, jitter is dominated by flicker noise from the current reference. Relative jitter is defined as the standard deviation of jitter divided by elapsed time; its value for a time period of the order of one second is an important parameter for time references used in WSN, since it limits

[5]The area labelled as "capacitors" in Fig. 6 also contains also transistors M_1 and M_3 of the current reference, which are required to match MOS capacitors C_A and C_B.

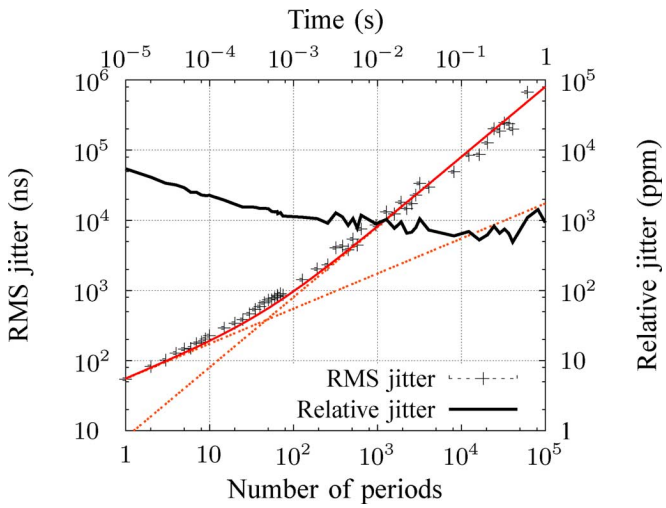

Fig. 7. Measured long-term jitter versus time; extrapolated thermal and flicker noise components and their cumulative contribution are also plotted.

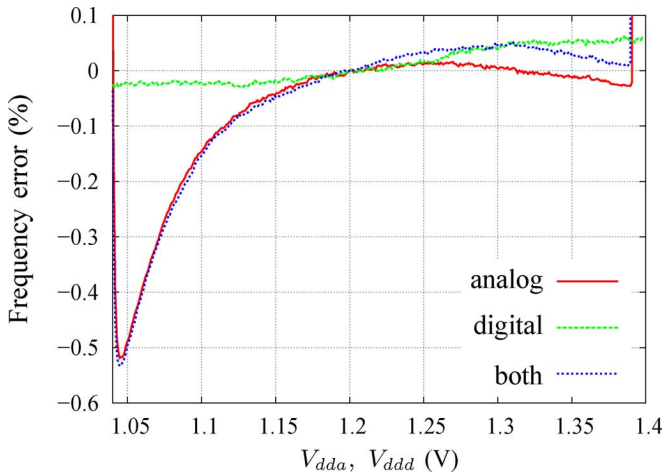

Fig. 8. Frequency error versus variations of analog supply (V_{dda}), digital supply (V_{ddd}) or both.

duty-cycle of the receiver when synchronization is performed over a time scale of seconds [2]. It can be proven that for most oscillators, relative jitter becomes flat for increasing time, as observed in the measurements [20]. The relative jitter is 0.1% after one second and is negligible compared to the temperature-induced frequency drift.

Frequency pushing is shown in Fig. 8. The nominal supply voltage of the circuit should be 2.5 V (with pMOS and nMOS threshold voltages of 0.63 V and 0.57 V, respectively) but the chosen topologies of the current reference and comparator allow functionality down to 1.05 V. The upper bound of the supply voltage is limited to 1.39 V by the start-up circuit in the current reference. With reference to Fig. 8, V_{dda} supplies the current reference, while V_{ddd} supplies the logic and the comparator. The increase of frequency with V_{ddd} is due to a decrease in the delay of the comparator, which is related to the period of *RESET* in Fig. 5 and is fixed by logic circuitry. The supply voltage of the comparator can be increased up to 1.5 V (not shown in Fig. 8) without affecting its functionality and it can be adjusted to shift the input common-mode range of the comparator. Fig. 8 shows

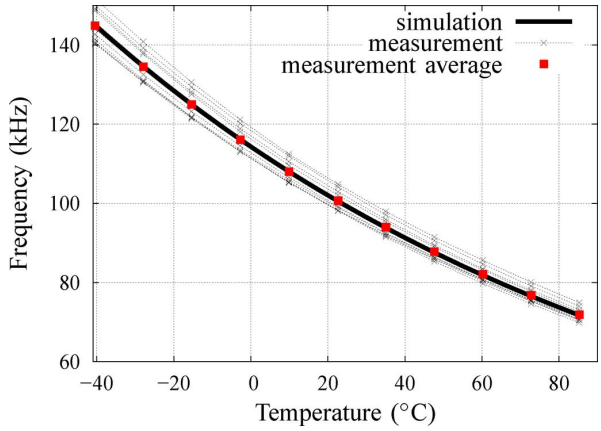

Fig. 9. Output frequency measurements and average on 11 samples ($V_R = 0.2$ V); the output frequency expected from simulation of the current reference is also shown with the solid line.

that at an output frequency of 100 kHz, the error is less than 0.1% for supply voltages above of 1.12 V.

Measurements on 11 samples from one batch were performed over the industrial temperature range (−40 °C to +85 °C) using a temperature-controlled oven. The measurement setup was designed to accurately stabilize the temperature of the samples during measurements (to within 0.01 °C); however, this stable temperature could only be set with an inaccuracy in the order of 0.1 °C. As the samples were not tested simultaneously, the measured data was post-processed to eliminate errors due to temperature mismatch. For each sample, frequency has been measured as a function of temperature. The data points were then interpolated to extract the values of frequency corresponding to a fixed set of temperatures. In Fig. 9, measurements are compared to simulations of the circuit of Fig. 2, where the solid line was obtained by using ideal models for all components except transistors M_1 and M_3. The measured output frequency shows the same temperature dependence of mobility as the simulations and an untrimmed inaccuracy of 7% (3σ) at room temperature. Its temperature dependence is approximately proportional to T^{α}, where T is the absolute temperature. The output frequency of the measured samples and the best fit of its average with the function T^{α} (obtained for $\alpha = -1.6$) are shown in the logarithmic plot of Fig. 10. After one-point calibration, the frequency spread with respect to average frequency has been computed in Matlab from the data in Fig. 9 and it is below 1.1% (3σ) over the range from −22 °C to 85 °C (Fig. 11). During the oven measurements only, capacitors C_A and C_B were biased in deep inversion ($V_{ddd} = 1.5$ V, $V_{r1} = 1.6$ V, $V_{r2} = 1.2$ V). This minimized the effect of threshold voltage spread on their capacitance, and ensured that the measured spread was mainly due to the core circuit.

IV. On Temperature Compensation

In the previous section it has been shown that the output frequency of the mobility-based oscillator is strongly temperature dependent (Fig. 9). However, Fig. 11 shows that the spread in this temperature dependence is in the order of 1%. This will be the residual error in the output frequency if the temperature

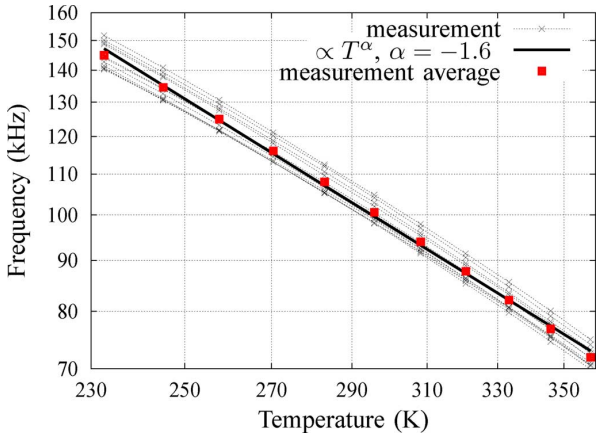

Fig. 10. Log-log plot of the output frequency (11 samples and their average for $V_R = 0.2$ V) versus the absolute temperature; the best fit using the function $f(T) = f_0 T^{\alpha}$ is included for comparison.

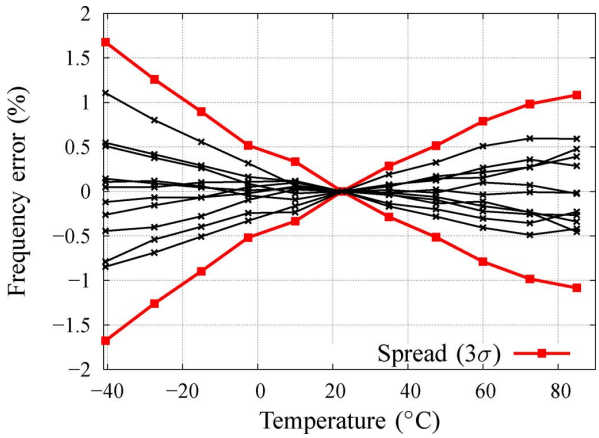

Fig. 11. Frequency error with respect to average frequency versus temperature after one-point trimming at room temperature with $V_R = 0.25$ V for 11 samples.

compensation scheme is perfect and if the oscillator is trimmed at a single temperature.

The compensation can be performed by varying a physical parameter in the oscillator circuit (Fig. 2), such as the voltage V_R, the gain of the current mirrors M_1–M_A and M_1–M_B, or the capacitance of C_A and C_B. Alternatively, compensation can be introduced in the processing of the output frequency, for example by varying the multiplication factor of a cascaded frequency multiplier or, if an alarm signal after a fixed time period is needed [2], changing the number of reference periods to be counted in the fixed period. In all these schemes, the compensation parameter should be varied as a function of the temperature and so a temperature measurement error will lead to additional spread.

If the frequency is approximated as $f = f_0 T^{\alpha}$ in a limited temperature range, an error in the temperature measurement will cause a relative error in the compensated frequency given by

$$\sigma_{\Delta f/f} \approx \sqrt{\sigma_0^2 + \left|\frac{T}{f}\frac{\partial f}{\partial T}\right|^2 \sigma_{\Delta T/T}^2} = \sqrt{\sigma_0^2 + \alpha^2 \sigma_{\Delta T/T}^2} \quad (6)$$

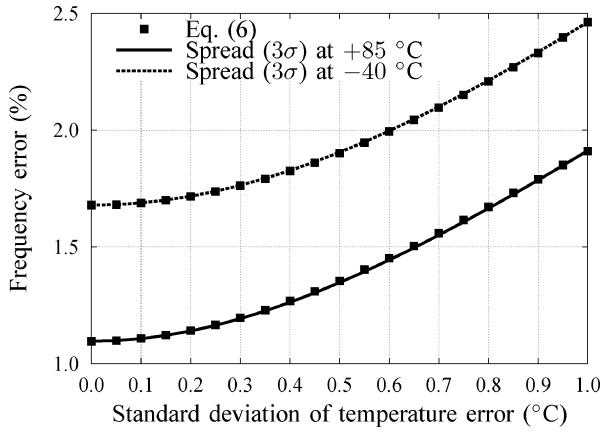

Fig. 12. Spread of the error of the compensated frequency versus the standard deviation of the error in temperature estimation; simulation results and computation of (6) are plotted respectively with lines and squares.

where $\sigma_{\Delta f/f}$ is the standard deviation of the error in the compensated frequency, σ_0 is the standard deviation of the error in the uncompensated frequency (i.e., the one reported in Fig. 11) and $\sigma_{\Delta T/T}$ is the standard deviation of the relative error in the temperature measurement. Simulations have been performed, assuming an ideal compensation by a multiplicative factor and a random error in temperature measurement, and the results are shown in Fig. 12. Equation (6) is also plotted in the figure using[6] $\alpha = -1.4$ for $-40\,^{\circ}$C and $\alpha = -1.9$ for $85\,^{\circ}$C. An increase in the spread of less than 0.05% is observed at both extremes of the temperature range for a temperature sensing error of $0.2\,^{\circ}$C. Such accuracy can be reached with conventional bandgap temperature sensors at a power dissipation in the order of some tens of μW [18], [19]. Since temperature variations are usually slow, a further reduction in power consumption can be achieved by duty-cycling the temperature sensor.

A lower sensitivity to temperature errors can be obtained if α in (6) is decreased. This can be achieved by making V_R a temperature- *dependent* voltage instead of a temperature-independent voltage. A particularly interesting case is when V_R is proportional to the absolute temperature (PTAT). This would be easy to realize, since such voltages are commonly employed in bandgap voltage references [21]. The use of a PTAT V_R would result in $\alpha \approx 0.5$ [with reference to (2)] and, consequently, to a smaller spread for a fixed accuracy of the temperature sensor. A PTAT V_R has been applied to the test chip and results are reported in Fig. 13. To reduce measurement time, the behaviour of the circuit at arbitrary values of temperature and voltage V_R were obtained by interpolating between actual measured data and the effect of compensation has been computed. The use of interpolation is the cause of the disturbances visible in Fig. 13. The application of a PTAT V_R increases the spread with respect to the constant V_R case (i.e., Fig. 11). Note that the compensation has been performed without adding any error in the temperature measurement. The larger spread can be explained by analyzing the effect of threshold voltage mismatch between

[6]The values used for α were obtained at $-40\,^{\circ}$C amd $85\,^{\circ}$C from the slope of the average frequency characteristic in Fig. 10.

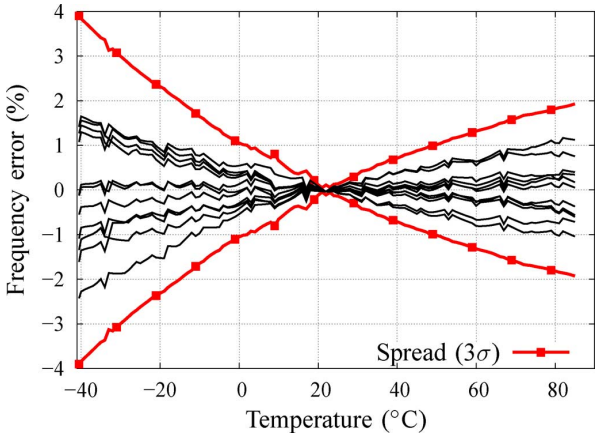

Fig. 13. Frequency error with respect to average frequency versus temperature after one-point trimming at room temperature with V_R proportional to absolute temperature (PTAT).

transistors M_1 and M_3 in Fig. 2. Taking into account a threshold voltage mismatch ΔV_{th} between M_1 and M_3, (1) is modified as

$$f(T) = \mu_n k \frac{C_{\text{ox}} \frac{W_1}{L_1}}{C} \frac{(V_R(T) + \Delta V_{th})^2}{V_{r1} - V_{r2}}. \tag{7}$$

After trimming at temperature T_0, it can be shown that the frequency error due to the threshold voltage mismatch is zero in the case of temperature-independent V_R and given by the following expression in the case of a PTAT V_R:

$$\frac{\Delta f'}{f'} \approx \frac{2\Delta V_{th}}{V_R(T_0)} \frac{T_0 - T}{T} \tag{8}$$

where f' is the output frequency after trimming. It can then be concluded that better performance can be achieved with compensation schemes which keep V_R temperature independent, and that the use of temperature-dependent V_R is only indicated if the matching between M_1 and M_3 can be significantly improved.

V. Conclusion

A fully integrated mobility-based 100-kHz frequency reference has been presented. Its frequency inaccuracy, due to temperature, supply variations and noise, respectively, is 1.1% (3σ) from $-22\,^\circ$C to $85\,^\circ$C, 0.1% with a supply variation of 0.27 V and 0.1% (rms) over a one second time span. This shows that, by adopting an appropriate temperature compensation scheme, the electron mobility can be used to generate a reference frequency accurate enough for WSN applications and that the proposed architecture is both low-voltage and low-power, as required by autonomous sensor nodes.

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