A Low-Voltage Mobility-Based Frequency Reference for Crystal-Less ULP Radios

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Abstract—The design of a 100 kHz frequency reference based on the electron mobility in a MOS transistor is presented. The proposed low-voltage low-power circuit requires no off-chip components, making it suitable for Wireless Sensor Networks (WSN) applications. After one-point calibration the spread of its output frequency is less than 1.1% (3σ) over the temperature range from -22 °C to 85 °C. Fabricated in a baseline 65-nm CMOS technology, the frequency reference occupies 0.11 mm² and draws 34 µA from a 1.2-V supply at room temperature.

I. INTRODUCTION

Wireless Sensors Networks (WSN) need radios that are small, cheap and energy efﬁcient. The largest fraction of the energy used in each node of a WSN is spent in idle listening to the channel [1]. If each node is equipped with an accurate time reference, synchronous networks can be employed to reduce the idle listening time. In that case, a higher accuracy of the time reference allows the receiver to predict the timeslot used by the transmitter with smaller error and to employ, consequently, a lower duty-cycle. Accuracy of a few ppm can be achieved by crystal-controlled oscillators (XCOs) but since such external components should be avoided in WSN nodes, accuracy can be given up for the sake of integration.

The tradeoff between integration and time/frequency accuracy is also present in the RF front-end. While commercial communication systems require high frequency accuracy, radios for WSN can be optimized to relax such speciﬁcations and so frequency accuracies of only a few percent are needed [1] [2]. In addition, the available power is limited to tens of µW, since the time reference is turned on continuously, and the supply voltage must be kept low to be compliant with typical WSN energy sources, such as batteries and energy scavengers.

Recently, much work has been devoted to implementing fully integrated frequency references in standard microelectronic technologies. The current state-of-the-art is illustrated in Fig. 1. LC oscillators [3] can provide accuracy and phase noise performances comparable to XCOs; however, it is impracticable to reduce their power consumption below 100 µW due to limited Q of integrated inductors and the possible need for high-speed frequency dividers. The accuracy of the compensated ring oscillator in [4] is high enough for WSN applications, but its power consumption is in the mW range. A very stable physical effect, i.e. the thermal diffusivity of bulk silicon, could be exploited for use in frequency references [5]; however, the silicon substrate needs to be heated to measure the diffusivity and this requires a few mW. The trimmed RC oscillator described in [6] also seems to achieve performances suitable for WSN, although the effect of process spread is not discussed.

An alternative way of realizing an accurate fully integrated oscillator is by employing charge mobility as a reference [7]. Mobility is less sensitive to process variations than other parameters, such as polysilicon resistance or oxide capacitance, and its standard deviation is less than 2% at room temperature for the adopted process. Although the temperature dependence of the mobility is large (approximately $T^{-1.3}$), it is well deﬁned and can be compensated for. The effect of process spread can then be removed by a single room temperature calibration.

This paper presents a proof of concept of a fully integrated oscillator referenced to the mobility, which can cover the WSN application area in Fig. 1. The oscillator is based on a current-controlled relaxation oscillator, in which the current is proportional to the mobility. Experimental validation of such approach will be provided, demonstrating a frequency spread in the temperature range of interest of less than 1.1% after one-point calibration and a power consumption of 41 µW. The circuit is presented in section II; experimental results are shown in section III and conclusions are drawn in section IV.

II. CIRCUIT DESCRIPTION

A. Oscillator structure

A simplified schematic of the oscillator is shown in Fig. 2. It consists of a current reference, two current mirrors $M_1 - M_A$ and $M_1 - M_B$, two capacitors $C_A$ and $C_B$ and a comparator.
The drain current of $M_1$ is mirrored by $M_A$ and $M_B$ with a gain of four and, as explained in the next section, is given by

$$I_1 = \frac{I_A}{4} = \frac{I_B}{4} = \frac{\mu_n C_{ox} W_1}{2} L_1 R_B^2$$  \hspace{1cm} (1)

where $\mu_n$ is the electron mobility, $C_{ox}$ the gate capacitance per unit area and $k$ a constant determined by ratios of matched transistors sizes. As shown in the timing diagram in Fig. 3, $C_A$ and $C_B$ are alternatively precharged to $V_1$ and then linearly discharged by $M_A$ and $M_B$. When the voltage on the discharging capacitor drops below $V_{th}$, the output of the comparator switches and the linear discharge of the other capacitor starts immediately, while the recharge is delayed by $D$. The delay $D$ ensures that non-idealities of the comparator do not affect the slope of the discharge at the crossing of $V_{th}$ and it is not critical, as it does not influence the period $T$. The delay $D$ and the signals driving the switches are generated by a digital circuit not shown in Fig. 2.

By inspecting Fig. 2 and Fig. 3, the period and frequency of oscillation can be easily determined, and from (1):

$$T = \frac{2C}{I_A} (V_1-V_2) \Rightarrow f = \frac{1}{T} = \frac{\mu_n C_{ox} W_1}{2} L_1 C (V_{1} - V_{2})$$  \hspace{1cm} (2)

where $C = C_A = C_B$. $C_A$ and $C_B$ are implemented with MOS capacitors operated in inversion and matched with transistor $M_1$, in order to obtain a process and temperature independent ratio $C_{ox}W_1/L_1$. If the reference voltages $V_{1}$ and $V_{2}$ are obtained from a bandgap reference, the residual frequency variations will be due to the spread and temperature dependence of the mobility and the voltage $V_{th}$. The latter can be used as a control voltage to compensate for the effects of temperature variations and process spread.

The two multiplexers at the input of the comparator are driven by the signal $\text{chop}$, shown in Fig. 3, to mitigate the effect of comparator offset. Thus, with an offset $V_{os}$ at the comparator input, the output is switched when $V_A = V_{1} - V_{os}$ or $V_B = V_{2} - V_{os}$ and the total error in the period is given by

$$\Delta t = \frac{V_{os}}{2(V_{1} - V_{2})} \left( \frac{\Delta C}{C} + \frac{\Delta I}{I_A} \right)$$  \hspace{1cm} (3)

where $\Delta C = C_A - C_B$ and $\Delta I = I_A - I_B$. Hence, if the capacitors and current mirrors are well matched, the resulting error is small. Since those components work at low frequency, good matching can be obtained by increasing device area and without significantly affecting oscillator’s performances.

B. Current reference

The operation of the circuit in the dashed box in Fig. 2 can be understood by noting that $M_2$, $M_4$ and $OA_2$ constitute a low-voltage current mirror and that $M_1$ is effectively diode-connected through $OA_1$ and $R$. Using the square-law MOS model, it is possible to derive \[8\]

$$I_1 = \frac{\mu_n C_{ox} W_1}{2} L_1 \left( \frac{V_{R}}{2m} - 1 \right)^2$$  \hspace{1cm} (4)

where $n = W_{4}/L_4$ and $m = W_{5}/L_5$.

The complete schematic is shown in Fig. 4. The current source $I_0$ is implemented by the unity-gain cascode current mirror $M_5 - M_8$. The value of $I_0$ is fixed by the current mirror $M_9 - M_{12}$ and by the external opamp\(^1\), which forces a voltage drop $V_R$ on $R_1$, so that $R_0 I_0 = R_1 \frac{W_5}{L_5} V_R = V_R$. Resistance values ($R_0 = 200 \text{ k}$, $R_1 = 20 \text{ k}$) are chosen as a tradeoff between resistor area, current consumption and the contribution of the parasitic currents through $R_1$.\(^2\)

The start-up circuit and the implementation of the opamps are shown in the dashed boxes in the figure. A folded cascode structure is adopted for $OA_2$ to reduce its systematic input offset. Since $OA_1$ must provide an output quiescent current $I_0$, it is biased with $I_{17} = I_0/2$ and it is dimensioned such that $\frac{W_{12}}{L_{12}} = \frac{W_1}{L_1}$ and $\frac{W_{13}}{L_{13}} = \frac{W_2}{L_2}$. The MOS capacitor $M_{27}$ and the fringe metal capacitor $C_{c}$ are compensation capacitors for the feedback loops involving respectively $OA_1$ and $OA_2$.

To avoid coupling digital noise to the gate of $M_1$ via the output mirrors $M_1 - M_{12}$, $M_A$ and $M_B$ of Fig. 2, the current is mirrored to $M_4$ and $M_3$ using the node $V_{G2}$ and additional pMOS and nMOS mirrors (not shown in Fig. 4).

C. Comparator

The delay of the comparator must be negligible with respect to the oscillation period $T$. This requires high gain and large bandwidth in the case of an open-loop topology, or a very small hysteresis in the case of a Schmitt trigger implementation. To overcome this problem, within the constraints of \(^1\) An external opamp is used only for testing purpose.\(^2\) Note that a pad with large ESD protection diodes is connected to one end of $R_1$.\(\text{Fig. 2. Mobility-referenced oscillator.}\)

\(\text{Fig. 3. Oscillator waveforms.}\)
a very tight power budget, an autolatch comparator was introduced. Its schematic is shown in Fig. 5 for the case when chop = 0 together with some waveforms. The core of the circuit is a dynamic latch. When a comparison is needed, a digital circuit resets the latch and then enables it. As long as \( V_B \) has not crossed \( V_{1,2} \), \( V_1 \) goes periodically to \( V_{dd} \) and \( V_2 \) to ground. The signal on \( V_2 \) is inverted and delayed to generate the \( \text{RESET} \) signal. \( V_1 \) and \( V_2 \) are then pulled up to \( V_{dd} \) and, after a delay, \( \text{RESET} \) go low. This cycle is repeated until \( V_B \) crosses \( V_{1,2} \) and \( V_1 \) go low. In this case the output is represented by the voltage on \( V_1 \). When \( \text{chop} = 1 \), the logic takes care of generating \( \text{RESET} \) from the appropriate node and chooses the right output node. The latch is preceded by a folded preamplifier to prevent kickback noise appearing on oscillator’s capacitors.

The delay of the comparator can be adjusted controlling the period of the described cycle. Simulations show that the delay is less than 13 ns in the worst case (process and temperature) with a total average current of 30 \( \mu \)A at 1.2 V supply. Low power is achieved by keeping the devices small, so as to minimize parasitic capacitance. Small devices have high flicker noise, but the offset compensation technique described by (3) also reduces the effect of flicker noise.

III. EXPERIMENTAL RESULTS

The oscillator has been realized in a baseline TSMC 65-nm CMOS process. The circuit occupies 0.11 mm\(^2\) and uses only 2.5-V I/O thick oxide MOS devices. 1.2-V thin oxide devices were avoided because of their high gate current, which is not negligible in very low current circuits. Most of the area of the circuit is occupied by the current reference and by the oscillator capacitors (Fig. 6). For flexibility in testing, all the reference voltages (\( V_{ref,1} \), \( V_{ref,2} \), \( V_R \)) were provided externally. For a nominal oscillation frequency of approximately 100 kHz, the reference current is \( I_1 = 125 \) nA for \( C = 6 \) pF, \( V_R = 2 \) V, \( V_{ref,1} = 1 \) V and \( V_{ref,2} = 0.6 \) V. A low frequency was chosen to reduce the impact of parasitic effects, such as comparator delay. The total current consumption with 1.2 V supply voltage is 34.3 \( \mu \)A (18.9 \( \mu \)A for comparator ad logic; 14.4 \( \mu \)A for current reference; 1 \( \mu \)A through pin \( V_{ref} \)). Note that to reduce the effect of ESD leakage currents, the current in \( R_1 \) is relatively large (10 \( \mu \)A). If the reference voltage \( V_R \) were integrated on chip, this current would be negligible. Consumption can be strongly reduced with a less accurate or duty-cycled comparator. Since the aim is to prove the feasibility of the proposed concept, the testchip was not fully optimized for power consumption but for accuracy.

Long-term jitter measurements are reported in Fig. 7, together with lines showing the extrapolated thermal and flicker noise components. Period jitter is 52 ns (rms) and is dominated by comparator thermal noise. After a large number of periods, jitter is dominated by flicker noise from the current reference. Relative jitter is defined as the standard deviation of jitter divided by elapsed time; its value for a time period of the order of 1 s is an important parameter for time references used in WSN, since it limits duty-cycle of the receiver when synchronization is performed over a time scale of seconds [1]. It can be proven that for most oscillators, relative jitter becomes flat for increasing time, as observed in the measurements. The relative jitter is 0.1% after 1 s and is negligible compared to the temperature-induced frequency drift.

3The area labeled as “capacitors” in Fig. 6 contains also transistors \( M_3 \) ad \( M_4 \) of the current reference, which are required to match with MOS capacitor \( C_A \) and \( C_B \).
A fully integrated mobility-based frequency reference has been presented. Its frequency inaccuracy, due respectively to temperature, supply variations and noise, amounts to 1.1% (3σ) from -22 °C to 85 °C, 0.1% with 0.24 V supply variation and 0.1% (rms) over 1 s time span. This shows that, by adopting an appropriate temperature compensation scheme, mobility can be used to generate a reference frequency accurate enough for WSN applications and that the proposed architecture is both low-voltage and low-power, as required by autonomous sensor nodes.

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REFERENCES