A PROGRAMMABLE-LOAD CMOS RING OSCILLATOR/ INVERTER CHAIN FOR PROPAGATION-DELAY MEASUREMENTS

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Abstract

This paper describes a test structure consisting of a ring oscillator and an inverter chain. The load of the elements of the ring oscillator and the inverter chain is programmable. The propagation-delay times measured give a better correlation with real logic circuits.

Introduction

A test structure often used for the characterization of the circuit performance in a particular process is the ring oscillator [1] or the inverter chain [2]. Characterization involves the evaluation of parameters such as speed/power product, propagation-delay time and fan-out capability.

Several implementations of ring oscillators and inverter chains have been reported. Generally, inverters or NOR gates [3] have been used to built these structures. Ring oscillators and inverter chains are often built with elements having a fan-out or fan-in of 1. The propagation-delay time or oscillation frequency of such structures therefore provides an optimistic prediction of the propagation-delay times measured under real load conditions. This is because effects due to interconnect capacitances and actual circuit loads are not taken into account. Propagation-delay times measured from such structures can therefore only serve as an upper bound for delays that can be expected for the actual logic circuits.

Yu et al. [4] found propagation-delay times in a high speed ring oscillator that varied from 100 ps up to 2 ns., depending upon the load. Several types of ring oscillator circuits having various fixed loads were used for their measurements.

This paper presents a test structure consisting of a combination of a ring oscillator and an inverter chain. The elements of this structure are connected to a programmable load varying from a fan-in of 1 upto a fan-in of 15. In this way, the operating environment of the circuit can be simulated in hardware. The measurements can be carried out by means of a conventional automated digital measurement system providing AC- and DC-parametric measurement capabilities.

Circuit description

The circuit diagram of the test structure is shown in figure 1. A single delay element is denoted as τ. If the input RO-enable is HIGH, the circuit acts as a ring oscillator; if the input RO-enable is LOW, the circuit acts as an inverter chain. Two transmission gates are used to select the mode of operation.

The circuit consists of 43 delay-elements in the ring oscillator mode. The number of delay elements is chosen in such a way that the measurements can be carried out with sufficient accuracy. The input Trigger is used as the start input of the ring oscillator in order to synchronize the ring oscillator and avoid oscillation at a high harmonic frequency. The oscillation frequency can be measured at output RO-out.

In the inverter-chain mode the inverter chain consists of 43 delay-elements. If a transition

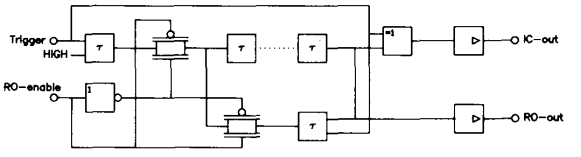

Fig. 1. Circuit diagram of the ring oscillator/ inverter chain.

from LOW to HIGH is applied to the input Trigger, a pulse with width w can be measured at the output IC-out. The second input of the first delay element of the inverter chain is connected to HIGH in order to obtain an equal delay path in both ring-oscillator mode and the inverter-chain mode.

Figure 2 shows the circuit diagram of a single delay element. Transmission gates are used for the selection of the appropriate load. The load of the delay element can be programmed by means of the inputs sel2, sel4 and sel8. The loads LD2, LD4 and LD8 consist respectively of 2, 4 or 8 inverters in parallel.
The chip lay-out of the delay element is shown in figure 4.

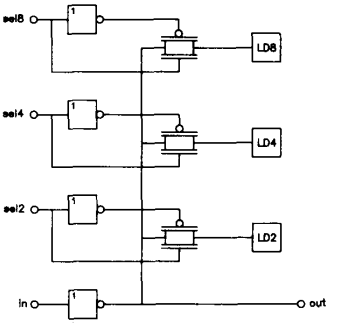

Fig. 2. Circuit diagram of a delay element τ.

Simulation results

The SPICE simulations of the test structure in the ring-oscillator mode and the inverter-chain mode showed a linear relationship between the propagation delay times and the load of each delay element. The parasitic effects due to the transmission gates were taken into account. The simulation results are depicted in figure 3.

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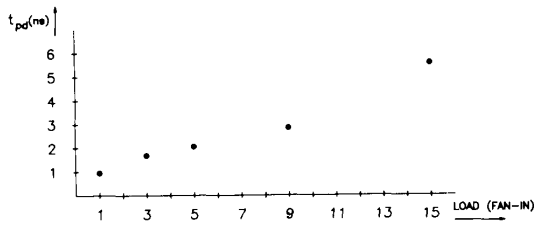

Fig. 3. Propagation-delay versus load for the inverter chain.

The test circuit is part of a CMOS Process Control Module (PCM) and incorporates test structures for the evaluation of process-parameters, SPICE-mosfet model-parameters and circuit-parameters. A 2 × N probe pad arrangement is used [6]. The PCM has been fabricated at the university of Twente in the Retrograde Twin Well UT-CMOS process [7].

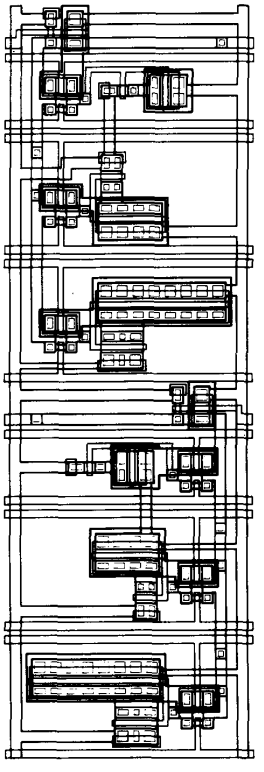

Fig. 4. Chip lay-out of a delay element.

Conclusions

Traditional designs of ring oscillators and inverter chains are often built up with single delay elements, e.g. inverters or NOR gates. The propagation delay times found, only serve as an upper bound for the actual logic circuits.
For a better correlation with real logic circuits the measurements have to be carried out on several test structures, having different load conditions.
The circuit presented here offers the capability to carry out propagation delay-measurements on two circuit types and under a number of load conditions. Its feature is that full characterization only takes one test circuit.

References

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