DIFFERENTIAL INPUT CURRENT INTEGRATOR FOR CHARGE DOMAIN NETWORKS

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ABSTRACT

This paper presents an input structure for Charge Domain Networks. In most Charge Domain Filters two inputs are required. Therefore two complementary signal charge packets superposed on a time-invariant bias charge packet are applied to the inputs. In the presented input structure, the charge packets are realised by current integration, providing excellent linear charge-to-voltage conversion for both surface channel and buried channel Charge Coupled Devices.

I. Introduction.

By way of its operation [1], every impulse response from one input to one output in a Charge Domain Network possesses only positive elements. However, most impulse responses to be realised, possess elements of both signs. To overcome this problem, one may imagine the overall impulse response to be composed of an impulse response from one input to which the original signal is applied and an impulse response from a second input to which the inverted signal is applied. Two complementary driven fill-and-spill inputs could be used, but it is difficult to obtain two signal charge packets with exactly the same size but opposite sign. A slight asymmetry in the complementary signal charge packets will lead to a shift of the zeros which characterize the frequency response of the network.

fig. 1. Differential input current integrator for Charge Domain Networks.

The input structure [2], shown in fig. 1, avoids this problem, due to its differential structure. The sources of transistors M1 and M2 are connected to a common current source. At the drain of M1 and M2 two complementary signal currents occur, superimposed on a DC current. Every circuit, a new potential well occurs at the drain of the

shielding MOSFETs and during one clock period, the current is flowing into this well and integrated into a charge packet. See fig. 2. The voltage-to-charge conversion is performed implicitly by this structure. Especially for filter applications, where signal processing is performed in the charge domain, excellent linearity is required for the voltage-to-charge conversion at the input for surface channel as well as for buried channel CCDs. Therefore an improved version of the circuit - see fig. 7 - with excellent linearity will be discussed in section IV.

III. Frequency Response of the Current Integrator.

The Fourier transform of a time-continuous integrator of current $I_1(t)$ is given by

$$F \left( \int_0^t I_1(t) \, dt \right) = \frac{1}{jw} I_1(jw)$$

with $I_1(jw)$ the Fourier transform of $I_1(t)$.

By integrating the current over a period $t-T$ instead of over $t$, we obtain the following Fourier transform:

$$F \left( \int_0^{t-T} I_1(t) \, dt \right) = \frac{1}{jw} e^{-jwu} I_1(jw).$$

Integration over a time period from $t-T$ to $t$ yields

$$F(Q_n(t)) = F \left( \int_{t-T}^t I_1(t) \, dt \right) = \frac{1}{jw} \left( 1 - e^{-jwu} \right) I_1(jw).$$

Subsequently the Fourier transform of $Q_n(t)$ can be found by considering the Fourier transform of $Q_1(t)$ sampled every clock period $T$. Algebraically:

$$F(Q_n(t)) = \sum_{k=-\infty}^{\infty} e^{-jwu(2k+1)} I_1(jw) \frac{2jkw}{jkw + \frac{1}{2jkw}}.$$
\[ Q_0^1(j\omega) = \frac{\sin(\frac{\omega T}{2})}{j(\frac{\omega T}{2})} e^{j\frac{\omega T}{2}} I_1(j\omega) \] (7)

with \( Q_0^1(j\omega) \) : \( n \)th alias of the Fourier Transform of \( Q_1(nT) \).

The attenuation, occurring at frequencies larger than the Nyquist frequency, shows the anti-aliasing character of this input structure.

III. Experimental Verification of the Frequency Response

The integrated circuit, shown in fig. 3, is used to measure the frequency response of the differential current integrator. The circuit consists of the differential current integrator in series with two programmable second order transversal filters and two floating diffusion outputs. The circuit has been realised in the buried channel P-OCD-technology [3] developed at Eloma Philips, the Netherlands.

![Microphotograph of programmable Charge Domain Filter with differential input current integrator.](image)

fig. 3. Microphotograph of programmable Charge Domain Filter with differential input current integrator.

Schematic representation of the circuits is shown in fig. 4. The programmability of the circuit allows it to be used as a single delay line. In this mode the charge from two of the three separate channels is drained via the accessory switches. Now a short OCD delay line remains on which the performance of the input circuits has been evaluated.

![Schematic representation of the integrated circuit.](image)

fig. 4. Schematic representation of the integrated circuit.

The frequency response \( Q_0^1(j\omega) \) has been measured by means of a network analyzer. See fig. 5. The measured frequency response is in good agreement with the theoretical prediction (7). Only in the vicinity of the clock frequency small deviations occur from (7). The response should vanish for \( \omega = \omega_p \) instead of \( \omega = \omega_b \), as it does. Moreover during the experiments, it is observed that these deviations vary strongly with slight changes in the clock signals.

![Comparison between measured frequency response (A), theoretical frequency response with (B) and without (C) correction for the transconductance modulation.](image)

fig. 6. Comparison between measured frequency response (A), theoretical frequency response with (B) and without (C) correction for the transconductance modulation.

The measured deviations can be explained, if transconductance modulation by clock signals is presumed:

\[ I_1(t) = U_d(t) \frac{I_m}{2} (1 + \Delta \cos(\omega_c t + \phi)) \] (8)

with \( U_d(t) \) : differential input voltage;
\( I_m \) : transconductance of M1 and M2;
\( \Delta \) : modulus of the transconductance modulation;
\( \phi \) : transconductance modulation phase;
\( \omega_c \) : clock frequency given by \( 2m/T \).

Suppose a differential sine wave input voltage equal to \( U_d \cos(\omega t) \). In that case \( I_1(t) \) contains three components:

\[ I_1(t) = U_d \frac{I_m}{2} \left[ \cos(\omega t) + \cos((\omega - \omega_c) t - \phi) + \cos((\omega + \omega_c) t - \phi) \right] \] (9)

Subsequently the current \( I_1(t) \) is integrated over a period \( T \). Depending on the frequency of the first term, this term will be attenuated more or less according to (7). If \( \omega \) approaches the clock frequency \( \omega_c \), the term with frequency \( \omega \) in (9) will be attenuated very strongly. However the component with frequency \( \omega = \omega_c \) in (9) will pass the integrator almost unattenuated.

The term with frequency \( \omega = \omega_p \) will be attenuated like the first term. After the integration, \( I_1(t) \) is sampled every clock period \( T \). But now all terms, due to the aliasing, 'shift back' to the original frequency \( \omega \). Especially the term of \( I_1(t) \) near frequency 0 gives rise to the measured deviations of the frequency response for frequency \( \omega \). A computer program has been written to fit \( \Delta \) and \( \phi \), to correct
the theoretical model to the measured data. In fig. 6 an example of a measured frequency response and its corresponding fit are shown. The modulus $\Delta$, which has been found, is equal to 0.10% and the phase $\phi$ is equal to 0.98°. This low value of the modulus $\Delta$ occurs because the input $I$ is modulated. It is therefore very important to keep ground as free from clock signals as possible.

However, we should not worry too much about the transconductance modulation by clock signals, since it does not introduce extra distortion and the influence on the frequency response is negligible for frequencies below the Nyquist frequency.

IV. Distortion.

In CCDs in general, the main sources for non-linearities and noise are the input and the output structure. The harmonic distortion of the input depends strongly on the ratio $n$ of the amplitude of the signal charge, $max(Q_{b})$, and the bias charge $Q_{b}$:

$$n = \frac{max(Q_{b})}{Q_{b}} \text{.} \quad (10)$$

For the fill-and-spill input in a surface channel CCD, Sèquin and Mohsen [5] have found a total harmonic distortion (THD) of app. 0.7 % for $n=0.5$. In a buried channel CCD, the measured THD for $n=0.5$ was measured to be approximately 2.5 %.

for the circuit shown in fig. 7. Measurements show 1 % THD for signal charge amplitudes up to 90 % of the bias charge. Currently this new input structure is used in experimental HP Charge Domain filters.

fig. 9. Measured and theoretical predicted total harmonic distortion (THD) versus $n$, the ratio amplitude signal charge to the magnitude of the bias charge. The signal frequency is equal to 1 kHz.

This can be achieved by using the circuit shown in fig. 7. This circuit has been realised in a PCCD technology by Eloi & Philips, the Netherlands, as shown in fig. 8. In fig. 9, the measured distortion is compared with the theoretical predictions (11). Excellent agreement is obtained and a considerable increase in linearity is gained, using this circuit.

V. Conclusion.

A differential input current integrator especially suited for Charge Domain Networks, operating in the video frequency band, is presented. It possesses an anti-aliasing frequency response, suppressing the higher frequencies. Additionally no extra clock pulse is required, in contrast with the fill-and-spill input. The circuit has been realised and the measured frequency response is in good agreement with the theoretical predictions. Small deviations in the vicinity of the clock frequency can be explained by transconductance modulation by clock signals. Further improvement of the linearity is obtained by using the circuit in fig. 7. Measurements show 1 % THD for signal charge amplitudes up to 90 % of the bias charge. Currently this new input structure is used in experimental HP Charge Domain filters.

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VII. References.


fig. 8. Microphotograph of the realised improved differential input current integrator.