Voltage Boosting Amplifier Techniques for Underwater Sensor Networks: Theory and Design

The background is a deep teal color with a subtle pattern of small white dots, resembling a starry night sky or underwater particles. Large, flowing, wavy lines in shades of yellow, orange, and red sweep across the upper half of the image. In the lower half, there are four stylized representations of underwater sensors or buoys, each with a yellow cylindrical body and a spiral antenna. These sensors are surrounded by concentric circles and wavy lines, suggesting signal transmission or detection. A single orange starfish is positioned in the bottom right corner.

Saifullah Amir

Voltage Boosting Amplifier Techniques for Underwater Sensor Networks: Theory and Design

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DISSERTATION

to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
prof. dr. T. T. M. Palstra,
on account of the decision of the Doctorate Board,
to be publicly defended
on Wednesday 7th of October 2020 at 16:45 hours

by

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This work is part of SeaSTAR project (no. 10552) and was supported by the Netherlands Organization for Scientific Research (NWO).

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Typeset with $\text{\LaTeX}$.

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ISBN 978-90-365-5035-2

DOI 10.3990/1.9789036550352

<https://doi.org/10.3990/1.9789036550352>

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Allah does not charge a soul except [with that within] its capacity.

Surah Al-Baqarah [2:286] - The Noble Quran

Dedicated to

My amazing parents, my lovely wife Sana,
my supportive siblings Assad and Sumbal and
my world
Haadi and Hashir.

ABSTRACT

The innovations in Wireless Sensor Networks (WSNs) has changed the way we communicate today. While radio based wireless communication has entered a mature phase of commercialization, underwater communication technology is still lagging behind. The most widely used type of communication for underwater is acoustic communication. This is due to the fact that acoustic communication allows long range underwater communication as compared to optical and radio based wireless communication. However issues with slow acoustic propagation, limited available bandwidth, variations in channel propagation and power efficiency makes the development of reliable and energy efficient Underwater Sensor Networks (USNs) a major challenge.

However the development of reliable and low cost USNs has a great potential of revolutionizing many areas of underwater monitoring, sensing, navigation, detection and many more. The progress in USNs involves many key areas including signal processing, underwater channel modeling, transducer design, energy harvesting and efficient amplifier design, to name a few. In this thesis we focus on the techniques for an energy-efficient amplifier design, in particular the associated challenges in driving piezoelectric loads with limited supply voltages.

Therefore to gain insight into the design aspects of the amplifier, different existing amplifier topologies suitable for driving piezoelectric transducers are reviewed with focus on wide bandwidth, low distortion and supply boosting. To improve power efficiency a voltage boosting amplifier that combines signal generation and supply boosting can be a good choice for driving piezoelectric transducers.

Following the review of amplifier topologies, Peak Current Mode Con-

trol (PCMC) based feedback is chosen as a key candidate for voltage boosting amplifiers due to the advantage of achieving wideband along with ease of compensation. A modeling approach is presented that calculates an accurate open loop transfer characteristic for boost converters that employ PCMC. Many techniques exist for modeling a PCMC based boost converter, however all these techniques focus on purely resistive loads and are not always accurate for a purely capacitive load. In this thesis a new modeling technique is presented which is simple and gives accurate results for both capacitive and resistive loads. Furthermore, the useful expressions for DC gain and pole locations of a boost converter operating in Continuous-Conduction Mode (CCM) with PCMC are derived and compare well to simulations and measurements.

Furthermore the presented modelling technique is extended by calculating the current-loop transfer characteristic of PCMC based converters running in CCM. The accuracy of the control-to-inductor current transfer is improved for capacitive loads, which is not correctly predicted by previous modeling methods. The resulting model for the control-to-output voltage transfer thus obtained is valid for the major basic converter topologies boost, buck and buck-boost.

Finally the design of a high-voltage amplifier for a piezoelectric transducer is presented, which incorporates boosting and signal generation within a single boost converter stage improving the total efficiency of the system. The proposed architecture combines hysteretic ripple current-mode control with an adaptive soft switching technique to achieve improved power efficiency over the full output power range. This is achieved by dynamically controlling the inductor current ripple to keep the converter running in soft switching. The feedback control and the soft switching regulation are implemented in a $0.25\text{ }\mu\text{m}$ 60V TSMC process with an external power stage. The system achieves a peak efficiency of 85% at 20W of output power up to 30 kHz signal frequency.

SAMENVATTING

Innovaties in draadloze sensornetwerken hebben grote invloed gehad op de manier waarop we communiceren. Terwijl draadloze radiocommunicatie een volwassen fase van commercialisering is ingegaan, blijft de technologie van onderwatercommunicatie nog steeds achter. Het meest gebruikte type communicatie voor onderwater is akoestische communicatie. Dit komt door het feit dat akoestische communicatie over langere afstanden mogelijk is vergeleken met optische en radio gebaseerde communicatie. Echter, lage geluidssnelheid, beperkte beschikbare bandbreedte, variaties in kanaalkarakteristieken en beperkte energie-efficiëntie maken de ontwikkeling van betrouwbare en energiezuinige onderwater sensor netwerken een grote uitdaging.

Betrouwbare en goedkope onderwater sensor netwerken zijn veelbelovend voor toepassingen als onderwatermonitoring, metingen op afstand, navigatie, detectie van indringers en nog veel meer. Dit vergt ontwikkelingen op het gebied van signaalverwerking, modellering van onderwaterpropagatie, transducerontwerp, energieopwekking en energie-efficiënte versterkers, om er maar een paar te noemen. In dit proefschrift richten we ons op de technieken voor het ontwerpen van energie-efficiënte versterkers, in het bijzonder de uitdaging van het aansturen van piëzoelektrische belastingen met een beperkte beschikbare voedingsspanning. Om inzicht te krijgen in de ontwerpaspecten van de versterker, worden verschillende bestaande versterkertopologieën die geschikt zijn voor het aansturen van piëzoelektrische transducers beoordeeld op bandbreedte, vervorming en de mogelijkheid de uitgangsspanning tot boven de voeding uit te sturen. Om de energie-efficiëntie te verbeteren, kan een spanningsverhogende versterker die signaalgeneratie en voedingsspanningsver-

menigvuldiging combineert, een goede keuze zijn voor het aansturen van piëzoelektrische transducers.

Na de beschouwing van versterkertopologieën, wordt op Peak Current Mode Control (PCMC) gebaseerde feedback gekozen vanwege de grote bandbreedte en het gemak waarmee een stabiele regeling gemaakt kan worden. Er wordt een model gepresenteerd dat een nauwkeurige open-lus overdrachtskarakteristiek berekent voor een boost-omzetter die PCMC gebruikt en in Continuous Conduction Mode (CCM) werkt. Er bestaan veel technieken voor het modelleren van een op PCMC gebaseerde boost-omzetter, maar al deze technieken zijn gericht op puur resistieve belastingen en zijn niet altijd nauwkeurig voor een puur capacatieve belasting. In dit proefschrift wordt een nieuwe modelleringstechniek gepresenteerd die eenvoudig is en nauwkeurige resultaten geeft voor zowel capacatieve als resistieve belastingen. Uitdrukkingen voor DC-versterking en poollocaties komen goed overeen met simulaties en metingen.

De gepresenteerde modelleringstechniek wordt verder uitgebreid door de stroom-lusversterking van PCMC-gebaseerde converters in CCM nauwkeurig te berekenen. De nauwkeurigheid van het model van regelspanning naar spoelstroom is verbeterd voor capacatieve belastingen, wat niet correct wordt voorspeld door eerdere modelleringmethoden. Het resulterende model voor de aldus verkregen overdracht van regelspanning naar uitgangsspanning is geldig voor de belangrijke basis-convertertopologieën boost, buck en buck-boost.

Uiteindelijk wordt een hoogspanningsversterker voor een piëzoelektrische transducer gepresenteerd, die boosting en signaalgeneratie bevat in een enkele boostconvertertrap die de totale energie-efficiëntie van het systeem verbetert. De voorgestelde architectuur combineert hysteretische rimpelstroomregeling met een adaptieve ‘soft switching’ techniek om een verbeterde energie-efficiëntie over het volledige uitgangsbereik te verkrijgen. De feedbackregeling en de ‘soft switching’ regeling zijn geïmplementeerd in een 0.25 μm 60V TSMC-proces met een externe eindtrap. Het systeem bereikt een piekefficiëntie van 85% bij 20 W uitgangsvermogen en heeft een bandbreedte van 30 kHz.

CONTENTS

ABSTRACT ·	vii
SAMENVATTING ·	ix
LIST OF ACRONYMS ·	1
LIST OF SYMBOLS ·	3
1 INTRODUCTION ·	5
1.1 Underwater Sensor Networks ·	7
1.2 Challenges in USN Design ·	9
1.3 Amplifier Design Challenges ·	10
1.4 Research Objectives & Thesis Outline ·	13
2 A REVIEW OF AMPLIFIERS FOR PIEZOELECTRIC LOADS ·	15
2.1 Introduction ·	15
2.2 Linear Amplifiers ·	16
2.3 Switching Amplifiers ·	18
2.4 Feedback Control Strategies ·	22
2.5 Conclusions ·	24
3 MODELING PEAK CURRENT MODE CONTROL FOR BOOSTING AMPLIFIERS ·	27
3.1 Introduction ·	27
3.2 Limitations of Existing Modeling Approaches ·	29
3.3 Small-Signal Analysis ·	35
3.4 Simulation Results ·	43
3.5 Experimental Verification ·	45

	3.6	<i>Conclusions</i>	· 48
4	EXTENSION OF THE MODELING TECHNIQUE TO BASIC PCMC SWITCHING CONVERTERS · 49		
	4.1	<i>Introduction</i>	· 49
	4.2	<i>Limitations of Existing Modeling Technique</i>	· 50
	4.3	<i>Extended Modeling Approach</i>	· 56
	4.4	<i>Verification of the Extended Modeling Technique</i>	· 60
	4.5	<i>Conclusions</i>	· 64
5	A SELF-OSCILLATING BOOSTING AMPLIFIER WITH ADAPTIVE SOFT-SWITCHING CONTROL · 65		
	5.1	<i>Introduction</i>	· 65
	5.2	<i>Ripple HCMC and Soft-Switching Regulation Scheme</i>	· 67
	5.3	<i>System and Circuit Implementation</i>	· 78
	5.4	<i>Measurements</i>	· 84
	5.5	<i>Conclusions</i>	· 91
6	CONCLUSIONS AND RECOMMENDATIONS · 93		
	6.1	<i>Summary and Conclusions</i>	· 93
	6.2	<i>Original Contributions</i>	· 96
	6.3	<i>Recommendations</i>	· 96
7	APPENDIX A · 97		
	7.1	<i>Discrete-time model for buck converter</i>	· 97
	7.2	<i>Small signal discrete-time model</i>	· 100
	7.3	<i>State space model and transfer functions</i>	· 102
A	DERIVATION OF DISCRETE-TIME MODEL FOR A BUCK CONVERTER · 103		
	A.1	<i>Discrete-time Model for Buck Converter</i>	· 103
	A.2	<i>Small Signal Discrete-time Model</i>	· 106
	A.3	<i>State Space Model & Transfer Functions</i>	· 108
	BIBLIOGRAPHY · 109		

LIST OF PUBLICATIONS ·115

ACKNOWLEDGEMENTS ·117

ABOUT THE AUTHOR ·121

xiii

CONTENTS

LIST OF ACRONYMS

CCM	Continuous-Conduction Mode.
CMC	Current Mode Control.
EMI	Electro Magnetic Interference.
ESR	Equivalent Series Resistance.
HCMC	Hysteretic Current Mode Control.
ISI	Inter Symbol Interference.
OFDM	Orthogonal Frequency-Division Multiplexing.
PCMC	Peak Current Mode Control.
PWM	Pulse Width Modulated.
QAM	Quadrature Amplitude Modulation.
RF	Radio Frequency.
RHPZ	Right-Half Plane Zero.
SONAR	SOund NAvigation and Ranging.
THD	Total Harmonic Distortion.
USN	Underwater Sensor Network.
VMC	Voltage Mode Control.
WSN	Wireless Sensor Network.

LIST OF SYMBOLS

$\overline{i_{L t_1}}$	Average inductor current during t_1 .
$\overline{i_{L t_2}}$	Average inductor current during t_2 .
α	Slope compensation affect.
ΔV_{win}	Hysteretic window voltage.
ω_p	Dominant pole frequency.
ω_{rhpz}	Right-Half plane Zero frequency.
ω_{zero}	ESR zero frequency.
C	Output Capacitance.
D	Duty ratio.
F_m	Modulator gain for Ridley model.
F_{m1}	Modulator gain for Tan model.
F_{m2}	Modulator gain for Bryant model.
G_0	DC gain.
$G_{id}(s)$	Duty-to-inductor current transfer function.
$G_{vd}(s)$	Duty-to-output voltage transfer function.
$H_e(s)$	Sampling effect in current feedback loop.
L	Inductance of the inductor.
M_1	Slope of sensed inductor current during on period.
M_2	Slope of sensed inductor current during off period.
M_{HS}	High side switch.
M_{LS}	Low side switch.

M_a	Artificial slope.
M_c	Slope of external ramp.
R_L	Load resistance.
R_{esr}	ESR of capacitor.
R_{fb1}	Feedback resistor.
R_{fb2}	Feedback resistor.
R_s	Current sense gain.
$T_{ci}(s)$	Control-to-inductor current transfer.
$T_{co}(s)$	Control-to-output voltage transfer function.
T_s	Switching period.
f_s	Switching frequency.
i_F	Fictional current.
i_L	Inductor current.
i_{Lp}	Peak inductor current.
k_r	Output voltage feedforward gain for Ridley model.
k_{r1}	Output voltage feedforward gain for Tan model.
k_{r2}	Output voltage feedforward gain for Bryant model.
m_c	Slope compensation factor.
s_n	Shipping noise.
v_C	Control input voltage.
w_n	Wind speed.

CHAPTER 1

INTRODUCTION

Effective communication has played a vital role in the development and progress of humankind. Nearly two hundred years ago, the only method of communication over a long distance was by using a messenger or birds. Over time, wireless communication technology has seen tremendous improvements since the discovery of electromagnetic waves by James C. Maxwell in the 1860s. Nowadays, endless possibilities exist for cheap, fast and effective wireless communication at almost any place around the globe. However, the same is not true for the vast oceans that cover the earth's surface, as underwater communication remains quite limited by comparison.

Present day underwater communication involves sound (acoustic), light (optical) or electromagnetic waves (radio). Researchers have investigated the use of underwater Radio Frequency (RF) electromagnetic waves for many years [1]; however, no popular solution exists due to the highly conductive nature of water, which causes rapid fading of RF waves when transmitted underwater. On the other hand, optical communication provides promising data rates but only over very short distances because of severe absorption that occurs at the optical frequencies and strong backscattering from suspended particles [2].

As early as the fourth century BC, Aristotle was first to observe that sound could travel in air and water. For example, dolphins and whales

have been using sound to communicate over long distances in the ocean waters. The first direct experimental proof of underwater sound propagation and velocity measurement came from Colladon and Sturm in 1826. In their experiment, illustrated in Fig. 1.1 [3, 4], an underwater bell was struck simultaneously with a flash of light on the surface, while an observer at a considerable distance measured the time interval between the flash and the arrival of the sound. The measured speed of sound in the water came out to be 1435 ms^{-1} which is close to the modern day value of 1438 ms^{-1} at 8°C .

Figure 1.1: Drawing of Jean-Daniel Colladon, a Swiss physicist, and his assistant, Jacques Charles-Francois Sturm, calculating the speed of sound in water [3, 4].

Acoustic waves have been widely used for underwater communications and monitoring due to the low attenuation of sound waves in water. This property has enabled the development of acoustic communication as an exciting alternative compared to RF and optical communication.

1.1 Underwater Sensor Networks

In the early years of underwater acoustic communication, the main focus was mostly limited to the development of systems for military applications. One of the examples of such systems is active and passive SOUNd NAvigation and Ranging (SONAR). In contrast to traditional point-to-point based communication, developing real-time Underwater Sensor Network (USN) for both civilian and military applications has a vast potential of revolutionizing many areas of science and industry. The capability to observe and act on different physical phenomena with the help of small distributed devices opens up new opportunities.

The application area of this research (SeaSTAR project) is primarily focused on underwater wireless monitoring, where a network of USNs is used to monitor an area of interest with each node that offers short links. A typical USN consists of several network nodes spread across an area of interest, where each network node is capable of receiving and transmitting data to the neighbouring network node in real-time as shown in Fig. 1.2.

Figure 1.2: A typical illustration of USNs deployed in an area

1.1.1 Application Areas of USNs

In recent years, with the advancements in the field of integrated circuits, battery technology, digital signal processing, low-cost piezoelectric transducers and modeling of the underwater channel has led researchers to develop major enabling technologies for a wide range of maritime applications. Some of these areas of application are now briefly discussed here.

- ***Environmental monitoring.*** USNs can be used to monitor different environmental conditions such as water quality, temperature (like for the great barrier reef), ocean currents, and detection of hazards substances that affect marine ecosystems. These systems can also be used to track and understand different fish activities and other marine life.
- ***Disaster prevention.*** With the development of real-time USNs, undersea seismic activity monitoring can be done from remote locations, resulting in early tsunami warnings.
- ***Undersea exploration and maintenance.*** Offshore oil and gas pipelines can be monitored to identify problems like oil leaks as well as assess extraction sites.
- ***Assisted navigation.*** An underwater sensor can assist in identifying hazards objects on the seabed and in water for commercial shipping lanes. These can also help in monitoring and regulating maritime traffic.
- ***Underwater surveillance.*** Harbors can deploy USNs for both surface ships and underwater vehicle monitoring. Hence unauthorized traffic can be detected.

Hence the development of collaborative, real-time, cheap and more power-efficient underwater sensor networks offers excellent future potential. However, there are also associated challenges in practical implementation of such systems [5, 6], which are briefly discussed in the next section.

1.2 Challenges in USN Design

Underwater is a harsh environment for wireless communication and therefore poses many challenges due to the unique properties of water. Some of the important challenges associated with the development of USN are briefly explained here.

- **Path loss.** As sound waves travel in water, they get attenuated due to conversion of acoustic energy into heat, which increases with distance and frequency. Other contribution to path loss is due to geometric spreading of sound energy as a result of the expansion of the wave fronts. It increases with the propagation distance and is independent of frequency.
- **Noise.** Underwater noise is generated from mainly two sources. The first is categorised as man made noise, which is due to machinery noise and shipping activity. The second source of noise is called ambient noise, related to hydrodynamics (movement of water including tides, currents, storms, wind, rain, etc.).
- **Multi-path propagation.** Another major challenge in underwater communication is the time-varying multi-path propagation. This results in severe degradation of the acoustic communication signal, since it generates Inter Symbol Interference (ISI).
- **Propagation delay.** The propagation speed in the underwater channel is much lower than in the radio channel. This large propagation delay therefore makes the coherence bandwidth of the channel low. Additionally the propagation delay for underwater sound depends on temperature, water depth, and salinity.
- **Doppler spread.** The doppler frequency spread can be significant in under water channel, causing many adjacent symbols to interfere at the receiver, requiring sophisticated signal processing to deal with the generated ISI.

- **Battery power.** Limited battery power is also one of the major issues. USN nodes must be energy efficient as battery power is limited and recharging/replacing batteries is usually not practical.

As illustrated in Fig. 1.3, each sensor node consists of a transducer that transforms electrical energy to mechanical energy (sound) or can convert sound energy at the receiver back to electrical energy. A sensor node requires a power stage to amplify signals before physical transmission and is usually the most power-hungry component of any transmission system. **Therefore the design and associated challenges of an energy efficient amplifier for USN is the subject of interest in this thesis.**

Figure 1.3: A typical illustration of an underwater sensor node

1.3 Amplifier Design Challenges

The design specifications of a power amplifier for underwater communication are influenced by the application area, type of acoustic transducer (load), usable bandwidth, distortion, and power efficiency requirements. These requirements will be discussed here briefly.

1.3.1 Bandwidth

The path loss of a signal in an acoustic channel is not only dependent on distance but also on signal frequency. Frequency selection is influenced by absorption loss and therefore affects the channel capacity with respect to distance [7]. The absorption of sound waves with respect to frequency in seawater can be determined by an empirical equation of the absorption coefficient given by Thorp's formula [8, 9]. Fig. 1.4 shows a plot of absorption of sound in seawater for frequencies up to 200 kHz. The second most im-

Figure 1.4: Absorption coefficient in seawater using Thorp's formula [9]

portant criterion in the selection of the frequency band is the ambient noise. The noise in the ocean can be modeled by considering the four significant sources of noise: shipping, turbulence, waves, and thermal noise [7, 9]. Fig. 1.5, shows the ambient noise spectrum for different combinations of wind speed and shipping activity levels. The minimum noise region occurs in the range of 20 – 200 kHz, and at higher frequencies, the noise starts to increase again. On the other hand the lowest absorption occurs below 50 kHz as shown in Fig. 1.4. Based on the above observations, it can be deduced that the optimal bandwidth for the sound generation for short to medium range USNs is up to 30 kHz [9].

Figure 1.5: Ambient noise PSD for different combinations of wind speed (w_n) and shipping noise (s_n) [9]

1.3.2 Linearity

In applications involving underwater communication, the maximum distortion requirement of the amplifier depends on the application and environmental factors. These include high noise from ships and waves, as well as time-varying channel characteristics that include frequency dependent attenuation, dispersion, Doppler effects and severe multi-path caused by the seabed and temperature gradients. Therefore the achieved linearity finally limits the choice of modulation schemes that can be used.

1.3.3 Power Efficiency

In an application such as underwater wireless monitoring, with a battery powered USN node, the requirement of output power for the amplifier can change drastically from low to high power levels and vice versa. This is due to the fact that each sensor node can drift and the distance from one node to the other can be variable. Therefore in order to improve battery life, the amplifier must be power efficient over a wide range of output power levels.

1.3.4 Piezoelectric Load

Piezoelectric transducers are best suited for an underwater sound generation because of their superior electro-acoustic efficiency [10]. They are

available in a wide variety of frequencies and sizes. Electrically, they behave capacitive, with a resistive component that is only present at frequencies where there is good coupling with the water and power transfer occurs.

The use of piezoelectric transducers as a load to an amplifier possess two major challenges. The first challenge in driving such transducers is related to the supply voltage. This is because for effective actuation of such transducers, high driving voltages are required (in the order of 10's to 100's of volts). With these battery-powered nodes having limited supply voltage, the requirement of the high voltage for piezoelectric transducers necessitates the use of supply-boosting techniques. The second challenge associated with driving piezoelectric transducers is due to the capacitive nature of these devices, which has a significant impact on the amplifier topology and control techniques, as not all the amplifiers can deal with reactive power transfer efficiently.

1.4 Research Objectives & Thesis Outline

1.4.1 Research Objectives

As discussed earlier, the design of an amplifier for USN with capability of driving piezoelectric transducer poses some unique challenges. However how to achieve this signal generation in an efficient way and what optimizations are needed has not been discussed clearly in literature.

Therefore the focus of this research is to realize a new power-efficient integrated amplifier for capacitive loads that can generate high output voltage signals despite having limited battery supply. Also, relevant control schemes need to be investigated that can handle such capacitive loads, keeping the distortion levels within a comparable range to state of the art solutions.

1.4.2 Thesis Outline

The rest of the thesis is organized as follows. An overview of a literature review of different approaches for driving piezoelectric transducers

is presented in chapter 2. Existing amplifier topologies and the related control schemes are discussed with issues related to linearity, efficiency, supply boosting, and stability. Specifically Peak Current Mode Control (PCMC) based scheme is discussed, as it provides superior performance over traditional control schemes.

In order to drive piezoelectric transducers, the amplifier design involves an accurate prediction of control loop characteristics. Therefore, in chapter 3, a new generic improved modeling technique is proposed that is applied to PCMC based boost converter for driving piezoelectric transducers. The improved modeling scheme is unique in the sense that it gives accurate modeling methodology that can be applied to both resistive as well as a capacitive load for a boosted switching amplifier.

In chapter 4, the modeling approach presented in chapter 3 is further extended to accurately predict feedback loop characteristics for all basic switching amplifiers with PCMC based topologies (buck, boost, and buck-boost) with prime focus on driving capacitive loads.

A new prototype for a power efficient boosting amplifier topology for piezoelectric transducers is proposed in Chapter 5. The design choices of the control loop along with implementation in 0.25 μm 60V TSMC process with an external power stage are discussed. Also, the relevant measurements of the implemented amplifier are compared to state of the art topologies.

A summary of this work with main conclusions is presented in chapter 6, with a list of original contributions and recommendations for future work.

A REVIEW OF AMPLIFIERS FOR PIEZOELECTRIC LOADS

Parts of Section 2.3.1, 2.3.2 and 2.4 in this chapter are taken from the author's paper published in IEEE Journal of Solid-State Circuits [11]¹.

2.1 Introduction

As discussed briefly in chapter 1, driving piezoelectric transducers for USNs poses some unique challenges. Therefore it is important to discuss in detail different amplifier topologies that are capable of efficiently processing reactive power and can handle high output voltage swing with good linearity.

The purpose of this chapter is to provide an overview of the state-of-the-art within the area of amplifiers and control schemes for piezoelectric transducers. For each topology aspects related to linearity, efficiency, high voltage swing and bandwidth are investigated along with the limitations of practical realizations of such amplifiers. As compared to some other architectures (like resonant amplifiers), the major requirement for the target

¹The 1st and 4th paragraph of Section 2.3.1, the 3rd, 5th and 6th paragraph of section 2.3.2 and the 2nd till 4th paragraph of section 2.4 are included from section 1 (introduction) of the paper.

application is to achieve a wide bandwidth of 0-30kHz and high signal swing at the output [7].

2.2 Linear Amplifiers

In the early years of development, linear amplifiers dominated the area of sound generation and capacitive actuation because these topologies have some distinct advantages, e.g. high linearity, simple implementation and low electromagnetic interference. Linear amplifiers, including class A, B, and class AB can be used to generate ac signals for piezoelectric transducers [12].

In Fig. 2.1, a typical class-B amplifier stage is shown. As compared to a class A topology with a maximum theoretical efficiency of 50% for a full scale sinewave in a resistive load, class-B amplifiers exhibit a maximum efficiency of 78.5%. This is because the two output transistors conduct alternatively to avoid quiescent current flow from the supply. However, this topology inherently dissipates as a voltage drop still occurs at the output transistors during the conduction phase. Several linear amplifiers for capacitive loads have been reported in literature [12–15]. As explained in [16], the class-B amplifier theoretical maximum efficiency (considering reactive output power) drops to 44% driving a capacitive load as compared to 78.5% of one driving a resistive load. The reduced efficiency is the result of the phase shift between load voltage and current for a capacitive load. The peak output current occurs at $V_{\text{out}} = 0$; therefore, more drop occurs across the transistors than in the resistive load case where maximum output current occurs at lowest drop voltage across the transistors. In [15], an improved class-B amplifier is presented that uses a capacitive buffer between the load and power stage. Although the proposed amplifier improves the power efficiency of the class-B stage by making charge recovery and reuse mechanism more efficient, the achieved efficiency of the amplifier is still quite low.

Also for signals that have a high peak-to-average ratio, like Orthogonal Frequency-Division Multiplexing (OFDM) and Quadrature Amplitude Modulation (QAM) modulated signals, the efficiency of the class-B am-

Figure 2.1: Basic class-B output stage with capacitive load

plifier further degrades as the average voltage drop across the output transistors becomes large due to the large peak-to-average ratio of the signals. One of the ways to improve efficiency, in this case, is to have an amplifier that tunes the supply voltage adaptively. This can be done with a class-G amplifier [17], as shown in Fig. 2.2. The advantage of this topology is that the amplifier is capable of switching between multiple supplies based on instantaneous signal amplitude. Although this helps to improve efficiency at low output signal levels, the output transistors still have a large V-I overlap due to the continuous conduction nature of the basic class-B stage. Also, the addition of multiple supplies is not a trivial task, and the implementation becomes more complicated due to the complex switching of supplies.

Even though above mentioned linear amplifiers are good candidates for signal generation due to the lowest distortion, the inherently low effi-

Figure 2.2: Concept of class-G amplifier with multiple supplies with capacitive load

ciency of these topologies makes them less suitable for battery powered applications.

2.3 Switching Amplifiers

An attractive alternative for driving piezoelectric transducers to linear amplifiers are switching amplifier topologies. This is because the switching topologies have been able to demonstrate very high efficiency, small size and distortion levels comparable to those of linear amplifiers. A variety of switch mode architectures are used to actuate piezoelectric elements, such as buck (class-D), boost and buck-boost. In this section, the advantages and disadvantages of these architectures are discussed in detail.

2.3.1 Class-D Amplifier

Over the years, class-D amplifiers (a buck-type converter) have slowly taken over the area of sound generation because of their high-efficiency

[18, 19]. Fig. 2.3, shows a typical class-D amplifier. The modulator converts the input signal into a high-frequency Pulse Width Modulated (PWM) signal, the output power stage then amplifies this high-frequency PWM signal at the output. However, in order to filter out the high-frequency PWM signal and retrieve the amplified low-frequency input signal, an LC filter is used, before the load.

Figure 2.3: Concept of class-D amplifier with a resistive load

Ideally, if the output switching transitions are infinitely fast with ideal switches, no V-I overlap occurs, resulting in a theoretical maximum efficiency of 100%. Another advantage of this topology is that, quasi-statically, the output voltage is a linear function of duty ratio (D); hence, the amplifier is also very suitable for low distortion applications. The amplifier often uses a feedback scheme (not shown) to reduce the distortion caused by non idealities like non-ideal PWM, delays, dead time and supply voltage variations.

For audio and capacitive actuation, a single stage class-D has been widely used. [16, 18, 20–32]. This is due to the fact that this topology offers superior efficiency by switching and limiting the loss associated with the circulating reactive power of the capacitive load.

Despite these advantages, the class-D topology has its own limitations. The maximum signal swing in a class-D amplifier is limited to the supply voltage and hence cannot effectively drive the piezoelectric transducer

with the limited battery voltage. This task is usually achieved by a two-stage solution, normally with a class-D amplifier for the generation of the dynamic signal and a dc-dc boost converter to increase the supply voltage of the class-D stage. Hence the total efficiency of the complete amplifier is lowered by the boost converter efficiency.

2.3.2 Voltage Boosting Amplifiers

Compared to linear and class-D amplifiers with an additional boost converter, if the signal generation and the boosting can be performed in a single stage, the overall efficiency can be improved with a lower number of components. In addition, to handle the capacitive loads and improve the overall efficiency, it is also necessary to recycle the stored reactive energy to a power source. The bidirectional boost and buck-boost topologies can achieve this task and hence fall in the category of boosting amplifiers.

A typical boosting amplifier can be viewed as a boost converter with time varying control signal and is illustrated in Fig. 2.4. When M_{LS} is on, the inductor L is charged from the supply. Turning off M_{LS} , the output voltage is boosted by discharging energy from L and supply into the output load via M_{HS} . Similar to the operation of class-D, the boosting

Figure 2.4: Concept of boosting amplifier with resistive load

amplifier reconstructs the output signal by filtering the high frequency PWM signal. However, the peak output signal is not any more limited

to the supply voltage; this makes boosting topologies most attractive for piezoelectric transducers with limited battery voltage. Additionally, the amplifier provides excellent efficiency, like class-D, due to the switching nature.

Despite the efficiency and supply boosting advantage, boosting amplifiers have not gained significant popularity in direct signal generation in audio applications. The major disadvantage is that the output voltage is a highly non-linear function of D , resulting in linearity degradation. In addition the presence of a Right-Half Plane Zero (RHPZ) for resistive loads, can result in limited bandwidth and high distortion at the output.

Since the application in focus is signal generation for piezoelectric transducers used for underwater acoustic communication, the choice of a boosting amplifier as a single stage solution could provide a two fold advantage. Firstly the RHPZ is present at much higher frequencies for capacitive loads [33], resulting in high bandwidth. Secondly, as the distortion requirement in underwater communication is less critical compared to audio applications, achieving acceptable linearity with improved efficiency can be advantageous. Therefore, next we discuss some of the methods described in literature that can be used to improve the linearity of a boosting amplifier.

Several techniques have been developed in literature make boosting amplifiers suitable for audio reproduction [34–44]. In [34–36], a boosting amplifier is proposed that uses two complementarily boost converters with the load connected differentially as shown in Fig. 2.5. Although the cancellation of the second harmonic improves distortion, Total Harmonic Distortion (THD) still remains relatively high.

The concept of pre-distortion is yet another method, which works by compensating the non-linear parts of the transfer function in such a way that the complete signal transfer becomes linear [38–41]. Since the effectiveness of pre-distortion is dependent on the cancellation of the non-linear parts of the transfer function, dynamic cancellation becomes challenging and often may require periodic calibration leading to more complexity. An interesting approach described in [44], uses a bidirectional

Figure 2.5: Concept of bridge-boosting amplifier with capacitive load

boost converter in combination with full-bridge to achieve high output voltage swing for a piezo actuator. The system is designed for very low bandwidth and output power, however.

Almost all the amplifiers have some form of feedback scheme to correct for errors. These dedicated feedback schemes for boosting amplifiers that can help improve linearity are briefly discussed next.

2.4 Feedback Control Strategies

The choice of feedback scheme determines the transient behaviour of the amplifier. At present, many of the amplifiers driving piezoelectric actuators adopt Voltage Mode Control (VMC), because of its simplicity. A typical VMC for a boosting amplifier is shown in Fig. 2.6. The control scheme uses a single voltage loop to track the input signal and generates a control voltage for the modulator. However, there are two major disadvantages of VMC when applied to a boosting amplifier. First, it is very difficult to achieve good stability over wide range of duty ratios. This is because the VMC sees both the inductor and output capacitor in the loop making the system second-order. Second, since the system is second-order, the achievable loop gain and position of poles/zeros depends heavily on D , as illustrated in Fig. 2.7 [45]. Hence in order to use VMC for a boosting amplifier with

full range of output swing, the amplifier's gain and bandwidth must be limited, resulting in degraded linearity.

Figure 2.6: A typical illustration of VMC of a boosting amplifier

Compared to traditional VMC, hysteretic voltage mode control is popular in buck based converters due to its fast transient response and simplicity [31]. However, this technique cannot be directly applied to boost converters due to the inherent phase difference between the output voltage and inductor current [46].

In comparison to VMC, PCMC, as shown in Fig. 2.8, uses an additional current feedback loop. This makes the system dominantly first order and thus results in simpler compensation, more bandwidth, and cycle by cycle current monitoring [47].

However, one of the major problem with peak or valley Current Mode Control (CMC) is the unstable subharmonic oscillations occurring when the $D > 0.5$. In order to reduce this effect, a fixed artificial slope M_a can be

Figure 2.7: A typical illustration of the loop gain dynamics of VMC of a boosting amplifier [45]

subtracted from the control signal. Fixed slope compensation makes the system stable within a limited range of duty cycles, as less slope compensation can lead to instability, and excessive slope compensation reduces the loop gain and makes the system approach VMC operation. Hence, to achieve good performance over wide duty cycle operation, complex adaptive slope compensation techniques depending on circuit components are required [48, 49].

Apart from the challenges mentioned above, PCMC is still a good candidate for boosting amplifiers. This is because current mode control can provide several advantages over voltage mode control in terms of good stability, higher bandwidth and loopgain. However, proper modeling of current mode control for capacitive loads needs yet to be investigated. Therefore in chapter 3 and 4, more focus is applied in discussing the methods and results of control loop modeling for boosting amplifiers especially applied to piezoelectric loads.

2.5 Conclusions

The application area for this thesis focuses on amplifiers for piezoelectric transducers used for underwater communication that are operated with limited battery voltage. In this chapter we have discussed various implementations and state-of-the-art solutions for amplifier topologies in

Figure 2.8: A typical illustration of PCMC of a boosting amplifier

driving piezoelectric loads. Linear amplifiers have the ability to provide excellent linearity however, the achieved efficiency is the main drawback. Class-D amplifiers are well suited for this application in terms of efficiency, however generation of high voltage signal from the limited supply can only be achieved at the cost of more complexity and degraded efficiency.

Boosting amplifiers are promising for this application because they can achieve boosting and signal generation combined in a single stage. This can potentially achieve better efficiency with limited voltage supply. In addition, the appropriate control scheme needs to be considered in order to achieve signal generation with acceptable distortion in boosting amplifiers. Compared to VMC, PCMC can achieve superior performance, but the behaviour with capacitive loads needs more attention. Therefore the next chapters take a more in-depth look at this.

MODELING PEAK CURRENT MODE CONTROL FOR BOOSTING AMPLIFIERS

This chapter is taken from the author's paper published in the IEEE Transactions on Power Electronics [33]¹.

3.1 Introduction

In order to use a boost converter for signal generation, understanding the dynamics and stability of the system is a crucial step. Therefore in this chapter the focus is on analyzing and developing a new modeling technique that is useful in predicting an accurate open loop transfer characteristic for a boost converter that employs PCMC. Many techniques exist for modeling a PCMC based boost converter, however all these techniques focus on purely resistive loads and are not always accurate for a purely capacitive load.

As explained earlier in chapter 2, PCMC is a popular control technique for a boosting amplifier (and boost converters in general) due to the fast transient response, overload protection, accuracy and ease of compensation.

¹Only the first paragraph of this chapter is different from the first paragraph of the paper.

Figure 3.1: A peak current-mode control based bidirectional boost converter

Some of the previous modeling approaches have used exact discrete-time and sampled-data modeling techniques [64–71]. However, due to complicated results, they lack insight into simple converter parameters and therefore are difficult to interpret as a circuit designer. Another popular approach is to use continuous time-models [50–63]. These modeling tech-

niques use a common methodology in representation of the entire system, but differ mainly in representing the sampling effect and modulator gain. These modeling techniques give very accurate results for classical applications where the load is dominantly resistive and the output capacitor is large to get small ripple. In our case, however, we intend to use the boost converter as a signal generator, necessitating the use of a much smaller output capacitor to increase bandwidth. Furthermore, the piezoelectric load is dominantly capacitive ($R_L = \infty$ in Fig. 3.1). It will be shown that the existing models are less accurate in this case, which motivated us to develop a new model.

In order to get a highly accurate model of a boost converter for wide load variations (for both capacitive and resistive loads), an unambiguous and a simple approach is used here by analyzing the complete converter stage (including closed-current loop) in discrete-time domain and then convert it to continuous-time for better insight into circuit parameters. The new approach doesn't need to separately analyse the current loop and power stage; instead, the closed-current loop is analyzed with capturing the effect of the output voltage simultaneously.

The outline of this chapter is as follows: In Section 3.2, the limitations of existing modeling approaches are discussed in detail. A complete and accurate small-signal model from control-to-output voltage of a PCMC based boost converter with capacitive and resistive load is derived in section 3.3. Finally, the model is verified and compared with simulation and measurement results.

3.2 Limitations of Existing Modeling Approaches

To model switched-mode converters, in [50] the complete model is obtained by combining the low-frequency modulator model with a state-space average model of the power stage. This is an interesting technique due to its simplicity but lacks the accuracy to predict the current loop instability at high frequencies. The work proposed in [65] uses sampled-data modeling for the current loop and thus is able to predict the well-known subharmonic oscillations at high frequency. However this technique alone is too

complex to be used in practical design. A simplified switch model was proposed in [52] to model the switching power stage and an extension of this model to current-mode control is reported in [72]. This technique achieves good accuracy, but the drawback of using the PWM switch model and incorporating current-mode control makes the method complex and is generally not straightforward. The injected-absorbed current approach [73] is aimed at providing ease of design and analysis, but provides less accurate results.

A continuous-time model is proposed by Ridley in [55], with the combination of a sampled-data model for the inductor-current loop and a three-terminal switch model for the power stage. This model has been very popular and provides better accuracy than the earlier approaches for both low and high frequencies. The method in [55] lies at the basis of subsequent techniques presented by Tan in [54] and Bryant in [57]. Therefore, this technique is discussed in more detail here.

The circuit in Fig. 3.1 is represented as a block diagram with a closed current-loop [55] and is shown in Fig. 3.2. The power stage is modeled using the duty-to-output voltage transfer $G_{vd}(s)$ and duty-to-inductor current transfer $G_{id}(s)$. The inductor current is sensed and converted to a voltage by the sense block R_s . The sampling effect is represented by $H_e(s)$ and is inserted into the current feedback loop, where (F_m) represents the modulator gain. The effect of the changing output voltage on the current loop is modeled by including an extra feedback path from output to the control voltage defined as output voltage feed-forward gain (k_r) [55]. It should be noted that the signals and blocks in this block diagram represent the structure of the model rather than actual physical blocks. In this method, the first step is to calculate basic power stage functions $G_{vd}(s)$ and $G_{id}(s)$. These transfer functions can be calculated in different ways. We have used state-space averaging here to calculate the power stage transfer functions for a boost converter stage and the results are formulated as:

$$G_{vd} = \frac{\frac{V_{dd}}{R_L D'^2} (R_L^2 D'^2 - s R_L L)}{D'^2 R_L + sL + s^2 R_L LC} \quad (3.1)$$

Figure 3.2: Block diagram of the modeling approach for PCMC proposed by Ridley [55]

$$G_{id} = \frac{\frac{V_{dd}}{D'}(2 + sR_L C)}{D'^2 R_L + sL + s^2 R_L LC} \quad (3.2)$$

In the next step, the control-to-inductor current transfer function is obtained in discrete-time followed by conversion into continuous-time form and is represented as [55]:

$$F_h(s) = \frac{i_L(s)}{v_c(s)} = \frac{1}{R_s} \frac{1 + \alpha}{sT_s} \frac{e^{sT_s} - 1}{e^{sT_s} + \alpha} \quad (3.3)$$

where

$$\alpha = \frac{M_2 - M_c}{M_1 + M_c}$$

Where M_1 is the on time inductor current slope, M_2 is the off time inductor current slope, M_c is the slope of compensation ramp, T_s is the switching period and α defines the slope compensation effect. The same notation will be used for all subsequent derivations.

This model uses $H_e(s)$ to incorporate the high-frequency effects and it is calculated using (3.3) and is approximated as [55]:

$$H_e(s) \cong 1 + \frac{s}{\omega_n Q} + \frac{s^2}{\omega_n^2} \quad (3.4)$$

where

$$Q = \frac{-2}{\pi} \text{ and } \omega_n = \frac{\pi}{T_s}$$

Ridley [55] presents the modulator gain (F_m) and feed-forward gain k_r for the boost converter as:

$$F_m = \frac{1}{(M_1 + M_c)T_s}, \quad k_r = \frac{D'^2 T_s R_s}{2L} \quad (3.5)$$

Using the block diagram in Fig. 3.2, the final control-to-output transfer function using Ridley's model can be expressed as:

$$T_{co}(s) = \frac{F_m G_{vd}(s)}{1 + G_{id}(s)F_m R_s H_e(s) - k_r G_{vd}(s)F_m} \quad (3.6)$$

The final control-to-output transfer function in (3.6) can now be calculated using (3.1), (3.2), (3.4) and (3.5). A similar approach is also presented by Tan in [54], where a different modulator gain (F_{m1}) and the feed-forward gain k_{r1} is presented as:

$$F_{m1} = \frac{1}{M_c + \frac{(D'-D)V_{dd}}{2L} \left(1 + \frac{s}{\omega_p}\right) T_s}, \quad k_{r1} = \frac{DD'T_s}{2L} \quad (3.7)$$

$$\omega_p = \frac{\omega_n}{Q} \quad (3.8)$$

$$Q = \frac{1}{\pi(m_c D' - 0.5)} \quad (3.9)$$

$$m_c = 1 + \frac{M_c}{M_1} \quad (3.10)$$

The major difference between [55] and [54] is the way the modulator gain, feed-forward gain and the high-frequency extension is modeled. The first one uses $H_e(s)$ and the other adds an extra pole in the modulator gain (F_{m1}). Hence Tan's model doesn't consider the sampling effect $H_e(s)$ as a separate block in feedback, but rather combines it within the modulator gain. The third popular approach similar to Tan's model is presented by Bryant in [57], where the modulator gain F_{m2} is calculated by using a closed current-loop and the feed-forward gain is ignored in this approach. The

modulator gain calculated by Bryant includes the sampling effect within the loop and is presented as:

$$F_{m2} = \frac{1}{G_{id} R_s \left(\frac{s T_s}{1+\alpha} \frac{e^{sT_s} + \alpha}{e^{sT_s} - 1} - 1 \right)}, \quad k_{r2} = 0 \quad (3.11)$$

In order to verify all of the models presented in [54, 55, 57], the models are derived using (3.6) with their respective modulator gains (F_m, F_{m1}, F_{m2}) and feed-forward gains (k_r, k_{r1}, k_{r2}), and the results are compared in Fig. 3.3 with SIMPLIS simulation. The circuit parameters listed in Table 3.1 are used with the output capacitance (C) and output resistance (R_L) to represent a typical application using a resistive load. It is interesting to note that

Table 3.1: Circuit parameters

Parameters	Values
Duty ratio (D)	0.5
Slope compensation factor (m_c)	1.66
Compensating slope (M_c)	24mV/ μ s
On time inductor current sense slope (M_1)	36mV/ μ s
Inductor (L)	100 μ H
Current sense gain ($R_s = R_i \cdot A_i$)	50 m Ω *6
Supply voltage (V_{dd})	12V
Switching frequency (f_s)	1MHz
Resistive load ($R_L \parallel C$)	(50 m $\Omega \parallel$ 10 μ F)
Capacitive load ($R_L = \infty \parallel C$)	26nF
Control voltage for capacitive load (V_c)	20mV
Control voltage for resistive load (V_c)	300mV

the results shown in Fig. 3.3 are indeed very accurate and match well with the simulation results for all the models. To validate the models in [54, 55, 57] for a capacitive load, the output load in the circuit in Fig. 3.1 is replaced by a purely capacitive load ($R_L \rightarrow \infty$). The static capacitance of the piezo actuator dominates at most frequencies, so a simple capacitor is a fairly accurate representation. Also the value of C is decreased to get sufficient bandwidth (see Table 3.1) and the simulation results are re-evaluated following the same steps as mentioned before. The results are plotted in Fig. 3.4.

The results shown in Fig. 3.4 are not very accurate for low frequencies for Tan's model compared to the simulation, whereas Bryant's model misses the low frequency pole completely. The simulation results for low

Figure 3.3: Comparison of the Ridley [55], Tan [54] and Bryant [57] models control-to-output transfer $T_{co}(s)$ with SIMPLIS simulation for a PCMC boost converter with resistive load ($50 \text{ m}\Omega || 10 \mu\text{F}$).

Figure 3.4: Comparison of the Ridley [55], Tan [54] and Bryant [57] models control-to-output transfer $T_{co}(s)$ with SIMPLIS simulation for a PCMC boost converter with capacitive load (26 nF).

frequency behaviour predicted by Ridley's model is indeed accurate but shows a 15 degree phase deviation at $f_s/2$ as compared to simulation results. In traditional applications, indeed, the difference at low frequency doesn't drastically affect the overall system design, as they are designed for DC operation only. However, in order to generate dynamically varying signals, like in our case, a more accurate model is important due to the wide variation in duty ratio.

The reason for the deviations between models and simulation can be explained by the choice of different modulator gain F_m , which is a block in a feedback system (Fig. 3.2) of which the behaviour depends on the closed loop itself. Therefore it is not as much calculated as selected in [54, 55] allowing for contradictory expressions. In [57], F_m is calculated from the closed loop, but the result is even less accurate as shown above. Therefore it should be noted that the accuracy of these models depends greatly on the way the modulator gain F_m , the gain term k_r and the sampling effect $H_e(s)$ are defined. The inconsistency in these definitions makes the above mentioned methods less attractive. In addition, all of these approaches require the derivation of many blocks, namely F_m , k_r , $G_{vd}(s)$, $G_{id}(s)$ and $H_e(s)$. As an alternative, we present a modeling technique that uses a much more straightforward analysis and provides highly accurate results for both capacitive and resistive loads for both high and low frequencies.

3.3 Small-Signal Analysis

The complete small-signal model of a PCMC based boost converter consists of the power stage and the closed current-loop. Therefore as a first step, the power stage and the closed current-loop are simultaneously modeled by using a discrete-time approach in subsection I. The resultant discrete-time model is then converted to the continuous-time domain for clear insight into different circuit parameters in subsection II.

3.3.1 Discrete-time State Space Modeling

This section derives the control-to-output (T_{co}) transfer function of the PCMC based boost converter for a generic load ($R_L \parallel C$) using discrete-time analysis. The process of determining the transfer function starts with

Figure 3.5: A closed-current loop PCMC based boost converter with RC ($R_L \parallel C$) load

the inspection of the relevant waveforms of the circuit shown in Fig. 3.5. The time-domain waveforms of the PCMC based converter are shown in Fig. 3.6a, where $R_s i_L$ is a measure for the sensed inductor current and M_1 and M_2 are the sensed inductor current on-time and off-time slopes respectively. In order to dampen the subharmonic oscillations and have a stable operation, a compensating slope M_c is required. Adding slope compensation to the current signal is equivalent to subtracting a slope from the control voltage v_C . The control voltage v_C in combination with the compensating ramp determines the peak inductor current i_{Lp} .

For the discrete-time analysis, the clock signal initiates each switching cycle at $T(n)$ with switching period T_s divided into on-time t_1 and off-time t_2 as shown in Fig. 3.6b.

The difference equations representing the state variables inductor current

(a) Continuous-time domain converter waveform for PCMC

(b) Continuous-time to discrete-time domain representation

Figure 3.6: Converter waveforms for PCMC with continuous-time and sampled discrete-time at clock $T(n)$.

(i_L) and output voltage (v_O) can be formulated from the geometry of the sensed current waveforms in Fig. 3.6b. The difference equation representing the discrete-time inductor current i_L at sampling instant $T(n+1)$ can be written as:

$$i_L(n+1) = \frac{R_s i_{LP}(n) - M_2 t_2}{R_s} \quad (3.12)$$

The difference equation representing the discrete-time output voltage $v_O(n+1)$, can be represented as the sum of the previous output voltage $v_O(n)$ at sampling instant $(T(n))$ and the voltage difference due to the flow of charge in the output capacitor. This charge consists of the charge supplied by the inductor during t_2 and the charge drained by the load resistance during the full switching cycle. The current during t_2 is the average current of $i_{LP}(n)$ and $i_L(n+1)$ and hence the output voltage can

be expressed as:

$$v_O(n+1) = v_O(n) + \frac{(i_{LP}(n) + i_L(n+1))t_2}{2C} - \frac{v_O(n)T_s}{R_L C} \quad (3.13)$$

In (3.12) and (3.13), it is easy to see from Fig. 3.6b that:

$$R_s i_{LP}(n) = R_s i_L(n) + t_1 M_1$$

$$t_1 = \frac{v_C(n) - R_s i_L(n)}{M_1 + M_c}$$

$$t_2 = T_s - t_1,$$

Also, from the power stage as shown in Fig. 3.5 we know that:

$$M_1 = \frac{V_{dd} R_s}{L}, \quad M_2 = \frac{(v_O - V_{dd}) R_s}{L},$$

$$D' = 1 - D$$

Where D represents the duty ratio and V_{dd} is the supply voltage. In order to construct the small-signal model, (3.12) and (3.13) are first written as a function of only $i_L(n)$, $v_C(n)$ and $v_O(n)$ as:

$$i_L(n+1) = i_L(n) - \frac{(v_O(n) - V_{dd})T_s}{L} + (v_C(n) - i_L(n)R_s)K_1 \quad (3.14)$$

where

$$K_1 = \frac{M_1 + M_2}{R_s(M_1 + M_c)}$$

$$v_O(n+1) = v_O(n) + \frac{R_s i_L(n) + M_1 t_1 + R_s i_L(n+1)}{2R_s C} \cdot t_2 - K_2 \quad (3.15)$$

where

$$K_2 = \frac{v_O(n)T_s}{R_L C}$$

The next step involves perturbation around the steady state point which is done by applying the following substitutions:

$$i_L(n+1) \rightarrow I_L(n+1) + i_l(n+1) \quad (3.16)$$

$$i_L(n) \rightarrow I_L(n) + i_l(n) \quad (3.17)$$

$$v_C(n) \rightarrow V_C(n) + v_c(n) \quad (3.18)$$

$$v_O(n) \rightarrow V_O(n) + v_o(n) \quad (3.19)$$

$$v_O(n+1) \rightarrow V_O(n+1) + v_o(n+1) \quad (3.20)$$

Where $I_L(n+1)$, $I_L(n)$, $V_C(n)$, $V_O(n)$ and $V_O(n+1)$ are the DC steady state terms. By substitution of (3.16), (3.17), (3.18), (3.19) and (3.20) in (3.14) and (3.15) the DC, first and second order terms are obtained. For the small-signal derivation the DC terms are cancelled and the second order terms are ignored, which results in the following simplified small-signal difference equation:

$$i_L(n+1) = -i_L(n)k_0 - v_o(n)k_1 + v_c(n)k_2 \quad (3.21)$$

$$v_o(n+1) = i_L(n)k_3 + v_o(n)k_4 + v_c(n)k_5 \quad (3.22)$$

where

$$\begin{aligned} k_0 &= \alpha = \frac{M_2 - M_c}{M_1 + M_c} \\ k_1 &= \frac{(1-D)T_s}{L}, k_2 = \frac{V_{dd}}{(1-D)L(M_1 + M_c)} \\ k_3 &= -\frac{\alpha D' T_s}{C} + \frac{M_1 L}{C(M_1 + M_c)R_L D'^2} + \frac{M_1(D)T_s}{2C(M_1 + M_c)} \\ k_4 &= 1 - \frac{D'^2 T_s^2}{2CL} - \frac{T_s}{R_L C} \\ k_5 &= \frac{V_{dd} T_s (1 - 0.5D)}{CL(M_1 + M_c)} - \frac{V_{dd}}{C(M_1 + M_c)R_L D'^2} \end{aligned}$$

Equation (3.21) and (3.22) are the fundamental equations for the PCMC based boost converter and can be now easily converted to a state-space representation.

The independent states (i_L and v_o) in the circuit contribute to the state vector $\mathbf{x}[n]$ and the independent input source (v_c) to the input vector $\mathbf{u}[n]$. Hence the general state-space model of a PCMC based boost converter can be represented as:

$$\mathbf{x}[n+1] = \mathbf{A}\mathbf{x}[n] + \mathbf{B}\mathbf{u}[n] \quad (3.23)$$

where

$$\mathbf{u}[n] = v_c(n), \quad \mathbf{x}[n] = \begin{bmatrix} i_l(n) \\ v_o(n) \end{bmatrix}$$

$$A = \begin{bmatrix} -k_0 & -k_1 \\ k_3 & k_4 \end{bmatrix}, \quad B = \begin{bmatrix} k_2 \\ k_5 \end{bmatrix}$$

(3.23) is a complete state-space representation of the circuit and the control-to-output transfer function can be found by taking the Z-transform:

$$z\mathbf{x}(z) = A\mathbf{x}(z) + B\mathbf{u}(z) \quad (3.24)$$

rearranging we get,

$$\frac{\mathbf{x}(z)}{\mathbf{u}(z)} = (zI - A)^{-1}B \quad (3.25)$$

Where I is the identity matrix. Substituting the matrices of A and B in (3.25) and rearranging the terms, the control-to-output discrete-time transfer function $T_{co}(z)$ can be written as:

$$T_{co}(z) = \frac{v_o(z)}{v_c(z)} = G_0 \frac{a_4 z + a_3}{a_2 z^2 + a_1 z + a_0} \quad (3.26)$$

where

$$G_0 = \frac{-V_{dd}}{D'^2(M_1 + M_c)}$$

$$a_4 = 2L(M_1 + M_c)D' + (M_1 + M_c)R_L(-2 + D)T_s D'^3$$

$$a_3 = (\alpha(M_1 + M_c)D' - M_1) \left(R_L T_s D'^2(D) + 2L \right)$$

$$a_2 = 2CD'LR_L(M_1 + M_c)$$

$$a_1 = 2D' \left((C(\alpha - 1)L + \frac{T_s^2 D'^2}{2})R_L + LT_s \right) (M_1 + M_c)$$

$$a_0 = -\alpha R_L T_s^2 (M_1 + M_c) D'^3 + D'^2(D) R_L T_s^2 M_1$$

$$-2\alpha(M_1 + M_c)L(-T_s + CR_L)D' + 2LT_s M_1$$

3.3.2 Continuous-time Domain Representation

Equation (3.26) gives an accurate system representation in discrete-time domain and can be very helpful in making digital control circuits. However, for better insight into how different circuit parameters influence the behaviour of the transfer function, a continuous-time representation can be

very helpful. Therefore in this section, (3.26) is converted to continuous-time using a second-order Padé approximation of $z = e^{sT_s}$. A first-order approximation of e^{sT_s} would not change the number of poles, and would not be able to translate the left half plane z -domain pole that describes the ringing around $f_s/2$ [74].

$$z = e^{sT_s} \approx \frac{s^2 + 6f_s s + 12f_s^2}{s^2 - 6f_s s + 12f_s^2}, \quad (T_s = \frac{1}{f_s}) \quad (3.27)$$

Putting (3.27) in (3.26), the continuous-time domain control-to-output transfer function $T_{co}(s)$ results in a fourth-order function with the form of:

$$T_{co}(s) = \frac{q_4 s^4 + q_3 s^3 + q_2 s^2 + q_1 s + q_0}{p_4 s^4 + p_3 s^3 + p_2 s^2 + p_1 s + p_0} \quad (3.28)$$

The coefficients of (3.28) can be simplified by using the following assumptions:

$$f_s \gg \frac{1}{2\pi R_L C} \quad (3.29)$$

$$f_s \gg \frac{1}{2\pi\sqrt{LC}} \quad (3.30)$$

This means that the switching frequency is higher than the $R_L C$ and LC frequency of the power stage. This will generally be true to achieve an acceptable ripple, so (3.28) can be rewritten as:

$$T_{co}(s) = \frac{k' (c_4 s^4 + c_3 s^3 + c_2 s^2 + c_1 s + c_0)}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad (3.31)$$

where

$$k' = -2V_{dd}$$

$$c_4 = -T_s^4 D'^2 R_L$$

$$c_3 = 6 D'^2 D R_L T_s^3 + 12 L T_s^2$$

$$c_2 = -72 T_s \left(\frac{1}{2} R_L (-1/3 + D) D'^2 T_s + L \right)$$

$$c_1 = 144 L + 72 R_L D'^2 T_s D$$

$$c_0 = -144 D'^2 R_L$$

$$b_4 = 2 T_s^4 \left(\frac{D'^3 R_L T_s (M_1 + M_c)}{2} + \right.$$

$$LD'(1 + \alpha)(M_1 + M_c) + LM_1$$

$$b_3 = 24CD'LR_L T_s(M_1 + M_c)$$

$$b_2 = (1 - \alpha)(144CD'LR_L T_s(M_1 + M_c))$$

$$b_1 = (288CD'LR_L(1 + \alpha)(M_1 + M_c)) = 288V_{dd}R_sCR_L$$

$$b_0 = \frac{144T_s}{L}(D'^3R_L(V_{dd}R_s + 2M_cL) + 4LV_{dd}\frac{R_s}{T_s})$$

As can be seen in (3.31), the conversion to continuous-time results in extra poles and zeros. Often the transfer function contains many poles and zeros, having a single dominant pole or zero. Similarly for practical power converters to work, the dominant pole (ω_{p1}) needs to be at a much lower frequency than the other poles. Hence in this case, dominant pole approximation as explained in [75] is useful to extract the low frequency pole.

If a circuit has n number of poles and m number of zeros, the transfer function $T(s)$ can be expressed generally as:

$$T(s) = \frac{a_0 + a_1s + a_2s^2 + a_3s^3 + \dots + a_ms^m}{b_0 + b_1s + b_2s^2 + b_3s^3 + \dots + b_ns^n} \quad (3.32)$$

If a system represented by (3.32) is known to have a dominant pole located at much lower frequency than the other $(n-1)$ poles, the higher frequency poles are neglected at lower frequencies, resulting in a first order transfer function. Then, the dominant pole in (3.31) can be calculated as:

$$\omega_{p1} = \frac{b_0}{b_1}, \text{ where } \omega_{p1} \ll \omega_{p2}, \omega_{p3}, \dots \quad (3.33)$$

At higher frequencies, b_1s then dominates b_0 , so the complexity of the denominator in (3.31) can be reduced. The same technique is used on the numerator of (3.31) to extract the dominant zero. Subsequently, poles and zeros above $\frac{f_s}{2}$ are neglected, which leads to the final form:

$$T_{co}(s) = G_0 \frac{1 - \frac{s}{\omega_{rhpz}}}{(1 + \frac{s}{\omega_p})(s^2 + 6f_s s \frac{(1-\alpha)}{(1+\alpha)} + 12f_s^2)} \quad (3.34)$$

where

$$G_0 = \frac{24Lf_s^3R_LD'V_{dd}}{D'^3R_LV_{dd}R_s + 2D'^3R_LM_cL + 4f_sLV_{dd}R_s}$$

$$\omega_{rhpz} = \frac{D'^2R_L}{L}$$

$$\omega_p = (1 - D)^3 \frac{\left(\frac{M_c}{M_1} + 0.5\right)}{LCf_s} + \frac{2}{R_L C}$$

Where G_0 is the DC gain, ω_{rhpz} is the right-half plane zero frequency, the second order term describes the subharmonic poles and ω_p is the dominant pole frequency. The model presented in (3.34) is not only comprehensible and accurate but can directly be applied to capacitive loads. So for a purely capacitive loads ($R_L \rightarrow \infty$) the second term of ω_p is zero, leaving:

$$\omega_p = (1 - D)^3 \frac{\left(\frac{M_c}{M_1} + 0.5\right)}{LCf_s} \quad (3.35)$$

3.4 Simulation Results

In order to validate the model in (3.34), the results are first compared to simulations in SIMPLIS with circuit parameters listed in Table 3.1.

A PCMC based boost converter running in CCM is simulated in SIMPLIS with an RC load ($R_L=50 \text{ m}\Omega$, $C = 10\mu\text{F}$) and other parameters as listed in Table 3.1, and the control-to-output transfer function is plotted in Fig. 3.7. The results from (3.34) match well with the simulation for both high and low frequencies. The same model is then used for a purely capac-

Figure 3.7: Control-to-output transfer $T_{co}(s)$ according to model (3.34) and SIMPLIS simulation for $R_L=50 \text{ m}\Omega$, $C=10\mu\text{F}$.

itive load ($R_L \rightarrow \infty$) and the results are compared with the simulations in SIMPLIS in Fig. 3.8. Again, the results match well with the simulation.

Figure 3.8: Control-to-output transfer $T_{co}(s)$ according to model (3.34) and SIMPLIS simulation for capacitive load ($R_L = \infty$, $C=26\text{nF}$).

Figure 3.9: Effect of duty cycle variation on the dominant pole location for a capacitive load

The dominant pole location in (3.34) is strongly influenced by the choice of duty cycle, considering other parameters remain constant. It is interesting to observe the effect of dominant pole movement for wide duty cycle variations as shown in Fig. 3.9. For purely capacitive loads, the dominant pole deviation is significant and cannot be ignored. In order to ensure the validity of these simulation and modeling results, the model is also verified by experimental verification for a capacitive load in the next section.

3.5 Experimental Verification

The experimental results for a PCMC based boost converter are only verified for a capacitive load due to the focus of the project involved. The simulation setup above demonstrates the real application area, however as the original circuit is not yet realised, an existing boost converter board is used to verify the model and simulation results. The schematic of the setup is shown in Fig. 3.10. The LM5122EVM-1PH synchronous boost controller

Figure 3.10: Measurement schematic of a peak current-mode control based bidirectional boost converter with capacitive load (370μF)

evaluation module (shown in Fig. 3.11) is used in Forced PWM mode for

these measurements along with a gain-phase analyzer (HP-4194A). The circuit parameters are listed in Table 3.2.

Figure 3.11: Modified LM5122EVM-1PH synchronous boost controller evaluation module

Table 3.2: Circuit parameters

Parameters	Values
Duty ratio (D)	0.5
Inductor (L)	10 μ H
Current sense gain($R_s = R_i \cdot A_i$)	4 m Ω *10
Supply voltage (V_{dd})	12V
Switching frequency (f_s)	250kHz
Control voltage (V_c)	168mV
Slope compensation (peak-peak)	270mV
Output capacitance (C)	370 μ F
Load resistance for capacitive load (R_L)	∞
Decoupling capacitor (C_d)	22nF
Input resistance (R_{in})	47 k Ω

A capacitor in a practical circuit has an Equivalent Series Resistance (ESR). For practical converters, the ESR of the capacitor is much smaller than the load resistance. Therefore the ESR of the capacitor only adds an extra zero in the transfer function and doesn't change the DC gain and the location of the dominant and subharmonic poles. Hence the capacitor's ESR was ignored in the main analysis as well as in Fig. 3.3 and 3.4. However for the experimental verification, ESR is present in the circuit and to validate

the effect of the ESR-zero, a small resistance of 55 m Ω is added to the capacitance in simulation and the results are shown in Fig. 3.12. Similarly, to accommodate the effect of ESR in the model, a real zero can be added to final model with the following expression:

$$\omega_{zero} = \frac{1}{R_{esr} \cdot C} \quad (3.36)$$

The experimental verification of the modeling is done using a testbed which is not designed to operate under such load (370 μ F) conditions. We used less output capacitance in order to be able to show the low frequency pole. As a result, the test board of the boost converter does not operate properly above $0.2f_s$ signal frequency. Although the board is originally designed to operate under wide duty ratio variation, reducing the output capacitor to a low value limits stable operation to around a duty ratio of 0.5. Therefore the measurements are only performed for a duty ratio of 0.5. The

Figure 3.12: Comparison control-to-output transfer $T_{co}(s)$ with simulation, measurement and model ($R_L \rightarrow \infty$).

results show that the model accurately predicts the DC gain, dominant pole and subharmonic poles. The measurement results of the control-to-output transfer function match well with the model at low frequencies, with some slight deviation at high frequencies, likely caused by measurement artifacts.

3.6 Conclusions

A new modeling approach to derive the control-to-output transfer function for peak current-mode controlled dc-dc boost converter operating in CCM is proposed. The main advantage of the proposed approach is its straightforwardness and accuracy. The power stage transfer including inductor current-to-output voltage and duty cycle-to-output voltage need not to be derived.

The location of the dominant pole and how it is affected by circuit parameters can help to design an accurate compensator, reduce static error and distortion at the output, especially in the case where the dominant pole moves to higher frequencies. With dynamic signals, the operating range of the duty cycle is significant and hence care must be taken for the design of slope compensation, selection of switching frequency and feedback compensation.

The control-to-output voltage transfer function derived here agrees very well with the simulation and measurement results. The modeling approach in this chapter concentrates on a PCMC based boost converter, but the method can also be applied to buck or buck-boost converter topologies.

EXTENSION OF THE MODELING TECHNIQUE TO BASIC PCMC SWITCHING CONVERTERS

The author would like to thank Mr. Tim van Doesum for his valuable contribution to this chapter, related to his master thesis work titled "Modeling of peak current-mode controlled power converters" performed at the University of Twente.

4.1 Introduction

The modeling approach presented in chapter 3 uses a discrete time modeling methodology that directly predicts the control-to-output transfer function of a PCMC based boost converter. The focus in chapter 3 was limited to a boost converter, however it is worth to investigate the applicability of the developed technique to other converter topologies as well.

Therefore as a first step, the same approach is used in this chapter for the buck converter to predict the control-to-output transfer function directly. However for the case of buck converter, as shall be explained later, the direct evaluation of control-to-output transfer function using discrete time modeling doesn't predict the complete transfer function accurately. In-

stead it is needed to first correctly calculate the control-to-inductor current transfer and then use it to develop the complete control-to-output voltage transfer function.

Hence the objective of this chapter is to extend the existing modeling technique previously developed to buck converter by applying necessary changes that result in an accurate model for all the basic converter topologies. Due to the focus of this thesis on capacitive loads, we assume all converters can handle a bidirectional output current and therefore work in CCM.

The outline of this chapter is as follows: In section 4.2, the limitations of existing modeling techniques are discussed. A complete small-signal model for the control-to-inductor current and control-to-output voltage of a PCMC based buck converter is derived in section 4.3. To verify the usefulness of the extended modeling approach, the technique is then applied to boost and buck-boost converters as well. Finally the models are compared with simulations and measurement results in section 4.4.

4.2 Limitations of Existing Modeling Technique

A PCMC based buck converter is shown in Fig. 4.1 as an example. The inductor current is sensed by R_i and A_i , such that the sense gain $R_s = A_i R_i$ is obtained. For compatibility with existing literature, the sensed inductor current $R_s i_L$ (which is actually a voltage) will be used in the remainder of this work to describe the inductor current behaviour. A compensating slope M_c is added to the sensed inductor current and the resulting signal is compared with the control voltage v_c to obtain the required PWM signal.

As a first step, the control-to-output transfer for the buck converter using the technique presented in chapter 3 is calculated. This calculation can be found in appendix A. The circuit is then first simulated using a resistive load. Fig. 4.2a shows a bode plot of the control-to-output voltage transfer function. The discrete-time model formulated, is compared with the SIMPLIS simulation.

In addition, the current loop of the circuit in Fig. 4.1 is also simulated in SIMPLIS, the parameters used for both the model and simulations are

Figure 4.1: PCMC based buck converter

Table 4.1: Circuit parameters for PCMC buck converter for resistive and capacitive load.

Parameters	Res load	Cap load
Duty ratio (D)	0.50	0.64
Compensating slope (M_c)	$0 \text{ mV } \mu\text{s}^{-1}$	$10 \text{ mV } \mu\text{s}^{-1}$
On time inductor current sense slope (M_1)	$15 \text{ mV } \mu\text{s}^{-1}$	$10.8 \text{ mV } \mu\text{s}^{-1}$
Inductor (L)	$100 \text{ } \mu\text{H}$	$100 \text{ } \mu\text{H}$
Current sense gain ($R_s = R_i \cdot A_i$)	$50 \text{ m}\Omega \times 6$	$50 \text{ m}\Omega \times 6$
Supply voltage (V_{dd})	10 V	10 V
Switching frequency (f_s)	1 MHz	1 MHz
Load ($R_L C$)	$10 \text{ } \Omega 100 \text{ } \mu\text{F}$	300 nF

listed in Table 4.1. The control-to-output voltage transfer model agrees with the simulation for low frequencies, but at high frequencies it deviates. The simulation predicts peaking around $f_s/2$ due to subharmonic oscillations, but the discrete-time model does not show peaking at all. However, the control-to-inductor current transfer function matches well with the simulation results. It must be noted that although operation like this, without compensating slope, is not desired under normal stable conditions, the subharmonic oscillations should be predicted by the model because they influence the phase margin of the overall voltage loop.

This discrepancy in the obtained discrete-time model for a buck converter can be explained using Fig. 4.3. When looking at Fig. 4.3b, it can

Figure 4.2: The control-to-output voltage transfer function in ((a)) and control-to-inductor current ((b)) are compared to SIMPLIS simulation for resistive load, using the values in Table 4.1.

be seen that the sample intervals correspond to the valley inductor current, and these show oscillatory behaviour. However, when looking at

Fig. 4.3c and 4.3d, it can be seen that the sampled intervals always describe the average output voltage. This is due to the fact that the system is under-sampled, which is a fundamental problem in the buck converter, and explains why the subharmonic oscillations do not show up in the control-to-output voltage transfer function.

Figure 4.3: Discrete and continuous-time waveforms for a buck converter in steady state ((a) and (c)) and for subharmonic oscillations ((b) and (d)) (shapes confirmed by simulation).

This is not the case for a boost converter which is modeled in chapter 3. The inductor current behaviour and correlated output voltage for a boost converter are shown in Fig. 4.4. From Fig. 4.4b and 4.4d it can be seen that the sampling intervals of both the inductor current and the output voltage do capture the effect of subharmonic oscillations.

Therefore for the case of buck converter it is necessary to first derive the control-to-inductor current transfer function accurately and use it to calculate the final control-to-output transfer function for both resistive and capacitive loads. The approaches used in [47, 60, 76–79] rely on deriving a z-domain expression for the control-to-inductor current transfer function

Figure 4.4: Discrete and continuous-time waveforms for a boost converter in steady state ((a) and (c)) and for subharmonic oscillations ((b) and (d)) (shapes confirmed by simulation)

which is expressed as:

$$\frac{i_l(z)}{v_c(z)} = \frac{1}{R_s} (1 + \alpha) \frac{z}{z + \alpha} \quad (4.1)$$

where $\alpha = (M_2 - M_c)/(M_1 + M_c)$, and M_1, M_2 are the sensed inductor current slopes and M_c is the compensating slope. This expression is universal for all basic PCMC based converter topologies. This z-domain transfer is then converted to the s-domain in different ways. The z-domain transfer function and resulting s-domain transfer functions are plotted in Fig. 4.5 for a capacitive load with values in Table 4.1 and compared to SIMPLIS simulation.

In addition, when applying the method described in chapter 3, to a PCMC buck converter, the resulting control-to-inductor current transfer function for capacitive load also deviates from the simulated graph as shown in Fig.4.5. The common problem is that the inductor current is under-sampled, since the z-domain sampling frequency is the same as the inductor current ripple frequency.

Figure 4.5: Control-to-inductor current transfer functions for a capacitively loaded buck converter, using circuit component values in Table 4.1.

Fig.4.6(a) shows the sensed inductor current waveform in case of steady state operation. The discrete-time descriptions that are used to obtain the control-to-inductor current transfer describe either the valley current ($i_L(n)$ and $i_L(n+1)$) [33, 47] or the peak current [78, 79]. Both descriptions differ considerably from the average current which is actually zero in case of a capacitive load, and this indicates why the low frequency behaviour is not predicted correctly.

To verify the problem, a sample-and-hold circuit is added to the simulation. This sample-and-hold causes the simulation to hold the signal of the valley inductor current. The results are shown in Fig. 4.7. The model agrees very well with the SIMPLIS simulation with sample-and-hold for capacitive load, verifying that the problem indeed comes from the sampled intervals coinciding with the valley current.

In order to accurately predict the current-loop transfer characteristics using an approach similar to the one described in chapter 3, a correct discrete-time description for both the average current and the subharmonic oscillations is required. The resulting z-domain transfer function can then be used to obtain continuous-time control-to-inductor current transfer,

which forms the basis of obtaining the final control-to-output voltage transfer function for the buck, boost and buck-boost converter topologies. These steps are explained in the next section.

4.3 Extended Modeling Approach

The first step uses a discrete-time based modeling approach based on chapter 3 to obtain the z-domain control-to-inductor current transfer and is explained in subsection I. To obtain a clear description of the relevant poles and zeros in terms of design parameters, the result from subsection I is converted to continuous-time in subsection II. Finally in subsection III, the control-to-output voltage transfer is obtained by multiplying the

Figure 4.7: The control-to-inductor current (A.34) is compared to SIMPLIS simulation for capacitive load, using the values in Table 4.1.

control-to-inductor current transfer with the inductor current-to-output voltage transfer.

4.3.1 Discrete-time State Space Modeling

Because the system is under-sampled, we first calculate the average current before sampling. However, calculating the average over T_s in Fig. 4.6(b) would average out any subharmonic oscillations, so the model would not be able to describe them. Therefore we introduce a fictional current i_F , as shown in Fig. 4.6. It must be noted that the addition of i_F to the converter is only done for the modeling purpose, in practical converters working with PCMC would not have this slope and therefore doesn't change any design parameters including the compensating slope M_c .

At the first sampling moment $t(n)$ it is equal to the average inductor current during T_1 , at the second ($t(n+1)$) it is equal to the average inductor current during T_2 . This is allowed because the average during $T_2(n)$ is roughly equal to the average during $T_1(n+1)$. A description of this fictional current i_F is found by looking at the geometry of Fig. 4.6, which can be

described as

$$R_s i_F(n+1) = R_s i_F(n) + \frac{1}{2} M_1 T_1 + \frac{1}{2} M_2 T_2, \quad (4.2)$$

where

$$T_1 = \frac{v_C(n) - R_s i_F(n)}{\frac{1}{2} M_1 + M_c}, \quad T_2 = T_s - T_1 \text{ with } T_s = \frac{1}{f_s}.$$

This description is similar to the one found in chapter 3, except now the sensed inductor current slopes M_1 and M_2 are only half as steep. In both cases, steady state and subharmonic oscillation, the average of the inductor current is now described accurately. However the amplitude of the subharmonic oscillation in Fig. 4.6(b), is only half as big for the description by the fictional current. Owing to the fact that the fictional current slopes are only half as steep, a correction can be easily done in the continuous-time domain description later. From the circuit diagram in Fig. 4.1 we know that:

$$M_1 = \frac{(V_{dd} - V_O)R_s}{L}, \quad M_2 = \frac{-V_O R_s}{L}, \quad D' = 1 - D,$$

where D is the duty ratio and switch S_1 is closed when the PWM signal is high. The discrete-time output voltage $v_O(n+1)$ equals the previous voltage $v_O(n)$ plus any difference caused by the charging of the output capacitor by the inductor current and the discharging caused by the load. The charge supplied during T_1 is the average current, which is equal to $i_F(n)$, multiplied by the time T_1 , the charge supplied during T_2 is the average current equal to $i_F(n+1)$ multiplied by time T_2 . So the output voltage can be described as:

$$v_O(n+1) = v_O(n) + \frac{i_F(n)T_1}{C} + \frac{i_F(n+1)T_2}{C} - \frac{v_O(n)T_s}{R_L C}. \quad (4.3)$$

Hence (4.2) and (4.3) can be rewritten as a function of only $i_F(n)$, $v_O(n)$ and $v_C(n)$. Following the procedure in chapter 3, the next step is to apply the substitutions to obtain equations with only DC terms and small-signal terms. The DC terms are canceled and the second order terms are ignored

to obtain the set of first order small-signal difference equations:

$$i_f(n+1) = i_f(n)k_0 + v_o(n)k_1 + v_c(n)k_2 \quad (4.4)$$

$$v_o(n+1) = i_f(n)k_3 + v_o(n)k_4 + v_c(n)k_5 \quad (4.5)$$

where

$$\begin{aligned} k_0 &= -\frac{\frac{1}{2}M_2 - M_c}{\frac{1}{2}M_1 + M_c}, \quad k_1 = -\frac{1}{2} \frac{T_s}{L} + \frac{1}{4} \frac{T_s M_2}{L(\frac{1}{2}M_1 + M_c)} \\ k_2 &= \frac{\frac{1}{2}V_{dd}}{L(\frac{1}{2}M_1 + M_c)}, \quad k_3 = \frac{M_c T_s}{C(\frac{1}{2}M_1 + M_c)} \\ k_4 &= 1 + \frac{DT_s^2}{LC} - \frac{1}{2} \frac{T_s^2}{LC} - \frac{T_s}{R_L C} - \frac{1}{2} \frac{DM_c T_s^2}{LC(\frac{1}{2}M_1 + M_c)} \\ k_5 &= \frac{\frac{1}{2}D'T_s V_{dd}}{LC(\frac{1}{2}M_1 + M_c)}. \end{aligned}$$

The z-domain transfer function $\frac{i_f(z)}{v_c(z)}$ can now be found using the state-space representation and applying the z-transform, resulting in:

$$T_{ci}(z) = \frac{i_f(z)}{v_c(z)} = \frac{k_2 z + k_1 k_5 - k_2 k_4}{z^2 - (k_0 + k_4)z + k_0 k_4 - k_1 k_3}. \quad (4.6)$$

4.3.2 Continuous-time Domain Representation

For a continuous-time domain representation, a second order Padé approximation of z is used to convert the discrete-time domain transfer function into the continuous-time domain. In addition, dominant pole and zero approximation is applied, to simplify the s-domain description [33]. These simplifications and substitutions lead to the following control-to-inductor current transfer function in the s-domain:

$$T_{ci}(s) = G_{DC,ci} \frac{1 + \frac{s}{\omega_z}}{\left(1 + \frac{s}{\omega_p}\right) \left(1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}\right)} \quad (4.7)$$

where

$$\begin{aligned} G_{DC,ci} &= \frac{1}{R_s} \frac{1}{1 + \frac{R_L T_s}{L} \left(m_c D' - \frac{1}{2}\right)} \\ \omega_z &= \frac{1}{R_L C}, \quad \omega_n = \frac{\sqrt{12}}{T_s} \\ \omega_p &= \frac{1}{R_L C} + \frac{T_s}{LC} \left(m_c D' - \frac{1}{2}\right) \end{aligned}$$

$$Q_p = \frac{1}{\sqrt{12} \left(D' \left(1 + \frac{M_c}{\frac{1}{2} M_1} \right) - \frac{1}{2} \right)}$$

and

$$m_c = 1 + \frac{M_c}{M_1}.$$

As mentioned in subsection I, the amplitude of subharmonic oscillations obtained using the fictional current description is only half of the actual subharmonic oscillation amplitude. The factor Q_p in (4.7) describes the amplitude of the subharmonic oscillations in the s-domain and can be corrected by doubling M_1 to obtain the actual inductor current slope, giving

$$Q_p = \frac{1}{\sqrt{12} \left(D' \left(1 + \frac{M_c}{M_1} \right) - \frac{1}{2} \right)} = \frac{1}{\sqrt{12} \left(D' m_c - \frac{1}{2} \right)}. \quad (4.8)$$

4.3.3 Control-to-Output Transfer

The final step is to obtain the control-to-output voltage transfer by multiplying $T_{ci}(s)$ with the inductor current-to-output voltage transfer $T_{io}(s)$ of the converter. Using the approach described in [77], $T_{io}(s)$ can be derived for all topologies. Assuming ideal converters (without ESR), this results in the universal expression for the control-to-output transfer

$$T_{co}(s) = G_{DC,co} \frac{1 - \frac{s}{\omega_{rhpz}}}{\left(1 + \frac{s}{\omega_p} \right) \left(1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2} \right)}, \quad (4.9)$$

where the parameters for the different topologies are given in Table 4.2 for both (4.7) and (4.9).

4.4 Verification of the Extended Modeling Technique

Since the SIMPIS simulations for boost converter match very well with the measurements in chapter 3, measurements of the control-to-inductor current and control-to-output voltage have only been done on a PCMC based boost converter, due to the availability of LM5122EVM-1PH synchronous boost controller evaluation module. For buck and buck-boost converters, we rely on the simulations results only. The measurement setup is given in

Table 4.2: Expressions for the model parameters for buck, boost and buck-boost topologies of (4.7) and (4.9).

	Buck	Boost	Buck-Boost
$G_{DC,ci}$	$\frac{1}{R_s} \frac{1}{1 + \frac{R_L I_s}{L} (m_c D' - \frac{1}{2})}$	$\frac{2}{R_s} \frac{1}{2 + \frac{R_L I_s D'^3}{L} (m_c - \frac{1}{2})}$	$\frac{1+D}{R_s} \frac{1}{1+D + \frac{R_L I_s D'^3}{L} (m_c - \frac{1}{2})}$
$G_{DC,co}$	$\frac{R_L}{R_s} \frac{1}{1 + \frac{R_L I_s}{L} (m_c D' - \frac{1}{2})}$	$\frac{R_L D'}{R_s} \frac{1}{2 + \frac{R_L I_s D'^3}{L} (m_c - \frac{1}{2})}$	$-\frac{R_L D'}{R_s} \frac{1}{1+D + \frac{R_L I_s D'^3}{L} (m_c - \frac{1}{2})}$
ω_z	$\frac{1}{R_L C}$	$\frac{2}{R_L C}$	$\frac{1+D}{R_L C}$
ω_{rhpz}	—	$\frac{R_L D'^2}{L}$	$\frac{R_L D'^2}{DL}$
ω_p	$\frac{1}{R_L C} + \frac{I_s}{LC} (m_c D' - \frac{1}{2})$	$\frac{2}{R_L C} + \frac{I_s D'^3}{LC} (m_c - \frac{1}{2})$	$\frac{1+D}{R_L C} + \frac{I_s D'^3}{LC} (m_c - \frac{1}{2})$
ω_n	$\frac{\sqrt{12}}{T_s}$	$\frac{\sqrt{12}}{T_s}$	$\frac{\sqrt{12}}{T_s}$
Q_p	$\frac{1}{\sqrt{12} (m_c D' - \frac{1}{2})}$	$\frac{1}{\sqrt{12} (m_c D' - \frac{1}{2})}$	$\frac{1}{\sqrt{12} (m_c D' - \frac{1}{2})}$

Fig. 4.8 and the component values used can be found in Table 4.3.

For comparison with the measurements, the model for a PCMC boost converter is extended to include the output capacitor ESR, this gives an extra zero in $T_{io}(s)$ and $T_{co}(s)$ at frequency $\omega_{ESR} = \frac{1}{R_C C}$. The model is compared to both measurement and simulation in Fig. 4.10 and 4.11, and the maximum magnitude deviation of the model with respect to simulation up to half f_s is 0.3 dB, the maximum phase deviation is 9° at $f_s/2$. The comparison between model and simulation for other topologies yields similar results. The maximum magnitude deviation of the model with respect to the measurement is 4 dB, the maximum phase deviation is 40° . This

Figure 4.8: Measurement setup of a PCMC based boost converter with capacitive load, the values for circuit parameters are given in Table 4.3.

Table 4.3: Circuit parameters for PCMC boost converter measurement

Parameters	Values
Duty ratio (D)	0.5
Slope compensation factor (m_c)	2.4
Compensating slope (M_c)	$67.5 \text{ mV } \mu\text{s}^{-1}$
On time slope (M_1)	$48 \text{ mV } \mu\text{s}^{-1}$
Inductor (L)	$10 \text{ } \mu\text{H}$
Current sense gain ($R_s = R_i \cdot A_i$)	$4 \text{ m}\Omega \times 10$
Supply voltage (V_{dd})	12 V
Switching frequency (f_s)	250 kHz
Load (C)	$370 \text{ } \mu\text{F}$
ESR (R_C)	$55 \text{ m}\Omega$
Decoupling capacitor (C_d)	22 nF
Input resistance (R_{in})	$47 \text{ k}\Omega$
External current sense gain (A_m)	30

Figure 4.9: Modified LM5122EVM-1PH synchronous boost evaluation module and AD8210 current shunt monitor

deviation happens at very low frequencies in the control-to-output voltage transfer and is caused by a high pass filter made by the input resistance of $1 \text{ M}\Omega$ of the gain-phase analyzer in combination with decoupling capacitor C_d . The model of the PCMC boost obtained using the new modeling method agrees very well with both simulation and measurements.

Figure 4.10: Control-to-inductor current transfer for a PCMC based boost converter with capacitive load.

Figure 4.11: Control-to-output voltage transfer for a PCMC based boost converter with capacitive load.

4.5 Conclusions

An extended modeling method is proposed for peak-current mode controlled dc-dc converters used in continuous conduction mode. The improvement compared to other approaches is that it gives a correct description of the control-to-inductor current transfer for capacitive loads. This is shown by comparisons with simulations and measurements, which also confirm the accuracy of the control-to-output voltage transfer which is obtained.

A SELF-OSCILLATING BOOSTING AMPLIFIER WITH ADAPTIVE SOFT-SWITCHING CONTROL

This chapter is taken from the author's paper published in IEEE Journal of Solid-State Circuits [11]¹.

5.1 Introduction

In chapter 2, it was explained that a boosting stage as a single stage amplifier for piezoelectric transducers has a benefit of higher efficiency over the traditional amplifiers topologies. However, since the linearity of such a topology is not good, the use of relevant feedback scheme is essential for making signal generation with acceptable distortion possible.

In chapter 3 and 4, the focus was on PCMC, which uses an additional current feedback loop for a feedback method as it provides many benefits over VMC by making the dynamics of the system simpler. Fig. 5.1 shows a typical PCMC scheme with a piezoelectric load. The load is primarily capacitive (C), with a resistive component R_L that models the water coupling

¹Starting the third paragraph, this chapter is identical to the paper from the end of section I and onward.

In addition to linearity, power efficiency is of crucial importance for developing low cost and low power USNs. In high voltage applications, soft-switching can considerably reduce dissipation [28, 32, 80]. Traditional PCMC does not provide an easy way to keep the converter running in soft-switching. Hence, as a good alternative to PCMC, a hysteretic based current-mode control scheme is proposed here, that is well suited for dynamic signal generation with soft-switching and doesn't require complex adaptive slope compensation schemes.

Therefore in this chapter, the key idea is to use a boost converter for direct signal generation in a power efficient way. This is achieved by integrating Hysteretic Current Mode Control (HCMC) (that achieves wide bandwidth and much greater stability) with fast cycle-by-cycle soft-switching

Figure 5.1: Peak current mode control scheme

operation. Section 5.2 discusses in detail the proposed control scheme that improves the efficiency and bandwidth. In section 5.3, the system and circuit realizations are discussed. The proposed strategy is verified by measurement results in Section 5.4, and finally the conclusion is described in Section 5.5.

5.2 Ripple HCMC and Soft-Switching Regulation Scheme

In this section, ripple HCMC and the associated soft-switching regulation scheme are proposed. The implementation and advantage of ripple HCMC is described and compared to traditional PCMC in subsection I. The mechanism of achieving minimum dissipation is discussed in subsection II and the adaptive soft-switching regulation scheme that improves the efficiency is explained in subsection III.

5.2.1 Ripple HCMC

Traditional current mode control schemes have gained more popularity in recent years due to the advantages stated earlier. However, most of the fixed frequency solutions suffer from subharmonic stability issues resulting in limited loop gain and bandwidth. The HCMC technique as explained in [81], provides fast transient response, higher loop gain and better stability than traditional current mode control schemes, as will be shown later. Fig. 5.2 shows a simple implementation of a ripple HCMC based self-oscillating boost converter. In ripple HCMC, a fixed voltage $\frac{1}{2}\Delta V_{win}$ is added and subtracted to the control signal V_c to generate the hysteretic window in which the inductor current oscillates. The sensed inductor current is fed into the controller and the peak and valley crossing points are dependent on the hysteretic window to generate the PWM signal. Compared to a hysteretic comparator implementation as described in [82], a separate error amplifier based structure is chosen here because it helps to control the average current that results in better frequency and voltage regulation [83]. In addition the noise immunity of the proposed structure with error amplifier is far superior to that of a comparator based scheme.

Figure 5.2: Ripple HCMC scheme

Contrary to peak or valley CMC, the switching frequency f_s is not fixed and is given by:

$$f_s = \frac{m_1 * D}{\Delta V_{win}} * R_s, \{D = 0..1\} \quad (5.1)$$

Where R_s is the sense resistance, m_1 is the rising inductor current slope, D is the duty ratio and V_{dd} is the supply voltage.

The variable switching frequency is a drawback of HCMC as it depends on several factors including input voltage, output voltage and hysteretic window. This creates some uncertainty with respect to Electro Magnetic Interference (EMI), though the frequency band can roughly be controlled.

To determine the loop stability, the PCMC circuit in Fig. 5.1 and the HCMC circuit in Fig. 5.2 are modelled in SIMPLIS. In this way the inherent loop gain of both control schemes can be compared and validated. The

circuit parameters are summarized in Table 5.1. The values are chosen such that the systems display identical loop gain at higher frequencies. The transducer parameters are not specific for a particular transducer, but the operation and performance of the circuits are not dependent on the exact values either.

The voltage loop gain and phase of both PCMC and HCMC are compared

Table 5.1: Circuit parameters

Parameters	Values
Duty ratio (D)	0.5
Inductor (L)	2 μ H
Current sense gain for PCMC($R_s \cdot A_i$)	25 m Ω *15
Current sense gain for HCMC($R_s \cdot A_i$)	25 m Ω *1
Supply voltage (V_{dd})	9V
Switching frequency (f_s)	1 MHz
Slope compensation (peak-peak)(PCMC)	150 mV
Compensator gain (PCMC)	12
Compensator gain (HCMC)	1
Output capacitance (C)	0.47 μ F
Resistance (R_L)	1 k Ω
Decoupling capacitance (C_{decap})	50 μ F

in Fig. 5.3 and Fig. 5.4 respectively. HCMC provides more loop gain, even having a compensator gain of one. In PCMC the dc gain is reduced by the amount of slope compensation, while HCMC has no slope compensation. The advantage can be seen at the higher frequencies because the phase shift is much lower for HCMC. It can also be seen that the PCMC operates at the edge of instability (to achieve the same unity gain frequency); any more loop gain in the compensator makes the system oscillate. Therefore in order to make the system sufficiently stable and increase the loop gain, a relatively complex compensation network and dynamic slope compensation are required.

To test HCMC for varying operating conditions, the topology in Fig. 5.2 with the circuit parameters in Table 5.1 is simulated in SIMPLIS for a range of duty ratios and switching frequencies. The results of loop gain and phase are shown in Fig. 5.5 and Fig. 5.6 respectively. It can be seen that the phase margin stays sufficient for a wide range of operating conditions. Apart from the inherent stability and higher bandwidth, ripple HCMC

Figure 5.3: Loop gain comparison of PCMC and HCMC

Figure 5.4: Phase comparison of PCMC and HCMC

Figure 5.5: Loop gain of HCMC for different duty ratios and switching frequencies

Figure 5.6: Phase of HCMC for different duty ratios and switching frequencies

provides an extra degree of freedom: changing the current ripple. This property is exploited here by adaptively adjusting the ripple to keep the converter in soft-switching and thus increase efficiency.

5.2.2 Minimum Dissipation

In an application involving battery powered USN nodes, the requirement of output power can change drastically from low to high power levels and vice versa. Therefore in order to improve battery life, the boost converter must be power efficient over a wide range of output power levels. A complete characterization of different power dissipation mechanisms in a class-D amplifier is given in [28]. The results show that for a high voltage class-D amplifier, minimum dissipation can be achieved by keeping the amplifier running near the soft-switching boundary, where the inductor current is just enough to charge and discharge the output switching node. Therefore in order to verify the same conclusion for a boost converter, the boost converter with power stage shown in Fig. 5.7 is analyzed here. The output voltage of a boost converter can be expressed as:

$$V_{out} = \frac{V_{dd}}{1-D} \quad (5.2)$$

The root mean squared inductor current $I_{L,RMS}$ is composed of a dc component I_L and a triangle ripple component ΔI_L . This can be expressed as

Figure 5.7: A bidirectional boost converter power stage

[28]:

$$I_{L,RMS} = \sqrt{I_L^2 + \frac{\Delta I_L^2}{12}} \quad (5.3)$$

The dc component of the inductor current I_L depends on the output current I_o and duty ratio (D):

$$I_L = \frac{I_o}{1 - D} \quad (5.4)$$

the ripple of the inductor current ΔI_L , is given by:

$$\Delta I_L = \frac{V_{dd} * D}{2 * L * f_s} \quad (5.5)$$

The total dissipation (P_d) in a boost converter can be categorized into three major loss mechanisms: conduction loss (P_{cond}) due to the inductor current ($I_{L,RMS}$), gate-driver loss (P_g) caused by charging and discharging the gate capacitance of the power transistors and switching loss (P_{sw}) associated with charging and discharging of the output parasitic capacitances of the power transistors at the PWM node. For high voltage applications, the dominant losses are the switching losses. As shown in Fig. 5.8, the switching loss (P_{sw}) based on falling switching transition (also valid for rising transitions) can be categorized into one of the following categories:

- Hard-switching loss: The inductor current cannot discharge the PWM node as shown in Fig. 5.8a.
- Partial soft-switching: The inductor current is not large enough to completely discharge the PWM node during dead time as shown in Fig. 5.8b.
- Complete soft-switching: The inductor current is enough to completely discharge the PWM node as shown in Fig. 5.8c.

In order to verify if the minimum dissipation can be achieved at the soft-switching boundary, a comparison of the transistor-level power dissipation simulation with the analytical model presented in [28] can be made. Therefore the output power stage shown in Fig. 5.7 with circuit parameters in Table 5.2 is simulated with two different output power conditions for a range of switching frequencies (to vary the inductor current ripple).

Table 5.2: Circuit parameters for dissipation analysis

Parameters	Values
Power mosfet model	IRFL014
Gate driver model	LTC4446
Diode model (D)	1N5819
Boot strap capacitance (C_{boot})	0.1 μ F
Duty ratio (D)	0.5
Inductor (L)	2 μ H
Supply voltage (V_{dd})	9 V
Driver voltage (V_{cc})	9 V
On resistance(r_{on})	250 m Ω
Gate charge (Q_{iss})	8nC
Output charge (Q_{oss})	6nC
Output capacitance (C)	10 μ F
Dead time (t_d)	80nsec
Load current(I_{o1})	50mA
Load current(I_{o2})	400mA

The comparison of the analytical model and circuit simulation is shown in Fig. 5.9 and Fig. 5.10 for an output current (I_{out}) of 50mA and 400mA respectively.

For low output power as shown in Fig. 5.9, the dissipation is mainly due to conduction losses at low switching frequency, due to the large current

Figure 5.8: Illustration of different switching conditions from hard-switching to complete soft-switching

ripple. As the switching frequency is increased, the conduction losses reduce, the converter stays fully soft-switching and a minimum dissipation point is achieved. Further increasing the switching frequency results in partial soft-switching transitions making switching loss start to increase. For high output power as in Fig. 5.10, the trend is similar. The minimum dissipation point is achieved at a lower switching frequency because a larger inductor current ripple is necessary to keep I_L bidirectional at the switching instants.

Figure 5.9: Minimum power loss Vs switching frequency for fixed $V_o=24V$ and $I_o=50mA$

Figure 5.10: Minimum power loss Vs switching frequency for fixed $V_o=24V$ and $I_o=400mA$

Compared to hard-switching, complete soft-switching requires a reverse inductor current that can be considered an extra loss. However, in high voltage applications, the CV^2 losses of charging parasitic capacitances are higher than the extra loss as a result of the reverse inductor current, as can be seen in Fig. 5.10.

These results show that also for a high voltage boost converter power stage, the minimum dissipation occurs at the boundary of soft-switching and partial soft-switching. For the case of simplicity the inductor core loss is ignored in the comparison above. Inductor core loss increases the total dissipation, however as shown in [28] the minimum dissipation still occurs very close to the soft-switching boundary. Therefore by changing the hysteretic window in HCMC as function of I_o , the current ripple can directly be controlled and the switching frequency can be brought to this point of minimum dissipation.

5.2.3 Soft-switching regulation loop

Based on the results in section II, our proposed scheme uses a soft-switching regulation loop as shown in Fig. 5.11 to reduce power dissipation, by adaptively changing the magnitude of the current ripple. This results in optimum power efficiency over wide range of output power levels for the HCMC based boost converter. In order to make the converter run in soft-switching, detection of the switching transitions is a first step. Depending on the magnitude and direction of the inductor current at the switching instant, switching of the V_{pwm} node can be made lossless. As was shown in Fig. 5.8c, complete soft-switching can occur when the inductor current is bidirectional and can charge/discharge the parasitics at V_{pwm} to V_{out} and GND respectively, making both the rising and falling transitions soft-switching. By observing the V_{pwm} node during t_d it can be detected if a transition is soft-switching: if the PWM node reaches the opposite supply rail within the dead time, the transition is lossless.

The soft-switching regulation loop that we use can be best understood with the help of Fig. 5.12 which shows a step increase of the average inductor current. The moment the average inductor current is increased, one

Figure 5.11: HCMC based boost converter with soft-switching regulation loop

of the transitions becomes hard-switching; this triggers the soft-switching regulation loop to increase the hysteretic window, causing the inductor current ripple (ΔI_L) to increase and move the converter back to soft-switching transitions. This way it can track the highest efficiency over a wide range of output power levels.

Although the HCMC loop and the soft-switching loop together determine the PWM signal, the loops are basically independent. Fig. 5.11 shows that the hysteretic window is determined by adding and subtracting $\frac{1}{2}\Delta V_{win}$ from the error voltage V_c , generating the inductor current switching points V_{peak} and V_{valley} . Therefore, these are symmetric around the error voltage V_c . So when the ripple (represented by ΔV_{win}) changes, V_{peak} and V_{valley} change, but the average stays the same. Although the

Figure 5.12: The regulation of soft-switching transitions

gain and phase of the HCMC loop change somewhat due to the changing switching frequency (as illustrated in Fig. 5.5 and Fig. 5.6), the duty cycle and the average inductor current stay the same and the output voltage regulation is (in first order) not disturbed. Hence the HCMC loop and f_s regulation loop are largely independent, preventing instability [83].

5.3 System and Circuit Implementation

The proposed implementation of the topology is shown in Fig. 5.13. The system is realized on a PCB using an external power stage and the control is realized on chip. The non-overlapping gate driver signals are generated internally for the external gate driver IC. The chip circuitry is mainly divided into the ripple HCMC loop and the soft-switching regulation loop. Due to the ease of adding and subtracting currents, the HCMC loop implementation is realized in the current domain.

5.3.1 HCMC regulation

The HCMC loop is responsible for making sure the output voltage V_o signal tracks the external reference signal V_{ref} using a negative feedback loop. The actual implementation of the transconductor is shown in Fig. 5.14. The on-chip Current-Sense (CS) transconductor produces two copies of I_{sense} , a scaled version of I_L , by translating the voltage across the sensing resistor R_s .

Figure 5.13: System overview of HCMC based boost converter with soft-switching regulation

Figure 5.14: Implementation of transconductor G_{m1}

The transconductor G_{m1} generates two copies of the desired control

current I_c (current representation of V_c in Fig. 5.11), whereas the transconductor G_{m2} produces the relevant window current I_{win} (current representation of V_{win} in Fig. 5.11) to set the desired f_s . The implementation of both transconductors is identical using source degeneration for better linearity, only the degeneration resistors are different and one of the output currents of G_{m2} is reversed because it must be subtracted from I_c . To avoid a negative window the charge pump voltage V_{cp} is always greater than V_{bias} . The peak and valley current comparators are implemented as inverters.

5.3.2 Current Sensing

In all current mode control based topologies, current sensing is a fundamental step. Several techniques have been reported in literature to implement on-chip current sensors [84–87]. For HCMC the complete inductor current needs to be sensed, therefore for maintaining simplicity and accuracy, the choice of an off-chip sense resistor R_s is made. The value of R_s is chosen to be four times smaller than R_{on} of the external power transistor to keep conduction losses low. To reduce distortion in V_o , a linear current sensing scheme is proposed in Fig. 5.15. The circuit is designed to handle common-mode voltages near V_{dd} and is implemented differentially. The gate voltage of the input transistors M_{1-4} is set by bias transistor M_b . The cascode transistor $M_{cascode}$ helps to improve current matching. The $M_{HVprotect}$ transistors clamp the LVNMOS gate voltage during an over-current situation.

During an increase in I_L as shown in Fig. 5.15, the gate-source voltage of both M_1 and M_2 increase while the gate-source voltage of M_3 and M_4 decreases. Hence the current I_1 increases and I_3 decreases. The difference current I_{sense} is thus equal to the inductor current I_L scaled by R_s and the transconductance (gm) of M_1 and M_3 . The advantage comes from the fact that while gm is non-linear, the difference of currents cancels the (dominant) second order non-linearity of gm. Therefore, linearity is better compared to a differential pair, where the sum I_1 and I_3 would be constant. The maximum non-linearity of the simulated current sense is 2.6% of full

Figure 5.15: High side current sense circuit

scale. Small deviations in the sensed inductor current are no problem because the external loop tracks the average current and adjusts it until the average current is correct. In total two replica currents are generated for peak and valley level detection as explained in Fig. 5.14 earlier.

5.3.3 Soft-Switching Regulation

The soft-switching regulation loop shown in Fig. 5.13 works by observing V_{pwm} at the end of the dead time t_d . This information is passed to the ripple control logic to determine if the ripple needs to be increased or decreased in order to keep the converter running in soft-switching. Based on this decision, the ripple control logic drives the charge pump/loop filter with an up/down single shot pulse. If the ripple needs to be increased, the charge pump increase V_{cp} with a step ΔV_{cp} and vice versa.

Due to the fact that we use an external power stage, the signals $V_{g,HS}$ and $V_{g,LS}$ generated by the chip suffer from propagation delay introduced by the external driver IC. Hence to satisfy the timing requirements for internal logic, a replica delay t_{prop} is added to the internal signals in the

ripple control logic block and must be set to match the external driver delay.

Depending on the output power level, the regulation loop adjusts f_s in order to maintain soft-switching. The minimum f_s is chosen to be 1MHz dictated by inductor size, distortion and point of hard-switching. Similarly the maximum f_s must be limited to approximately 3.2MHz due to the external power stage propagation delay, distortion caused by dead time and gate driver dissipation. The f_s limits are externally set by specifying the window limits; the window limit block monitors I_{win} and disables the ripple control logic if needed.

In normal operation during steady state the regulation loop oscillates around soft and partial soft-switching transitions every alternate switching cycle. The main time constant in the loop, however, is set by the loop filter, ensuring a dominant first order behaviour of the loop gain. Therefore in response to sudden increase/decrease in output power, the regulation loop doesn't abruptly change the ripple.

The step size ΔV_{cp} of the charge pump is set to 20mV, equivalent to a 110mA change in inductor current, which is based on the required tracking speed of the loop. In the proposed design, the tuning window of the charge pump voltage is 350mV, meaning the loop can adapt from minimum to maximum inductor current in 18 switching periods. With an average switching frequency of 2MHz this results in a 30kHz full-power bandwidth.

5.3.4 V_{pwm} Detect & Ripple Control

The V_{pwm} detection circuit is shown in Fig. 5.16. When $H2L_{det}$ or $L2H_{det}$ is high, it detects if V_{pwm} has reached the corresponding supply rail within the dead time t_d . Since the $V_{g,HS}$ driver signal is level shifted by the driver IC for proper operation, $L2H_{det}$ must also be level shifted to turn on $M_{shield}HS$ transistor, as shown in Fig. 5.16. The $H2L$ detection is communicated via a current mirror near V_{dd} to isolate the severe ground bounce on the power ground. The detection information is passed to the ripple control logic shown in Fig. 5.17. The ripple control logic checks if

Figure 5.16: Soft-switching detection circuit

Figure 5.17: Ripple control logic

both rising and falling transitions of the V_{pwm} node are soft-switching, triggering the corresponding DN pulse. If any one of the V_{pwm} transitions is not finished within t_d , the UP pulse is triggered. These UP/DN pulses

are passed on to the charge pump at the end of each switching cycle resulting in increase/decrease in the current ripple. The charge pump is timed by a one shot circuit to increase and decrease the voltage in steps at the input of the transconductor.

5.4 Measurements

The proposed HCMC based boosting amplifier with soft-switching regulation is implemented on a PCB as shown in Fig. 5.18, combining an external power stage and the proposed chip. The chip is implemented in a 60V 0.25 μm high voltage CMOS process with a size of 3mmx3mm and is shown in Fig. 5.19. The performance and component parameters are summarized in Table 5.3. For the chip implementation the analog and digital sections are separated in the layout to avoid switching noise. Similarly the external power stage switching current loop is separated from the analog signal path, to reduce the effect of ground bounce. For start-up operation, the soft-switching loop is initially disabled by an enable/disable pin and an initial charge pump voltage of $V_{cp}=1.55\text{ V}$ is applied externally. After the amplifier reaches steady state operation, the soft-switching loop is enabled.

Figure 5.18: Implemented PCB for the amplifier

Figure 5.19: Chip micrograph

Table 5.3: Performance and Components Summary

Parameters	Values
Technology	0.25 μm HVCMOS
Driver IC	LM5101C
Power transistors	NDT3055
C_{boot}	0.1 μF
Inductor (L)	2 μH
Supply voltage (V_{dd})	9V
Driver voltage (V_{cc})	9V
IC voltage	5V
On resistance (r_{on})	100 m Ω
Output capacitance (C)	0.47 μF
Decoupling capacitor (C_{decap})	50 μF
Switching Freq (f_{s})	1MHz-3.2MHz
Signal Freq (f_{sig})	30 kHz
* R_{L}	1k Ω
Dead time (t_{d})	80nsec
Maximum Power Efficiency(η)	85% @ 20VA
Die Size	3 mm $\times$ 3 mm
* R_{L} models the water coupling	

Fig. 5.20 shows the boosted output voltage, measured across the load for a 30kHz sine wave. The output shows a 38Vpp signal with a supply voltage of 9V. Although the technology supports 60V, the maximum output voltage is limited to 50V because at high switching frequencies the dead time limits the maximum boosting ratio. Also, some of this headroom is used for r_{on} losses.

Figure 5.20: Time domain waveform of boosted output signal (red) generated at 30kHz across V_{out} and GND with an input supply of 9V

Fig. 5.21 and Fig. 5.22 present a comparison between the operation of the amplifier at two output powers. For the first case where the amplifier is driven by a high swing input signal, the inductor current ripple is increased to make the converter run near the soft-switching boundary. When the input voltage signal decreases, the inductor current ripple decreases resulting in optimum operation.

As the load is dominantly capacitive at the desired signal frequency of 30kHz, the processed output power (P_{out}) is apparent power. Hence the measured efficiency is calculated as:

$$\eta = \frac{P_{out}}{P_{out} + P_d} \quad (5.6)$$

Where P_{out} is measured as $V_{out,rms} * I_{out,rms}$ (VA) and P_d is the total amplifier power dissipation, including external power stage and control

Figure 5.21: Time domain waveform of PWM (green) signal generated at 30kHz across V_{pwm} and GND with inductor current I_L (blue)

Figure 5.22: Time domain waveform of PWM (green) signal generated at 30kHz across V_{pwm} and GND with inductor current I_L (blue)

circuits. The measured efficiency of the boosting amplifier for a 30kHz sine wave as a function of P_{out} is shown in Fig. 5.23 for both fixed and adaptive f_s . P_{out} is varied by changing the amplitude of the output signal. Since the proposed scheme tunes itself to achieve minimum power loss, the effectiveness of the scheme is compared to two fixed 1MHz and 3.2MHz f_s modes. Fig. 5.23 clearly shows that the scheme tracks the best efficiency

across the whole output power range as compared to the low and high switching modes.

Figure 5.23: Efficiency measurements for adaptive and fixed f_s as a function of output power at 30kHz input signal.

Figure 5.24: Power dissipation measurements for adaptive and fixed f_s as a function of output power at 30kHz input signal.

Fig. 5.24 shows a comparison of the power dissipation P_d of the adaptive f_s regulation with fixed f_s conditions. At low output power, the amplifier regulates itself to 3.2MHz switching frequency and at high power it regulates itself to 1MHz switching frequency.

For the case of minimum output power, the soft-switching regulation improves the efficiency from 18.9% to 27% by dissipating 35% less power compared to switching at a fixed 1MHz. The dissipation at low output power is mainly dominated by fixed dissipation sources independent of load current, like static currents, gate driver losses and other capacitive

losses. In case of peak output power, the efficiency is improved from 78% to 84% by dissipating 33% less power compared to switching at a fixed 3MHz. This improvement is largely independent of the signal frequency as the soft-switching loop is fast enough to track a 30 kHz signal, so lower frequency signals will be quasi static in comparison.

The system achieves a THD+N of 0.6% at 1kHz and 5% at 30kHz with a $40V_{pp}$ sinusoidal output signal as shown in Fig. 5.25 and Fig. 5.26 respectively.

Figure 5.25: Spectrum plot of 30kHz $40V_{pp}$ sine generated across the load with 9V input voltage

Figure 5.26: Spectrum plot of 1kHz $40V_{pp}$ sine generated across the load with 9V input voltage

THD+N of the amplifier is also examined as a function of output voltage swing in Fig. 5.27. In addition the amplifier's distortion is compared with adaptive and fixed f_s . THD+N of a hysteretic based boost converter

Figure 5.27: THD + N measurement results comparison with $f_{sig} = 1\text{kHz}$, $V_{dd} = 9\text{V}$, for adaptive f_s and fixed f_s of 1MHz and 3.2MHz

depends on several factors. Apart from the inherent boost converter non-linearity, contributing effects are noise, the influence of f_s on the loop gain [88], asymmetric rise and fall time of the V_{pwm} node [28] and the effect of fixed dead time at high f_s [89]. The exact contribution of each effect to THD+N, however, is difficult to predict.

The proposed amplifier is compared in Table 5.4 with previously reported state-of-the-art piezoelectric driver topologies. Although the topology in [44] uses a boost converter for direct signal generation, the operating bandwidth and output power are very low.

Table 5.4: Comparison with other high-voltage piezo-driver topologies

Parameters	This work	[44]	[90]	[28]	[15]
Technology	0.25 μm	0.18 μm	-	0.14 μm	-
Topology	boosted	boosted	boosted	class-D	linear
Load	470 nF	330 nF	330 nF	23 μF	10 μF
Bandwidth (BW)	30kHz	150Hz	150Hz	300Hz	200Hz
Inductor (L)	2 μH	100 μH	4.7 μH	100 μH	N/A
V_{opp}	40V	100V	100V	80V	220V
Supply(V_{dd})	9V	3.6V	3.6V	80V	220V
f_s	1-3.2MHz	kHz range	-	230-530kHz	N/A
Efficiency	85%	*82%	*32%	**83%	-
($P_{out,max}$)	20VA	0.39VA	0.39VA	45VA	1VA
THD+N	0.6%-5%	0.56%	1.2%	0.94%	0.62%
	1kHz-30kHz	150Hz	150Hz	500Hz	200Hz

'-'=not available, N/A=not applicable

(*) Derived efficiency based on given load and dissipation conditions

(**) Derived efficiency based on class-D+boost ($\eta = 90\%$) with same boosting ratio

The topology in [90] shows much lower efficiency with even higher distortion. The work in [28] is based on a class-D amplifier which uses a fixed supply voltage. In this case for the purpose of comparison, the real efficiency of the system is calculated based on that class-D amplifier combined with a hypothetical dc-dc boost converter with an efficiency of 90%. In [15], a linear amplifier is proposed; the efficiency figures are not available but bandwidth is lower and distortion is higher. Overall, the proposed system shows higher efficiency and much higher bandwidth than previous works.

5.5 Conclusions

This chapter proposes an efficient method of generating high voltage signals for piezoelectric transducers from a single boost converter stage. By using ripple hysteretic current-mode control the boost converter can achieve high bandwidth without stability problems. Furthermore, by combining the hysteretic loop with soft-switching regulation, the inductor current ripple is automatically tuned to achieve soft-switching regulation over a wide range of output power. The control circuits are realized on chip and measurements show that the performance improves the state of the art by featuring higher efficiency and considerably higher bandwidth.

CONCLUSIONS AND RECOMMENDATIONS

This chapter describes the most important conclusions in this thesis, followed by a summary of the original contributions and a discussion on the future recommendations.

6.1 Summary and Conclusions

In chapter 1, a brief introduction to underwater communication with focus on advantages of acoustic communication was presented. To support the growing need in building scalable acoustic underwater sensor networks, the chapter highlighted the importance of highly power efficient and low cost solutions for USNs, followed by a discussion on key application areas and major challenges in the design and development of USNs.

In general, the communication capacity of underwater channel is low and the network nodes need to be highly power efficient to be able to operate with limited battery power, making the design of electronics for such an application a key challenge. In particular, the design of an amplifier for a piezoelectric load needs special considerations like supply boosting and high power efficiency, to be able to support such an application. This is the key motivation of this thesis, i.e. *to realize a new power-efficient integrated*

amplifier for driving piezoelectric loads that can generate high output voltage signals despite having limited battery supply.

Therefore, in chapter 2, different approaches for amplifier design related to piezoelectric transducers were discussed. It was explained that the linear amplifiers are good for sound generation with excellent linearity but fail to deliver output power with good efficiency, especially for capacitive loads. Switching amplifiers on the other hand, like the class-d amplifier has been a popular choice for sound generation due to its high efficiency and low distortion, however it still needs to have supply boosting incorporated to meet the high output voltage swing requirement for driving the piezoelectric loads.

It was proposed that a boosting amplifier, on the other hand, can combine supply boosting and signal generation to accomplish a more power efficient solution. However, the distortion of such a topology is much higher than for comparative schemes. Therefore to keep the distortion to an acceptable level, a feedback scheme with wide band operation and good stability is necessary. This makes current mode control schemes a good option for a boosting amplifier over voltage mode control.

In order to understand the control for an amplifier with piezoelectric load, a PCMC scheme for a boost converter stage was investigated in chapter 3. In particular, the traditional modeling approaches fail to predict accurately the transfer characteristics for a boost converter stage with PCMC, driving a capacitive load. A new modeling methodology based on discrete time modeling has been developed. It was shown with the help of simulations and measurements, that the proposed modeling method is able to accurately predict the transfer characteristics for both resistive and capacitive loads.

With the developed model in chapter 3, the understanding of stability of PCMC for a boosting converter stage for a capacitive load has been established. This results in an accurate prediction of loop gain, location of poles and zeros, which is essential for the design of a feedback compensation scheme for a boost converter stage with PCMC.

The method developed in chapter 3 was focused on the boost converter

topology only. Chapter 4 discussed the validity of the modeling method to other basic switching topologies like buck and buck-boost as well. It was shown that the developed method needs to be adapted and modified in order to capture the full dynamic characteristics for a buck converter stage. The extended model developed in chapter 4, is thus able to capture the current and voltage loop characteristics for all basic converter topologies for PCMC.

Following the analysis in chapter 3 and 4 for PCMC scheme, chapter 5 proposed the design of an improved boosting amplifier scheme for driving piezoelectric transducers. It was shown that although the traditional PCMC scheme is a good candidate for quasi-static signals, the need for complex adaptive slope compensation for dynamic signal generation makes PCMC unattractive. A HCMC scheme which uses the concept of self oscillation makes the system more stable without the need for extra slope compensation. Additionally it achieves higher loop gain, wider bandwidth and easier ripple control compared to PCMC.

Since the amplifier needs to be highly power-efficient, the underlying loss mechanisms in a high voltage switching topology have been investigated. It was shown that the power dissipation of the amplifier can be reduced by operating the amplifier under soft-switching boundary condition. This can be done adaptively by controlling the inductor current ripple. This is done changing the switching frequency of the amplifier, based on the detection soft and hard switching transitions.

Thus combining HCMC based feedback with soft-switching regulation gives the advantage of achieving both good efficiency and high loop gain. Following the analysis, a prototype of a self-oscillating boosting amplifier was designed that uses a soft-switching regulation loop with a HCMC scheme. The realized amplifier incorporates boosting and signal generation in a single stage and therefore improves the efficiency at both low and high output power with acceptable distortion. Compared to various topologies for driving piezoelectric loads, the proposed amplifier achieves best in class peak efficiency of 85%.

6.2 Original Contributions

- A new discrete time based modeling technique is derived for a boost converter. In particular, the model is able to accurately predict the loop dynamics for both capacitive and resistive loads.
- An extended modeling approach is presented for all the three basic switching converter topologies (buck, boost and buck-boost).
- Design and analysis of a hysteretic current-mode control loop with a linear on chip current sensing.
- Adaptive switching frequency regulation loop that achieves higher efficiency for both low and high output power load conditions.
- Design and realization of a single stage boosting amplifier that combines hysteretic feedback with soft-switching regulation.

6.3 Recommendations

- The type of signal modulation that is best suited for underwater applications and the required implications on amplifier linearity should be further explored.
- It has been shown with the help of simulations that hysteretic current-mode control for the boost converter achieves better stability and higher loop gain as compared to traditional peak current-mode control. This can be further investigated by developing a model that can predict the performance and give insight in the design parameters.
- Bridge based topologies with adaptive soft-switching regulation can be further explored, as it can be beneficial for lower distortion and higher output voltage.
- Identifying key contributors to the distortion in a boosting amplifier and their mitigation can be beneficial for further improvements in THD.

APPENDIX A

In this part of thesis the mathematical derivation based on chapter 3 are applied to calculate the discrete time model for a buck based topology. The equations derived here are used in chapter 4.

7.1 Discrete-time model for buck converter

The PWM based buck converter from Fig. 4.1 is repeated here in Fig. A.1, the method from chapter 3 is used to derive a model for this converter.

Figure 7.1: A PWM based buck converter, both the current loop and voltage loop are shown.

Figure 7.2: The sense voltage and control voltage v_c waveforms.

The current through the inductor is sensed by a sense resistor, this sensed current $R_s i_L$ is given in Fig. A.2. From this figure the following relations for the current $i_L(n)$, $i_L(n+1)$ and $i_{Lp}(n)$ at discrete-time intervals $T(n)$ and $T(n+1)$ are derived:

$$R_s i_{Lp}(n+1) = R_s i_{Lp}(n) - M_2 t_2, \quad (7.1)$$

$$R_s i_{Lp}(n) = R_s i_L(n) + M_1 t_1, \quad (7.2)$$

where

$$t_1 = \frac{v_c(n) - R_s i_L(n)}{M_1 + M_c}, \quad (7.3)$$

and

$$t_2 = T_s - t_1. \quad (7.4)$$

From Fig. A.1 expressions of M_1 and M_2 can be written as:

$$M_1 = \frac{(V_{dd} - v_O(n))R_s}{L}, M_2 = \frac{v_O(n)R_s}{L}. \quad (7.5)$$

Substituting (A.2), (A.3), (A.4) and (A.5) into (A.1) gives:

$$i_L(n+1) = i_L(n) - \frac{i_L(n)R_s V_{dd} - v_c(n)V_{dd}}{R_s V_{dd} - v_O(n)R_s + M_c L} - \frac{v_O(n)T_s}{L}. \quad (7.6)$$

This is a function of only $i_L(n)$, $v_c(n)$ and $v_O(n)$. The inductor current i_L is a state variable, the other state variable of this system is the output voltage v_O . The next step is to derive an equation for the output voltage at

time $T(n+1)$. The voltage at $T(n+1)$ depends on the voltage at $T(n)$ and the capacitor voltage difference between those intervals:

$$v_O(n+1) = v_O(n) + \Delta v_{\text{cap}}, \quad (7.7)$$

where Δv_{cap} is the voltage difference over the capacitor and can be written as the charge difference on the capacitor plates divided by the capacitance:

$$\Delta v_{\text{cap}} = \frac{\Delta Q}{C}. \quad (7.8)$$

This charge difference can be written as the capacitor current during time T_s , multiplied by this period:

$$\Delta Q = i_{\text{cap}} T_s. \quad (7.9)$$

The capacitor current can be obtained from Fig. A.1, by subtracting the current in the load resistor R_L from the inductor current i_L :

$$i_{\text{cap}} T_s = i_L T_s - i_{RL} T_s. \quad (7.10)$$

The current i_{RL} through R_L during period T_s is equal to the voltage over the resistor, which is v_O , divided by the resistance R_L :

$$i_{RL} T_s = \frac{v_O(n)}{R_L} T_s. \quad (7.11)$$

The sampling time or clock period T_s can be split into the intervals t_1 and t_2 as shown in Fig. A.2, this is convenient, because from Fig. A.2 the average inductor currents during those intervals can be obtained. The charge flowing through the inductor during T_s can be written as:

$$i_L T_s = \langle i_L \rangle_{t_1} \cdot t_1 + \langle i_L \rangle_{t_2} \cdot t_2, \quad (7.12)$$

where $\langle i_L \rangle_{t_1}$ is the average inductor current during time interval t_1 as seen in Fig. A.2. The average inductor current during t_1 is:

$$\langle i_L \rangle_{t_1} = \frac{i_L(n) + i_{LP}(n)}{2}, \quad (7.13)$$

the average inductor current during t_2 is:

$$\langle i_L \rangle_{t_2} = \frac{i_{LP}(n) + i_L(n+1)}{2}. \quad (7.14)$$

By substituting, (A.10) can now be written as:

$$i_{cap}T_s = \frac{i_L(n) + i_{LP}(n)}{2}t_1 + \frac{i_{LP}(n) + i_L(n+1)}{2}t_2 - \frac{v_O(n)}{R_L}T_s. \quad (7.15)$$

Substituting this into (A.7), the following expression is obtained:

$$v_O(n+1) = v_O(n) + \frac{i_L(n) + i_{LP}(n)}{2C}t_1 + \frac{i_{LP}(n) + i_L(n+1)}{2C}t_2 - \frac{v_O(n)}{R_L C}T_s. \quad (7.16)$$

Substituting (A.1) through (A.5) gives us $v_O(n+1)$ in terms of $i_L(n)$, $v_C(n)$ and $v_O(n)$:

$$\begin{aligned} v_O(n+1) = v_O(n) &- \frac{R_s^2 V_{dd} i_L(n)^2}{LC \left(\frac{R_s V_{dd}}{L} - \frac{R_s v_O(n)}{L} + M_c \right)^2} + \frac{R_s V_{dd} i_L(n) v_C(n)}{LC \left(\frac{R_s V_{dd}}{L} - \frac{R_s v_O(n)}{L} + M_c \right)^2} \\ &- \frac{1}{2} \frac{V_{dd} v_C(n)^2}{LC \left(\frac{R_s V_{dd}}{L} - \frac{R_s v_O(n)}{L} + M_c \right)^2} + \frac{T_s i_L(n)}{C} - \frac{R_s V_{dd} T_s i_L(n)}{LC \left(\frac{R_s V_{dd}}{L} - \frac{R_s v_O(n)}{L} + M_c \right)} \\ &+ \frac{V_{dd} T_s v_C(n)}{LC \left(\frac{R_s V_{dd}}{L} - \frac{R_s v_O(n)}{L} + M_c \right)} - \frac{1}{2} \frac{T_s^2 v_O(n)}{LC} - \frac{T_s v_O(n)}{R_L C}. \end{aligned} \quad (7.17)$$

7.2 Small signal discrete-time model

By assuming only small perturbations in i_L , v_C and v_O , the model can be linearized using the following substitutions:

$$i_L(n+1) \rightarrow I_L(n+1) + i_l(n+1) \quad (7.18)$$

$$i_L(n) \rightarrow I_L(n) + i_l(n) \quad (7.19)$$

$$v_C(n) \rightarrow V_C(n) + v_c(n) \quad (7.20)$$

$$v_O(n) \rightarrow V_O(n) + v_o(n) \quad (7.21)$$

$$v_O(n+1) \rightarrow V_O(n+1) + v_o(n+1) \quad (7.22)$$

where the capital letters denote DC steady state terms and the lower case ones the small signal variations. By discarding DC-terms and higher order

small signal terms (like $v_o(n) \cdot i_L(n)$), the following linear small-signal difference equations are obtained:

$$i_L(n+1) = k_0 i_L(n) + k_1 v_o(n) + k_2 v_c(n) \quad (7.23)$$

$$v_o(n+1) = k_3 i_L(n) + k_4 v_o(n) + k_5 v_c(n). \quad (7.24)$$

The k -coefficients can be obtained from (A.6) and (A.17) after applying the perturbations as described above. It is assumed that the large signal term $I_L(n+1)$ is equal to $I_L(n)$, this is the same as assuming that $I_L(n)$ is a DC term and does not change over time. The value of $I_L(n)$ is equal to the average of the inductor current minus half the ripple, as can be seen from Fig. A.2. The average inductor current is

$$I_{avg} = \frac{V_{dd}D}{R_L} \quad (7.25)$$

and the current ripple is

$$I_{ripple} = \frac{M_1 t_1}{R_s} = \frac{M_1 D T_s}{R_s}, \quad (7.26)$$

so the DC inductor current at $T(n)$ becomes

$$I_L(n) = \frac{V_{dd}D}{R_L} - \frac{1}{2} \frac{M_1 D T_s}{R_s}. \quad (7.27)$$

Furthermore the DC term of the output voltage of the buck converter is assumed to be:

$$V_O(n) = D V_{dd}, \quad (7.28)$$

this is true for low voltage ripple. The DC term $V_C(n)$ is obtained by rewriting (A.3) and taking only the DC term of the inductor current:

$$V_C(n) = t_1(M_1 + M_c) + R_s I_L(n), \quad (7.29)$$

where

$$t_1 = D \cdot T_s. \quad (7.30)$$

The following k -coefficients are obtained:

$$\begin{aligned} k_0 &= -\alpha = -\frac{M_2 - M_c}{M_1 + M_c}, & k_1 &= \frac{\alpha T_s}{L} - \frac{M_1 T_s}{L(M_1 + M_c)} \\ k_2 &= \frac{V_{dd}}{L(M_1 + M_c)}, & k_3 &= \frac{M_c T_s}{C(M_1 + M_c)} \\ k_4 &= 1 - \frac{T_s}{R_L C} - \frac{1}{2} \frac{T_s^2}{LC} + \frac{T_s^2 M_1 D}{LC(M_1 + M_c)}, & k_5 &= \frac{(1-D)T_s V_{dd}}{LC(M_1 + M_c)}. \end{aligned}$$

7.3 State space model and transfer functions

Now that we have the model in the form of (A.23) and (A.24), it can be represented in the general state-space form:

$$\mathbf{x}[n+1] = A\mathbf{x}[n] + B\mathbf{u}[n] \quad (7.31)$$

where

$$\mathbf{u}[n] = v_c(n), \mathbf{x}[n] = \begin{bmatrix} i_l(n) \\ v_o(n) \end{bmatrix}$$

$$A = \begin{bmatrix} k_0 & k_1 \\ k_3 & k_4 \end{bmatrix}, B = \begin{bmatrix} k_2 \\ k_5 \end{bmatrix}$$

By using the z-transform, the control-to-inductor current and the control-to-output voltage can be found as

$$z\mathbf{x}(z) = A\mathbf{x}(z) + B\mathbf{u}(z), \quad (7.32)$$

can be rewritten to

$$\frac{\mathbf{x}(z)}{\mathbf{u}(z)} = (zI - A)^{-1}B, \quad (7.33)$$

where I is the identity matrix and $\mathbf{x}(z)$ is a vector of the inductor current and the control-to-output voltage. The control-to-inductor current transfer function can be written as:

$$T_{ci}(z) = \frac{i_l(z)}{v_c(z)} = \frac{k_1k_5 - k_2k_4 + k_2z}{z^2 + (-k_0 - k_4)z + k_0k_4 - k_1k_3}. \quad (7.34)$$

The control-to-output voltage transfer function can be written as:

$$T_{co}(z) = \frac{v_o(z)}{v_c(z)} = -\frac{k_0k_5 - k_2k_3 - k_5z}{z^2 + (-k_0 - k_4)z + k_0k_4 - k_1k_3}. \quad (7.35)$$

These z-domain transfer functions are compared to simulation in the next section to verify that they accurately describe the PWM based buck converter, both for resistive and capacitive load in chapter 4.

DERIVATION OF DISCRETE-TIME MODEL FOR A BUCK CONVERTER

In this part of thesis the mathematical derivation based on chapter 3 are applied to calculate the discrete time model for a buck based topology. The equations derived here are used in chapter 4.

A.1 Discrete-time Model for Buck Converter

The PWM based buck converter from Fig. 4.1 is repeated here in Fig. A.1, the method from chapter 3 is used to derive a model for this converter. The current through the inductor is sensed by a sense resistor, this sensed current $R_s i_L$ is given in Fig. A.2. From this figure the following relations for the current $i_L(n)$, $i_L(n+1)$ and $i_{Lp}(n)$ at discrete-time intervals $T(n)$ and $T(n+1)$ are derived:

$$R_s i_L(n+1) = R_s i_{Lp}(n) - M_2 t_2 \quad (\text{A.1})$$

$$R_s i_{Lp}(n) = R_s i_L(n) + M_1 t_1 \quad (\text{A.2})$$

where

$$t_1 = \frac{v_C(n) - R_s i_L(n)}{M_1 + M_c} \quad (\text{A.3})$$

Figure A.1: A PWM based buck converter, both the current loop and voltage loop are shown.

and

$$t_2 = T_s - t_1 \quad (A.4)$$

From Fig. A.1 expressions of M_1 and M_2 can be written as:

$$M_1 = \frac{(V_{dd} - v_O(n))R_s}{L}, M_2 = \frac{v_O(n)R_s}{L} \quad (A.5)$$

Substituting (A.2), (A.3), (A.4) and (A.5) into (A.1) gives:

$$i_L(n+1) = i_L(n) - \frac{i_L(n)R_s V_{dd} - v_c(n)V_{dd}}{R_s V_{dd} - v_O(n)R_s + M_c L} - \frac{v_O(n)T_s}{L} \quad (A.6)$$

This is a function of only $i_L(n)$, $v_c(n)$ and $v_O(n)$. The inductor current i_L is a state variable, the other state variable of this system is the output voltage v_O . The next step is to derive an equation for the output voltage at time $T(n+1)$. The voltage at $T(n+1)$ depends on the voltage at $T(n)$ and the capacitor voltage difference between those intervals:

$$v_O(n+1) = v_O(n) + \Delta v_{cap} \quad (A.7)$$

where Δv_{cap} is the voltage difference over the capacitor and can be written as the charge difference on the capacitor plates divided by the capacitance:

$$\Delta v_{cap} = \frac{\Delta Q}{C} \quad (A.8)$$

This charge difference can be written as the capacitor current during time T_s , multiplied by this period:

$$\Delta Q = i_{cap} T_s \quad (A.9)$$

Figure A.2: The sense voltage and control voltage v_c waveforms.

The capacitor current can be obtained from Fig. A.1, by subtracting the current in the load resistor R_L from the inductor current i_L :

$$i_{cap} T_s = i_L T_s - i_{RL} T_s \quad (A.10)$$

The current i_{RL} through R_L during period T_s is equal to the voltage over the resistor, which is v_O , divided by the resistance R_L :

$$i_{RL} T_s = \frac{v_O(n)}{R_L} T_s \quad (A.11)$$

The sampling time or clock period T_s can be split into the intervals t_1 and t_2 as shown in Fig. A.2, this is convenient, because from Fig. A.2 the average inductor currents during those intervals can be obtained. The charge flowing through the inductor during T_s can be written as:

$$i_L T_s = \bar{i}_{L t_1} \cdot t_1 + \bar{i}_{L t_2} \cdot t_2 \quad (A.12)$$

where $\bar{i}_{L t_1}$ is the average inductor current during time interval t_1 as seen in Fig. A.2. The average inductor current during t_1 is:

$$\bar{i}_{L t_1} = \frac{i_L(n) + i_{LP}(n)}{2} \quad (A.13)$$

the average inductor current during t_2 is:

$$\bar{i}_{L t_2} = \frac{i_{LP}(n) + i_L(n+1)}{2} \quad (A.14)$$

By substituting, (A.10) can now be written as:

$$i_{cap} T_s = \frac{i_L(n) + i_{LP}(n)}{2} t_1 + \frac{i_{LP}(n) + i_L(n+1)}{2} t_2 - \frac{v_O(n)}{R_L} T_s \quad (A.15)$$

Substituting this into (A.7), the following expression is obtained:

$$v_O(n+1) = v_O(n) + \frac{i_L(n) + i_{LP}(n)}{2C}t_1 + \frac{i_{LP}(n) + i_L(n+1)}{2C}t_2 - \frac{v_O(n)}{R_L C}T_s \quad (\text{A.16})$$

Substituting (A.1) through (A.5) gives us $v_O(n+1)$ in terms of $i_L(n)$, $v_C(n)$ and $v_O(n)$:

$$\begin{aligned} v_O(n+1) = v_O(n) &- \frac{R_s^2 V_{dd} i_L^2(n)}{LC \left(\frac{R_s V_{dd}}{L} - \frac{R_s v_O(n)}{L} + M_c \right)^2} + \frac{R_s V_{dd} i_L(n) v_C(n)}{LC \left(\frac{R_s V_{dd}}{L} - \frac{R_s v_O(n)}{L} + M_c \right)^2} \\ &- \frac{1}{2} \frac{V_{dd} v_C(n)^2}{LC \left(\frac{R_s V_{dd}}{L} - \frac{R_s v_O(n)}{L} + M_c \right)^2} + \frac{T_s i_L(n)}{C} - \frac{R_s V_{dd} T_s i_L(n)}{LC \left(\frac{R_s V_{dd}}{L} - \frac{R_s v_O(n)}{L} + M_c \right)} \\ &+ \frac{V_{dd} T_s v_C(n)}{LC \left(\frac{R_s V_{dd}}{L} - \frac{R_s v_O(n)}{L} + M_c \right)} - \frac{1}{2} \frac{T_s^2 v_O(n)}{LC} - \frac{T_s v_O(n)}{R_L C} \end{aligned} \quad (\text{A.17})$$

A.2 Small Signal Discrete-time Model

By assuming only small perturbations in i_L , v_C and v_O , the model can be linearized using the following substitutions:

$$i_L(n+1) \rightarrow I_L(n+1) + i_l(n+1) \quad (\text{A.18})$$

$$i_L(n) \rightarrow I_L(n) + i_l(n) \quad (\text{A.19})$$

$$v_C(n) \rightarrow V_C(n) + v_c(n) \quad (\text{A.20})$$

$$v_O(n) \rightarrow V_O(n) + v_o(n) \quad (\text{A.21})$$

$$v_O(n+1) \rightarrow V_O(n+1) + v_o(n+1) \quad (\text{A.22})$$

where the capital letters denote DC steady state terms and the lower case ones the small signal variations. By discarding DC-terms and higher order small signal terms (like $v_o(n) \cdot i_l(n)$), the following linear small-signal difference equations are obtained:

$$i_l(n+1) = k_0 i_l(n) + k_1 v_o(n) + k_2 v_c(n) \quad (\text{A.23})$$

$$v_o(n+1) = k_3 i_L(n) + k_4 v_o(n) + k_5 v_c(n) \quad (\text{A.24})$$

The k -coefficients can be obtained from (A.6) and (A.17) after applying the perturbations as described above. It is assumed that the large signal term $I_L(n+1)$ is equal to $I_L(n)$, this is the same as assuming that $I_L(n)$ is a DC term and does not change over time. The value of $I_L(n)$ is equal to the average of the inductor current minus half the ripple, as can be seen from Fig. A.2. The average inductor current is

$$I_{\text{avg}} = \frac{V_{\text{dd}} D}{R_L} \quad (\text{A.25})$$

and the current ripple is

$$I_{\text{ripple}} = \frac{M_1 t_1}{R_s} = \frac{M_1 D T_s}{R_s} \quad (\text{A.26})$$

so the DC inductor current at $T(n)$ becomes

$$I_L(n) = \frac{V_{\text{dd}} D}{R_L} - \frac{1}{2} \frac{M_1 D T_s}{R_s} \quad (\text{A.27})$$

Furthermore the DC term of the output voltage of the buck converter is assumed to be:

$$V_O(n) = D V_{\text{dd}} \quad (\text{A.28})$$

this is true for low voltage ripple. The DC term $V_C(n)$ is obtained by rewriting (A.3) and taking only the DC term of the inductor current:

$$V_C(n) = t_1(M_1 + M_c) + R_s I_L(n) \quad (\text{A.29})$$

where

$$t_1 = D \cdot T_s \quad (\text{A.30})$$

The following k -coefficients are obtained:

$$\begin{aligned} k_0 &= -\alpha = -\frac{M_2 - M_c}{M_1 + M_c}, & k_1 &= \frac{\alpha T_s}{L} - \frac{M_1 T_s}{L(M_1 + M_c)} \\ k_2 &= \frac{V_{\text{dd}}}{L(M_1 + M_c)}, & k_3 &= \frac{M_c T_s}{C(M_1 + M_c)} \\ k_4 &= 1 - \frac{T_s}{R_L C} - \frac{1}{2} \frac{T_s^2}{LC} + \frac{T_s^2 M_1 D}{LC(M_1 + M_c)}, & k_5 &= \frac{(1-D) T_s V_{\text{dd}}}{LC(M_1 + M_c)} \end{aligned}$$

A.3 State Space Model & Transfer Functions

Now that we have the model in the form of (A.23) and (A.24), it can be represented in the general state-space form:

$$\mathbf{x}[n+1] = A\mathbf{x}[n] + B\mathbf{u}[n] \quad (\text{A.31})$$

where

$$\mathbf{u}[n] = v_c(n) \text{ and } \mathbf{x}[n] = \begin{bmatrix} i_l(n) \\ v_o(n) \end{bmatrix}$$

$$A = \begin{bmatrix} k_0 & k_1 \\ k_3 & k_4 \end{bmatrix}, B = \begin{bmatrix} k_2 \\ k_5 \end{bmatrix}$$

By using the z-transform, the control-to-inductor current and the control-to-output voltage can be found as

$$z\mathbf{x}(z) = A\mathbf{x}(z) + B\mathbf{u}(z) \quad (\text{A.32})$$

can be rewritten to

$$\frac{\mathbf{x}(z)}{\mathbf{u}(z)} = (zI - A)^{-1}B \quad (\text{A.33})$$

where I is the identity matrix and $\mathbf{x}(z)$ is a vector of the inductor current and the control-to-output voltage. The control-to-inductor current transfer function can be written as:

$$T_{ci}(z) = \frac{i_l(z)}{v_c(z)} = \frac{k_1k_5 - k_2k_4 + k_2z}{z^2 + (-k_0 - k_4)z + k_0k_4 - k_1k_3} \quad (\text{A.34})$$

The control-to-output voltage transfer function can be written as:

$$T_{co}(z) = \frac{v_o(z)}{v_c(z)} = -\frac{k_0k_5 - k_2k_3 - k_5z}{z^2 + (-k_0 - k_4)z + k_0k_4 - k_1k_3} \quad (\text{A.35})$$

These z-domain transfer functions are compared to simulation chapter 4 to verify that they accurately describe the PWM based buck converter, both for resistive and capacitive load.

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LIST OF PUBLICATIONS

Peer reviewed journal articles

- **S. Amir**, R. van der Zee and B. Nauta, "A Self-Oscillating Boosting Amplifier With Adaptive Soft Switching Control for Piezoelectric Transducers," in IEEE Journal of Solid-State Circuits, vol. 54, no. 1, pp. 253-265, Jan. 2019.
doi: 10.1109/JSSC.2018.2871633
- **S. Amir**, R. van der Zee and B. Nauta, "An Improved Modeling and Analysis Technique for Peak Current-Mode Control-Based Boost Converters," in IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 5309-5317, Sept. 2015.
doi: 10.1109/TPEL.2014.2368176

ACKNOWLEDGEMENTS

WATU IZZU MANTASHA WATU ZILLU MANTASHA.

Firstly all praise to Allah Almighty for giving me strength and blessings to complete this endeavour. He showed me time and again that hard work always pays off.

Time flies and memories last forever and finally after many years I am writing the part of the thesis which comes at the end, but reminds me that a PhD is not just about technical stuff, it teaches you more than that. My desire to do the PhD research in an excellent group led me to contact Prof Bram Nauta, head of Integrated Circuit Design (ICD) Group in 2011 and that was the start of an amazing yet a very demanding journey of my life.

I would like to thank my promoter Bram Nauta and co-promoter Ronan for putting their trust in me and giving me an opportunity to work at ICD group. Thanks to Bram for showing me that one should always strive for the best to achieve great things. It was always encouraging to have discussions with you.

I am especially thankful to my daily supervisor Ronan for always providing me with the right motivation and availability throughout this long journey. Ronan's realistic approach over my extreme optimism not only made things possible but also kept me going even after my PhD contract was finished. His availability was always a message away and I cannot be more thankful to him for spending endless hours in reviewing my thesis. He is not only a great supervisor but an amazing human being. Your constant encouragement and cool headedness played a key role in finishing this thesis. Thank you Ronan !

I would like to thank Gerard Wienk for helping me resolve CAD related problems and special thanks to Henk de Vries for his help during the measurement phase. He took extra effort to solve my mounting issues of the chip which eventually made the chip to work. Thanks to Gerdien Lammers, the management assistant of our group for always being there and solving all administrative issues. Thank you so much for arranging everything flawlessly up till the end. I would also like to thank other members of the staff Dr. Eric Klumperink, Dr. A.J. Annema and prof. Dr. F.E. van Vliet for all the valuable discussions during chip talks. Special thanks to Mark for introducing me to Bruco, which helped me get my first job in Netherlands.

My gratitude goes to my former colleagues of the ICD group Milad, Shaadi, Ramen, Remco, Amir, Dlovan, Dawei, Erik, Ines, Harish, Michael, Drik Jan, Harijot, Reda, Johan and Hugo. I learned a lot from all of you guys. Special thanks to Saqib Subhan for all your support during the first few years and helping me get my first Gazelle bike (which is still with me and runs perfect).

I cannot forget to mention, Haifeng Ma, a person who helped me a lot with technical stuff specially during stressful phase of the design. Thanks a lot for that. My room-mate, Claudia whom with I shared many ups and downs during this journey, finally we both made it and that makes me really happy. My former colleague at ICD and later at ItoM, Vishal, grateful for all your help during every phase. Thanks to my fellow PhD students within SeaSTAR project Koen and Wouter for having many fruitful discussion and encouragement. Big thanks to NWO/TTW, the Dutch Technology Foundation for funding the project, Holst Centre Netherlands for silicon donation and Stefano Stanzione for his support during layout.

I would also like to thank few people who made it possible for me stay in Netherlands. Edwin, Lex and Jelle, my former colleagues at Bruco and later at ItoM. Thanks a lot for proving me opportunity to work and do my PhD work in parallel. Also thanks to Erwin, Marc, Eisse, Froukje, Leonie, Frank, Jelmer and Egbert, at ItoM Enschede. You guys made me practice my Dutch. Thanks for all the support. Also a big thanks to Angelo

at Infineon, you have been very supportive, understanding my special situation you went out of your way to help me out.

Life in Enschede would not have been so fun, without having my Pakistani friends around. I would like to thank Adeel, Naveed, Yawar, Mehdi, Ibrahim, Tauseef, Faizan, Ghazanfer and Jahanzeb for making life memorable in Enschede. Special thanks to Sohail bhai for his calm and supportive attitude. Similarly Afzal bhai has been like an elder brother and I will always cherish your unconditional support.

All this would not have been possible without the prayers of my parents and father in law. Whenever I needed emotional, financial or moral support, you were always there and still are. It is my parents who made me what I am today. I cannot find words to thank my father who is a role model for me. Your dream to see me having a PhD always kept me going. You have taught me the strongest attribute in life of "Never giving up". My gratitude goes to my brother Assad, my sister Sumbal, Saima bhabhi and Ali for being so supportive and taking care of the parents so well that I could focus on my work. Allah bless you all!

Lastly, words are not enough to thank my wife Sana with whom I started this journey. You stood strong during those rough times with a smile and kept my spirits high. You are not only an amazing wife but a selfless human being. Despite my mood spikes, working on weekends and having almost no time for the family, you never complained. Thanks for being there!. My both sons Haadi and Hashir you are the reason for all the comfort I got at end of those tiring days. Your love and smiles made me forget all the worries. Hopefully I will be able to compensate for the lost time I could not give you before.

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Enschede, October 2020.

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