Low-Power High-Linearity Mixer-First Receiver Using Implicit Capacitive Stacking With 3× Voltage Gain

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Abstract— In this article, we present a passive mixer-first receiver front end providing a low-power integrated solution for high interference robustness in radios targeting Internet-of-Things (IoT) applications. The receiver front end employs a novel N-path filter/mixer, a linear baseband amplifier, and a step-up transformer to realize sub-6-dB NF and >20-dBm OB-IIP3 concurrently. The proposed N-path filter/mixer exploits an implicit capacitive stacking principle to achieve passive voltage gain of 3 during down-conversion and high out-of-band linearity simultaneously while using at least 2× less total capacitance for the same RF bandwidth compared to a conventional switch-capacitor N-path filter. Fabricated in 22-nm complementary metal–oxide–semiconductor (CMOS) fully depleted silicon on insulator (FDSOI), the receiver prototype—including a 2:6 transformer—occupies only 0.2 mm^2 of active area. Operating in the frequency range of 1.8–2.8 GHz, the front end provides a 45–47-dB conversion gain and a baseband bandwidth of 2 MHz. Due to passive voltage gain in the filter/mixer and transformer, the implemented front end consumes only 1.7–2.5 mW of power to achieve <6-dB NF, ~24/60/1 dBm out-of-band IIP3/IIP2/B1dB, respectively.

Index Terms— Bottom-plate mixing, complementary metal–oxide–semiconductor (CMOS), capacitive stacking, fully depleted silicon on insulator (FDSOI), high linearity, interference-robust, low power, low noise, mixer-first receiver, N-path filter, passive mixer, transformer.
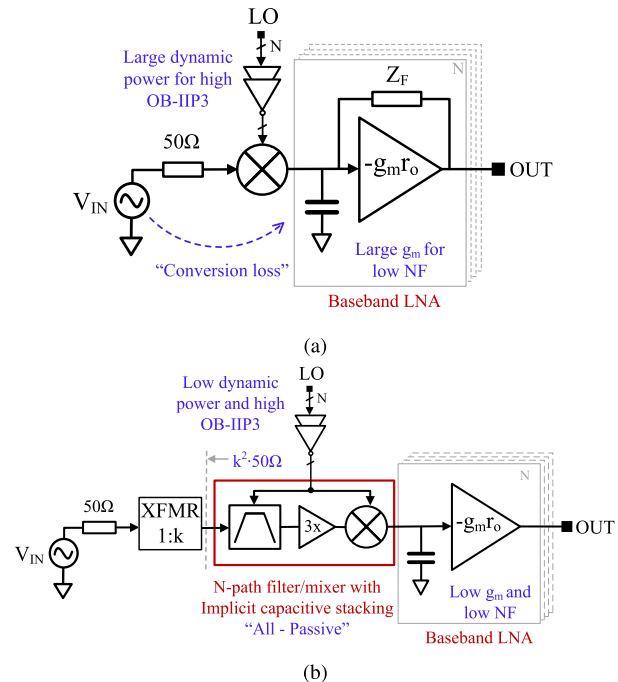

Fig. 1. (a) Typical passive mixer-first RX front end and (b) proposed front end using an N-path filter/mixer with implicit capacitive stacking.

I. INTRODUCTION

INTERNET-OF-THINGS (IoT) platform connects approximately 10 billion devices in 2019 and is expected to double the connectivity in the next four to five years [1]. Enabled by technologies, such as Bluetooth, Wi-Fi, and NB-IoT [2], [3], these IoT radios are crowding the already congested low-GHz spectrum. As such, interference tolerance is becoming indispensable for low-power IoT receivers. This article presents an interferer-robust low-power complementary metal–oxide–semiconductor (CMOS) receiver front end that can be employed for IoT applications in the low-GHz spectrum.

In CMOS, passive mixer-first circuits have become a popular topology for receivers targeting large interferer tolerance and low noise figure simultaneously [4]–[13]. They achieve >20-dBm out-of-band (OB-) IIP3, 2–6-dB noise figure (NF), and >0-dBm OB-blocker tolerance, albeit, at the cost of power consumption, usually in the range of 10–100 mW [4]–[10]. A typical passive mixer-first receiver front end is shown in Fig. 1(a). The main power-consuming blocks in the front end are baseband low-noise amplifiers (BB-LNAs) at the mixer output and local-oscillator (LO) buffers, driving mixer switches. Large power consumption in BB-LNAs is due to: 1) the use of multiple amplifiers at the multiple mixer outputs and 2) the use of large transconductance (g_m) to limit the

NF degradation of mixer-first RX caused by switching loss of the passive mixers and non-zero switch resistance (R_{SW}). For example, the RX in [8] uses 50-mW I/Q BB-LNAs with a g_m of 360 mS to achieve 2.3-dB NF, while the RX in [10] uses a 19.8-mW noise-canceling BB-LNA with a combined g_m of 24 mS for 4-dB NF. As seen in the figure, the BB-LNAs are often used as trans-impedance amplifier (TIA) with shunt-feedback impedance either to realize 50 Ω matching [4], [5] or virtual ground [14] at the baseband terminals of the mixer and achieve high in-band linearity. Recently, techniques with higher order impedance roll-off at the baseband terminals of mixer [8]–[13] have been proposed to improve the linearity of the receiver in the presence of nearby blockers. Such linearity-enhancement techniques consume high power as they also require baseband amplifiers with large transconductance [8] and high loop gain [14], and, sometimes, auxiliary amplifiers [12], [13]. For example, the RX in [9] spends 21.6-mW power in a 1.8-V I/Q TIA, while the RX in [12] burns 143 mW of power in BB-LNAs and auxiliary amplifiers to realize 40-dB roll-off at the mixer output.

The OB linearity of a mixer-first RX at far-off frequencies depends on the ratio of R_{SW} and driving impedance, R_S [15]. This incites these RXs to use wide mixer switches with small R_{SW} values for high interferer tolerance and low NF at the cost of power in LO buffers, driving these switches. For example, the RXs in [11] and [12] use R_{SW} of 1 and 1.5 Ω for 44- and 33.3-dBm OB-IIP3, respectively. To drive these switches, dividers and LO buffers consume 33 mW/GHz in [11] and 18 mW/GHz in [12].

A survey of the state-of-the-art passive mixer-first RXs, benchmarking their NF and OB-IIP3 performance with their power consumption, is shown in Fig. 2. All the reported receivers in the figure have one or more stages of baseband amplification, and their maximum OB-IIP3, achieved for far-off interferers, and in-band double-sideband (DSB) NF are used for comparison. As seen in the survey, mixer-first RXs tend to trade off their OB-IIP3 performance for low power consumption, for example, by using small mixer switches with poor linearity. Interestingly, the NF degradation, due to large R_{SW}, in some low-power RXs is reduced by using techniques, such as passive matching networks [16]–[20] and active gain-boosted switch capacitor [21]. By providing voltage amplification, these techniques facilitate low NF in the passive mixer-first RXs without using power-hungry BB-LNAs, albeit at degraded linearity.

Recently, the authors presented a 600-μW RF front end [22] that uses an implicit capacitive stacking technique, resulting in 2× voltage gain (6 dB V/V) in a passive 4-path filter, and a step-up transformer to achieve both high linearity (25-dBm OB-IIP3) and 6-dB NF at 1 GHz. However, with an off-chip transformer and no BB-LNAs, the front end in [22] is far from an integrated RX. In this article, we propose a mixer-first RX topology that uses a new 4-path filter with an implicit capacitive stacking technique providing 3× passive voltage gain (9.5 dB V/V), which is 3.5 dB more than [22] and ~9.5 dB more than the typical differential-ended mixer-first RXs [4], [11]. Moreover, it achieves >2× narrower RF bandwidth than [22] for a given RF capacitance and LO power.
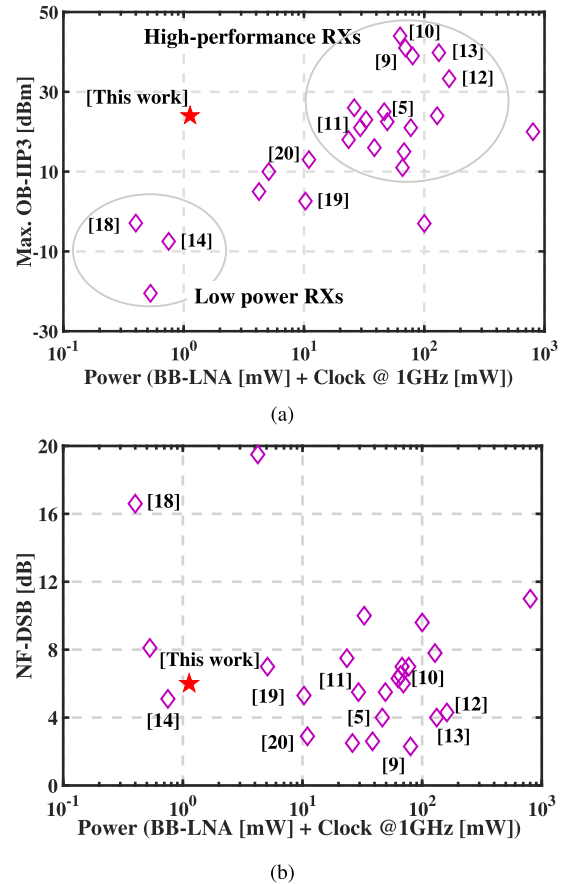

Fig. 2.   Survey of (a) OB-IIP3 and (b) NF performance of the state-of-the-art low-GHz passive mixer-first RXs. Please note that the dynamic power of the RX is scaled to 1 GHz here for comparison.

As shown in Fig. 1(b), the proposed RX also includes: 1) an on-chip transformer (XFMR) to realize a balun at the RF input and achieve extra passive voltage gain and high OB-IIP3 using small MOS switches and 2) a linear BB-LNA. The proposed RX front end realizes impedance matching using parasitic capacitances in the 4-path filter/mixer. Hence, voltage-mode BB-LNAs are used in this front end instead of conventional shunt-feedback BB-LNAs. To the best of our knowledge, the proposed RX front end consumes the least reported power to simultaneously achieve <6-dB NF and ≥24-dBm OB-IIP3 (see Fig. 2) while operating in 1.8–2.8-GHz LO range. The insights on design optimization and performance of the 4-path filter with 3× voltage gain due to implicit capacitive stacking are discussed in Section II. The RX topology and the circuit details are explained in Section III. Section IV presents the measurement results of the experimental prototype. Finally, Section V wraps up the article with conclusions.

II. N-Path Filter/Mixer With 3× Voltage Gain

Bottom-plate switch-capacitor filter/mixers [11] can fundamentally achieve higher linearity than top-plate switch-capacitor variants [23]. As shown in Fig. 3, they are used as a frequency-tunable RF bandpass filter with a passband loss of 1.8 dB, in front of an I/Q passive mixer in an RX front end [11]. In this section, we present a novel N-path filter with
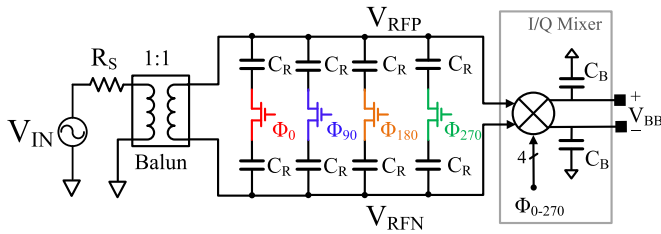
Fig. 3. Typical RX front end with a 4-path bottom-plate filter and an I/Q top-plate mixer, inspired by Lien *et al.* [11].
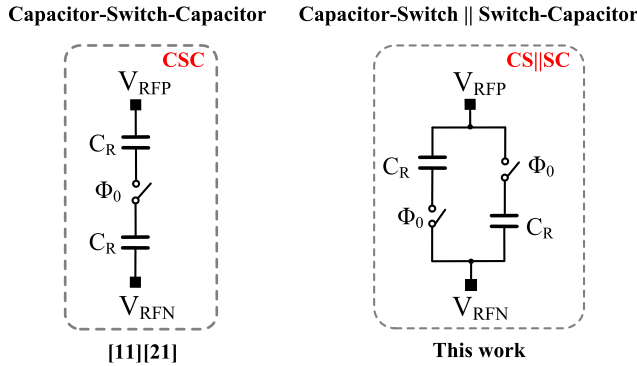

Fig. 4. Capacitor-switch-capacitor (CSC) network and proposed capacitor-switch ∥ switch-capacitor combination (CS∥SC).

a voltage mixer, providing passive voltage amplification of 9.5 dB at down conversion and high out-of-band linearity.

A. Topology

The proposed N-path filter/mixer topology comprises a parallel combination of a capacitor-switch and switch-capacitor (CS∥SC) network in each path compared to capacitor-switch-capacitor (CSC) network in a typical differential bottom-plate filter [11], as shown in Fig. 4. Both switches in the CS∥SC combo are driven by the same LO phase as in the CSC branch. Please note that each capacitor in the CS∥SC combo sees the full swing of the differential input compared to half the swing across each capacitor in a CSC branch, which is the case in [22], assuming negligible R_{SW}. Hence, when the filtered RF signal is down-mixed from the bottom-plates of the capacitors in CS∥SC combo, the proposed topology provides $3\times$ voltage gain, instead of $2\times$ gain, as in [22], by the virtue of implicit capacitive stacking. This is explained below in detail using Fig. 5.

To explain the operation, let us first assume that the differential RF input is applied using an ideal 1:1 transformer. Please note that, in our receiver prototype, we will use a step-up transformer providing source impedance up-conversion at the RF input. Hence, the capacitances and switch resistances used in the prototype will be different than the ones used in this section. Each CS∥SC network consists of capacitors, C_R, and switches (S_{1-8}), driven by 4-phase non-overlapping LO signals $\phi_0 - \phi_{270}$, operating at a frequency, f_{LO}. The bottom-plate terminals (A_x, B_x) of the capacitors C_R of each CS∥SC combo are connected to baseband capacitors, C_B, using I/Q

mixer switches (M_{1-8}). Here it is assumed that both the CS∥SC combo and I/Q mixers are operating in the "mixing regime" where $T_{ON} \ll RC$ [24]. Hence, for an input sinusoidal with frequency, $f_{RF} \approx f_{LO}$, it will take many LO cycles for each C_R to settle to a quasi-DC voltage. The steady-state voltage on each C_R is the average of the RF input voltage that it sees during the on-time of its corresponding switch. Assuming ideal switches with negligible R_{SW}, the voltage at the RF nodes (V_{RFP}, V_{RFN}) is a time-multiplexed version of these capacitor voltages, providing narrow-band RF N-path filtering around $f_{RF} = f_{LO}$. Now, let us consider the red-slice of CS∥SC combo in Fig. 5, which is clocked by phase ϕ_0. For $f_{RF} = f_{LO}$, let the average DC voltage across both the C_R capacitors in the red-slice be $2V_0$. Due to differential symmetry, the RF voltages at V_{RFP} and V_{RFN} would be $\pm V_0$ during the phase ϕ_0. When observed from the bottom-plate terminals (A_0, B_0) of C_R, the dc voltage $2V_0$ in C_R can be seen stacked upon the RF voltages, V_{RFP} and V_{RFN}. It means that the voltage at terminal B_0 would be $2V_0 + V_{RFN}$, which is equal to $3V_0$, during ϕ_{180}, since V_{RFN} is equal to $+V_0$ in this phase. Likewise, the voltage at A_0 during ϕ_{180} would be $-3V_0$. These voltage-boosted RF signals at terminals A_0 and B_0 are down-mixed onto baseband capacitors with capacitance C_B, using switches $M_{1,2}$, clocked by ϕ_{180}. The half-a-period delay between LO clocks of filter and mixer switches is essential to maximize the baseband voltages. Finally, since no explicit extra switches are needed to realize the addition, this can be seen as a new variant of the implicit capacitive stacking technique, as proposed in [22]. Since $2V_0$, rather than V_0 is present on the stacking capacitor, $3\times$, instead of $2\times$, the voltage gain is achieved.

B. Transfer Behavior

We will now compare the behavior of the proposed CS∥SC filter/mixer using implicit capacitive stacking to a typical top-plate mixer-first RX with a 4-path bottom-plate (CSC) filter at its input [11]. From now on, the former will be called CS∥SC RX and the latter as CSC RX for convenience. The circuit implementation of the CS∥SC RX is shown in Fig. 5, whereas that of CSC RX is presented in Fig. 3. Please note that the CSC RX does not employ implicit capacitive stacking. For the rest of the section, nMOS switches and capacitors, used in both RXs, are implemented in Global foundries 22-nm fully depleted silicon on insulator (FDSOI) process. The transfer functions of both RXs at RF ($V_{RFP/N}$) and baseband (V_{BB}) outputs are simulated using SpectreRF, and the results are presented in Fig. 6(a) and (b), respectively. As shown in Fig. 6(a), the RX with CS∥SC filter achieves narrower N-path filtering compared to the CSC RX. This is because the CSC capacitors are in series across the RF inputs, whereas the two CS∥SC capacitors are in parallel to the RF inputs (see Fig. 4). Hence, for a given C_R, the effective capacitance across the RF inputs in the CSC network is $C_R/2$, while that in CS∥SC combo is $2C_R$, at any time instant. This renders smaller bandwidth for the same amount of total capacitance ($8 \times C_R$). Alternately, to achieve equal RF bandwidth, the CSC filter requires $4\times$ larger capacitance than CS∥SC filter, as verified in Fig. 6(a). Strikingly, the CS∥SC
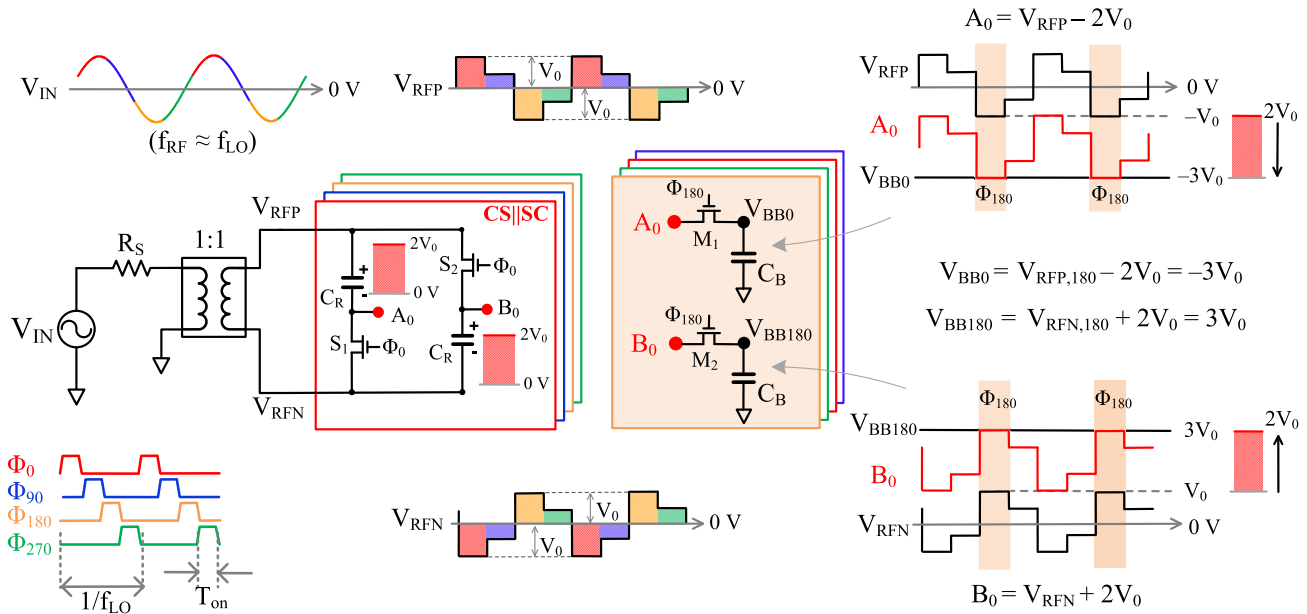
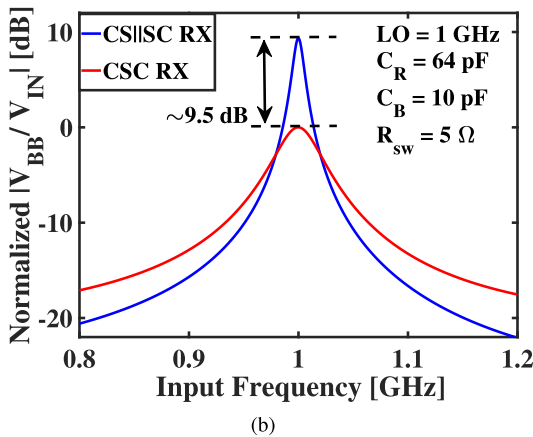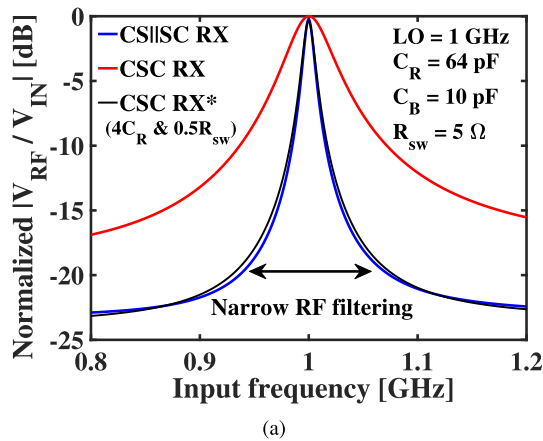Fig. 5.   Schematic of an RX front end with the proposed CS‖SC filter using implicit capacitive stacking technique.

Fig. 6.   Simulated (a) RF–RF gain, $V_{RF}(f)/V_{in}(f)$ and (b) RF–IF gain, $V_{BB}(f - f_{LO})/V_{in}(f)$ of a CSC RX (see Fig. 3) and a CS‖SC RX (see Fig. 5). The gain of the RXs is normalized to the peak gain of CSC RX in each graph.

Fig. 7.   Simulated RF–RF gain, $V_{RF}(f)/V_{in}(f)$ of the CS‖SC RX for different C_R and C_B capacitances, provided that $C_R + C_B = 74$ pF. The gain is normalized to its peak gain.

filter uses two switches per slice instead of one in CSC. Hence, its effective R_{SW}/R_S ratio is half of that of the CSC filter and, thereby, achieves $2\times$ better out-of-band rejection [23]

compared to the CSC filter, at the cost of $2\times$ LO power. Any mismatch between the switches in CS‖SC filter would degrade its IIP2 and LO re-radiation performance, similar to typical 4-path filters [11], [23].

As shown in Fig. 6(b), the proposed CS‖SC RX provides $\sim$9.5-dB extra voltage gain at down conversion for in-band frequencies and achieves narrower bandwidth than the CSC RX. Please note that high impedance at the output of down-mixer is essential for reading out the $3\times$ voltage-boosted signal from the bottom-plate terminals of C_R, as in [22]. Since the baseband capacitor, C_B, loads C_R at large frequency offsets, the voltage boosting degrades at these frequencies. Though it causes an extra order of filtering at the baseband output, the C_R capacitor and the switch resistance together introduce a zero at high frequencies, as derived in [22], and limit the filter roll-off to 20-dB per decade. The bandwidth of the CS‖SC RX depends on the sum of the C_R and C_B capacitances. This is highlighted in Fig. 7, which shows the simulated RF–RF gain of the proposed CS‖SC RX for different C_R and C_B capacitance combinations, provided that

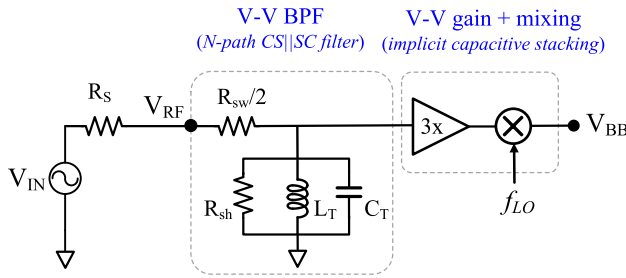This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

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Fig. 8. Simplified functional view of the proposed CS∥SC filter using implicit capacitive stacking to model its transfer behavior.

(a)

(b)

Fig. 9. Simulated and calculated (a) RF–RF gain, $V_{\mathrm{RF}}(f)/V_{\mathrm{in}}(f)$, and (b) RF–IF gain, $V_{\mathrm{BB}}(f - f_{\mathrm{LO}})/V_{\mathrm{in}}(f)$, of a CS∥SC RX for different R_s impedances.

their sum is constant. To a first order, the -3-dB bandwidth can be approximated to $1/8\pi R_s(C_R + C_B)$, assuming equal R_{SW} in filter and mixer switches and $R_{\mathrm{SW}} \ll R_s$, as in [22].

The filtering behavior of the proposed CS∥SC RX using implicit capacitive stacking around its LO frequency can be approximately modeled as a cascade of a bandpass RLC filter [11], [23], a linear amplifier, and an ideal mixer, as shown in Fig. 8. Similar to [11], [15], the RLC parameters in the bandpass filter can be derived as follows:

$$R_{\mathrm{sh}} = \frac{4\gamma}{1 - 4\gamma}(R_s + 0.5 \cdot R_{\mathrm{SW}}) \tag{1}$$

$$C_T = \frac{2\,C_R + 2\,C_B}{2\gamma} \tag{2}$$

$$L_T = \frac{1}{(2\pi f_{\mathrm{LO}})^2 C_T} \tag{3}$$

where $\gamma = 2/\pi^2$ for the 4-path filter [15]. Please note that the RLC bandpass filter models the CS∥SC structure only in its magnitude [11], [23]. Here, R_{SW} of the filter and mixer switches are assumed to be equal. The harmonic shunt impedance, R_{sh}, models the power loss in the antenna resistance due to signal re-up-conversion by the LO harmonics in passive mixers [25]. Due to the transparency of a passive mixer, the filtering behavior of both C_R and C_B is modeled using C_T at the RF node. L_T describes the frequency translation of filtering profile around f_{LO}. Due to two parallel switches and capacitors in the CS∥SC combo, the switch resistance is halved, and C_R is doubled in R_{sh} and C_T calculations, respectively. The $2C_R/2\gamma$ component in C_T is the same as C_p in [11, eq. (4)], while $2C_B/2\gamma$ accounts for the C_B loading of C_R in alternate LO phases and the consequent charge sharing between them. Since a double-balanced mixer is used for down-conversion in Fig. 5, the conduction time for each baseband capacitor, C_B, is doubled, thereby resulting in a 2γ factor in (2). The linear amplifier and the ideal mixer model the voltage gain and down-conversion behavior of the implicit capacitive stacking technique.

Please note that the functional view in Fig. 8 neglects the zero introduced by the R_{SW} and C_B to keep the analysis simple. For small R_{SW}, the zero is at far-off frequency compared to the operating bandwidth and can be safely neglected. Furthermore, small R_{SW} is preferred in the receivers targeting high out-of-band linearity [15], [22]. Using the functional view, the RF–RF and RF–IF transfer behaviors of the proposed
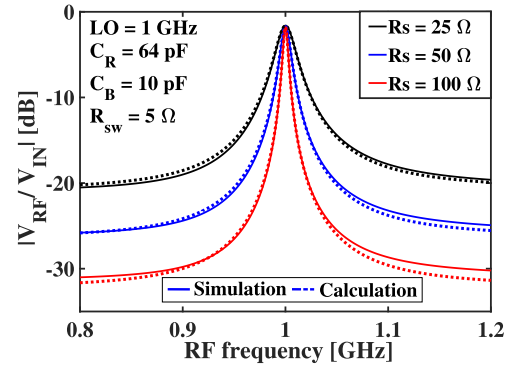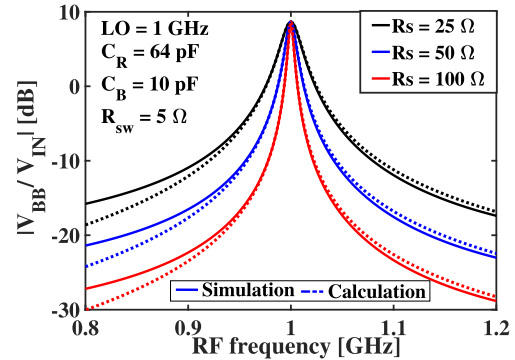
CS∥SC RX in Fig. 5 can be calculated as follows:

$$\frac{V_{\mathrm{RF}}}{V_{\mathrm{in}}} = \frac{Z_T + 0.5 \cdot R_{\mathrm{SW}}}{Z_T + R_s + 0.5 \cdot R_{\mathrm{SW}}} \tag{4}$$

$$\frac{V_{\mathrm{BB}}}{V_{\mathrm{in}}} = \frac{3 \cdot Z_T}{\sqrt{4\gamma}\,(Z_T + R_s + 0.5 \cdot R_{\mathrm{SW}})} \tag{5}$$

where Z_T is the effective impedance of the RLC tank and can be given as

$$Z_T = \frac{s L_T}{s^2 L_T C_T + s L_T/R_{\mathrm{sh}} + 1}. \tag{6}$$

The factor $\sqrt{4\gamma}$ in (5) accounts for the voltage gain between the RF and baseband terminals of an ideal passive mixer [11], [25]. The analysis is verified with the Spectre PSS/PXF simulation of the CS∥SC RX in Fig. 5. The calculated and simulated RF–RF and RF–IF transfer behaviors of the CS∥SC RX are shown in Figs. 9 and 10, along with the component values used. Fig. 9(a) and (b) shows the RF–RF and RF–IF conversion gains, respectively, for three different R_s values, whereas the same for different C_B capacitances is shown in Fig. 10(a) and (b). Here, the C_B capacitance is set to be smaller than, equal to, and larger than C_R capacitance. As seen in the figures, the functional view of CS∥SC RX predicts the transfer behavior reasonably well in all scenarios. Moreover, CS∥SC RX exhibits same 9.5-dB in-band RF–IF gain and similar filtering profile for different R_s, C_B, and C_R values.

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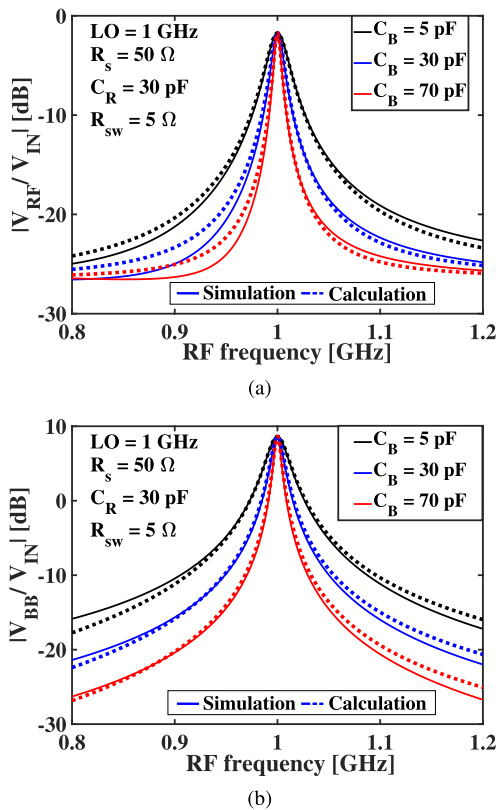
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Fig. 10. Simulated and calculated (a) RF–RF gain, $V_{RF}(f)/V_{in}(f)$, and (b) RF–IF gain, $V_{BB}(f - f_{LO})/V_{in}(f)$, of a CS‖SC RX for different C_B capacitances.
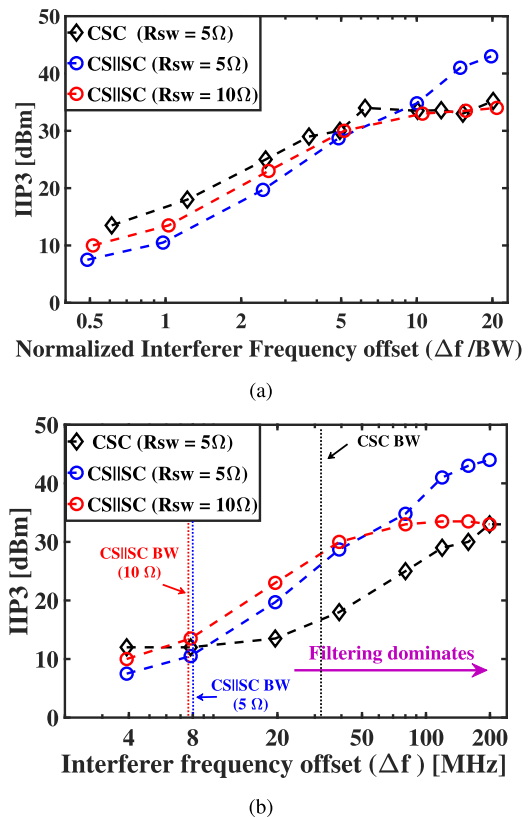

Fig. 11. Simulated IIP3 performance of a CSC RX (see Fig. 3) and a CS‖SC RX (see Fig. 5) with $f_{LO} = 1$ GHz, $C_R = 64$ pF, and $C_B = 10$ pF.

C. IIP3 Performance

The IIP3 performance of a passive mixer-first receiver at any frequency offset, Δf, can be simply improved by either scaling down R_{SW} at the cost of LO driving power or lowering the -3-dB RF bandwidth at the cost of capacitance area. Hence, for a fair comparison between the two passive mixer-first receiver techniques, it is essential that the mixers use the same effective R_{SW}/R_s ratio and provides the same -3-dB RF bandwidth. For the latter case, one can also normalize the frequency offset of the interferers with the -3-dB bandwidth of the circuit to de-embed the influence of bandwidth in the IIP3 comparison. An additional benefit in this approach of bandwidth normalization is that it allows the use of the same capacitance for both structures. It means that they occupy a similar area and have the same cost of implementation. In Fig. 11(a), we employ this approach of normalizing the frequency offset of interferers to compare the IIP3 performance of CS‖SC RX and CSC RX with different -3-dB bandwidths and the same effective switch resistance. Please note that the CS‖SC filter employs two parallel switches at any instant of time compared to one in the CSC filter. Consequently, the effective R_{SW}/R_s ratio of CS‖SC filter is half that of the CSC filter at large Δf. Hence, the IIP3 of a CS‖SC using an R_{SW} of 10 Ω should be compared with a CSC using 5-Ω R_{SW} for the same effective R_{SW}/R_s ratio and LO power. In addition, CS‖SC RX with R_{SW} of 5 Ω is also presented in Fig. 11(a) for reference. As seen in the figure, at smaller normalized interferer frequency offsets, Δf/BW,

the CS‖SC RX exhibits 4–6 dB worse IIP3 compared to CSC RX. This is because the switches S_{1-8} in CS‖SC filter are "top-plate" switch-capacitor exhibiting large gate-source voltage-related non-linearities compared to a CSC filter and a high-linearity bottom-plate switch capacitor variant [11]. In addition, switches M_{1-8} in the voltage boosted mixer see $3\times$ larger signal at their source–drain terminals, which worsens the IIP3 of CS‖SC further compared to CSC RX with no voltage gain at its top-plate mixer input. At far-off frequency offsets where the capacitive impedances in CS‖SC and CSC filters are negligible, both these filters have a similar structure, and hence, they exhibit more or less same IIP3 at these frequency offsets. This fits well with the analysis presented in (24) in [15] and the results presented in Fig. 6 in [11]. Please note that the in-band IIP3 of CS‖SC RX is still ~10 dBm, and it increases to >20 dBm for $\Delta f \geq 2 \times$ BW. Such large IIP3 implies that the linearity of subsequent baseband amplifiers will limit the overall IIP3 of the mixer-first RX at in- and transition-band frequencies, rather than the CS‖SC filter [8], [14]. Finally, the proposed CS‖SC filter achieves ~$4\times$ narrower RF bandwidth than the CSC filter for given C_R and R_{SW}. Due to this narrow bandwidth, the CS‖SC RX exhibits better IIP3 than CSC RX for close-by interferers, as shown in Fig. 11(b), while consuming a similar capacitance area and LO power as that of CSC RX.

D. Noise Performance

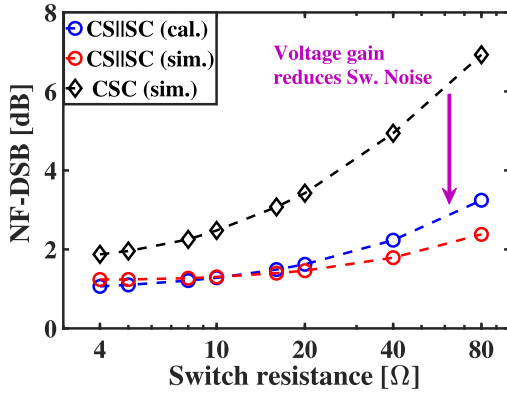Noise in the CS‖SC RX is due to the thermal noise of the filter and mixer switches and their harmonic folding due

Fig. 12. Simulated and calculated in-band NF versus resistance of an individual switch of a CSC RX and a CS∥SC RX with f_{LO} = 1 GHz, C_R = 64 pF, and C_B = 10 pF.

to the switching. The ∼9.5-dB voltage gain realized due to implicit capacitive stacking reduces the contribution of switch noise to the input-referred noise of the RX. Similar to [15], an approximate relation for the minimum noise factor of the proposed CS∥RX can be derived as

$$F \approx 1 + \frac{1}{K_{N0}} + \frac{2(R_{SW,F} + R_{SW,MX})}{R_S \cdot A_V^2}\left(1 + \frac{1}{K_{N0}}\right) \quad (7)$$

where K_{N0} is the noise folding factor accounting for harmonic folding of thermal noise of source/switch resistance, as defined in [15]. For a 4-path filter/mixer, K_{N0} would be ∼4.3. The second term accounts for harmonic folding of the noise of R_S, the source resistance. The third term describes the input-referred noise of the filter and mixer switches while accounting for harmonic folding and voltage gain, A_V, due to capacitive stacking. Since the noise of switches is directly sampled at the mixer output, the voltage gain is included here when their noise is referred to the input.

As shown in Fig. 12, the simulated noise figure of the CS∥SC RX fits well with the calculated results using (7) for different switch resistances. Compared to a CSC RX, the proposed RX provides better NF, especially for large switch resistances. Please note that, as the switch resistance decreases, the difference in NF between these two structures also reduces. This is due to the reduction in noise contribution of switches to the overall noise of the RX. For large switches, with small R_{SW}, the noise figure benefit of CS∥SC RX becomes small.

E. Impedance Matching via Parasitic Capacitance

C_R capacitors in the proposed CS∥SC filter are directly connected to the RF input terminals. Due to its parasitic capacitance to the substrate, the C_R capacitors introduce significant unwanted capacitance at the RF input and cause signal loss (due to low-pass filtering with R_S [11]). Depending on the process and layout, the parasitic capacitance, C_p, is a fraction of C_R in the implementation, e.g., 1.1% in [11] and 1.3% in [22]. By shunting the re-up-converted signal power at harmonic images, the parasitic capacitance also degrades the harmonic shunt impedance, R_{sh}, and the noise figure of the

proposed filter/mixer topology [11], [15]. Baseband amplifiers with complex shunt feedback can be used at the mixer output to mitigate the gain loss and impedance reduction due to parasitic capacitance [5], [8]. Alternately, the reduction in R_{sh} can be exploited to realize the desired input impedance without using baseband resistors [22].

The parasitic capacitance at the RF input causes mixer switches to see a complex source impedance ($R_s \parallel 1/C_p$) [15]. Due to switching action, the complex source impedance results in frequency-dependent harmonic shunt impedance, $R_{sh}(\omega_{LO})$ [11, eq. (9)]. By optimally sizing the C_R, the total parasitic capacitance at the input terminals can be tuned such that the resulting R_{sh} matches with R_S at the desired LO frequency. For a given R_{SW} and R_S, the −3-dB baseband bandwidth of the proposed 4-path filter/mixer topology is proportional to the sum of the RF and BB capacitors, ($C_R + C_B$). Since C_R for a given LO frequency is defined by the impedance matching requirement, the maximum achievable baseband bandwidth of the proposed topology is also limited. On the other hand, this bandwidth can be reduced orthogonally by tuning C_B capacitors. As its parasitic capacitance is isolated from the input terminals by mixer switches, M_{1-8} and C_R, C_B capacitors will not influence the R_{sh}. Similar to conventional resistor-termination matching [26], this parasitic capacitance-based impedance matching limits the minimum achievable NF of the receiver to 3 dB.
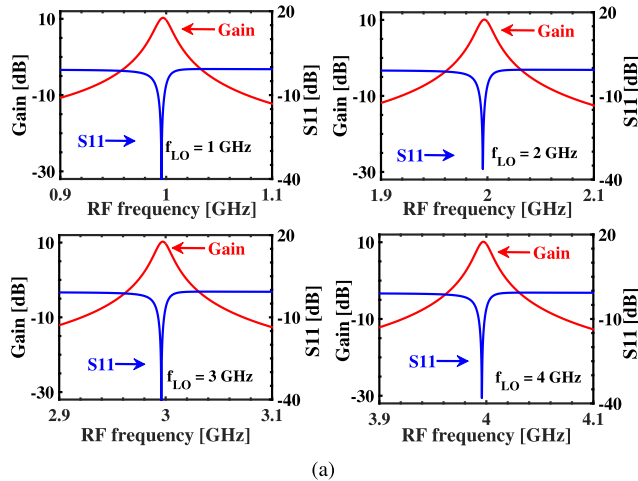
To substantiate the aforesaid discussion, the capacitors with parasitic capacitance model are used in the CS∥SC RX for simulation. The results are presented in Fig. 13(a) and (b). Here, $C_R + C_B$ is sized to be 74 pF in each path [see Fig. 13(c)] to achieve both 50 Ω matching and −3-dB BB bandwidth of ∼8.5 MHz, an arbitrary choice, in the LO frequency range of 1–4 GHz. The C_R and C_B values are varied in the specified LO frequency range, while their sum value remains at 74 pF. Similar in-band RF–IF gain and filtering behavior is noticed in all these scenarios. Due to 3× voltage gain, the contribution of the filter/mixer switches to the input-referred noise is reduced, and the RX achieves the expected 3-dB NF in the simulated LO frequency range. Please note that the required $C_R + C_B$ value for a given BB bandwidth can be reduced using a step-up transformer as it up-converts the R_s seen by the CS∥SC RX. The up-converted R_s also requires low parasitic capacitance C_p and, thus, low C_R for impedance matching.

III. PROPOSED RECEIVER TOPOLOGY

The receiver in this work is designed for the target specifications of ≥25-dBm OB-IIP3, ≤5-dB NF, and a center frequency of 2.4 GHz while consuming power as low as possible. The circuit schematic of the proposed receiver front end is shown in Fig. 14. At the top level, it comprises an all-passive RF front end, I/Q baseband amplifiers, and multiphase LO generation circuitry. The implementation details of the receiver blocks are discussed in the following.

A. All-Passive RF Front End

The transformer, a 4-path CSC filter combined with the proposed CS∥SC filter, and a voltage mixer constitute an

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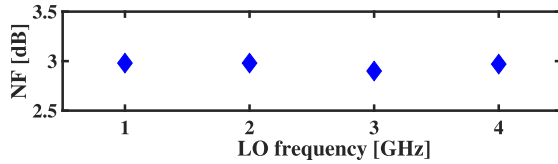
Fig. 13.   (a) Simulated conversion gain, S_{11}, and (b) in-band noise figure of the proposed CS∥SC RX with $R_{SW} = 5$ Ω for multiple LO frequencies. (c) C_R and C_B values used to achieve $S_{11} < -20$ dB and ∼8.5-MHz BB bandwidth.

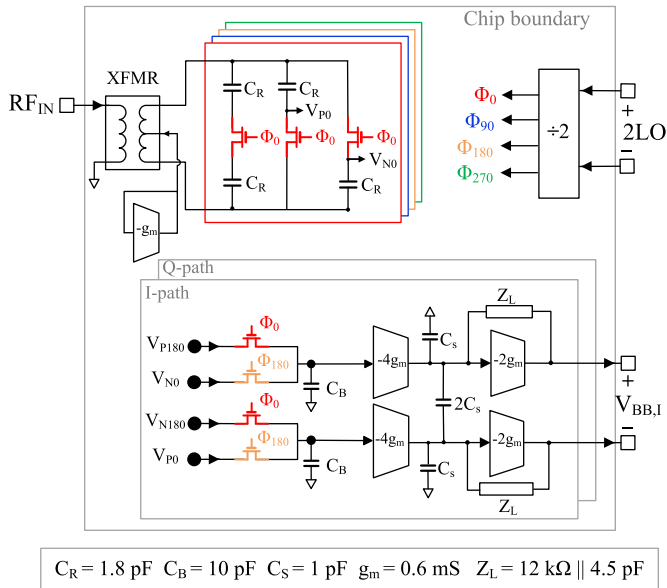
Fig. 14.   Top-level schematic of the proposed mixer-first receiver front end.

all-passive RF front end, providing impedance matching, voltage gain, filtering, and down-mixing at high linearity.

A step-up transformer is used at the input of the proposed receiver topology: 1) to convert single-ended RF input to differential RF signal; 2) to provide extra passive
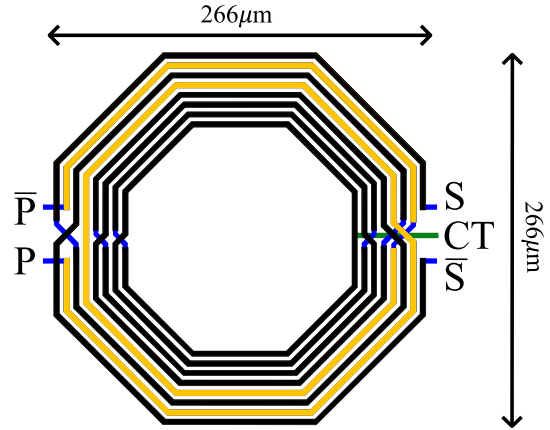

Fig. 15.   Physical layout of 2:6 planar transformer, showing primary (P_1, P_2) and secondary (S_1, S_2) terminals.

voltage amplification; and 3) to up-convert the 50 Ω antenna impedance to large R_S at the mixer input. This facilitates high even-order harmonic rejection [8], moderate noise figure [19], and high OB-IIP3 [22] in the proposed receiver. Hence, a high turn ratio and large fractional bandwidth are desired in the transformer. However, the on-chip coils have limited Q (≤ 15), resulting in more insertion loss, compared to off-chip transformers [22], [26], [27]. With the increase in the transformer turn ratio, the magnetic coupling decreases due to far-off secondary coils, while the self-resonance frequency also decreases due to parasitic capacitive coupling [19]. Hence, in this work, we limit the physical turn ratio to 2:6 for operation around 2.4 GHz. Please note that the insertion loss of the transformer describes the maximum power transfer between the primary and secondary terminals of the transformer when the terminals are impedance-matched. It means that any insertion loss of the transformer would directly add to the noise figure of the impedance-matched receiver. Hence, it is essential to minimize the insertion loss for the selected configuration.

The layout of the implemented planar transformer with two-turn primary and six-turn secondary coils is shown in Fig. 15. Coils are implemented in the top-most copper layer to reduce substrate parasitics [28]. Electromagnetic-Momentum simulations are used to optimize the physical parameters of the transformer for low insertion loss and high self-resonance frequency. The coils have width, thickness, and spacing of 4, 3, and 3 μm, respectively, and occupy a total area of 266×266 μm^2.

From EM-Simulations, the magnetizing inductances realized at the primary and secondary coils are 2.1 and 11 nH, respectively, with a coupling coefficient, k, of 0.72. The primary and secondary coils achieve a maximum Q of 7.7 and 12.7. Shunt capacitors are used at both primary and secondary terminals to tune the frequency range and minimize the insertion loss around 2.4 GHz. On the secondary side, the parasitic capacitances of N-path and CS∥SC filters are adapted as tuning capacitors. The transformer stand-alone provides close to 8-dB voltage gain with an insertion loss of ∼1.5 dB around 2.4 GHz. It up-converts the 50 Ω antenna resistance at the primary to ∼270 Ω at the secondary terminal. The up-converted

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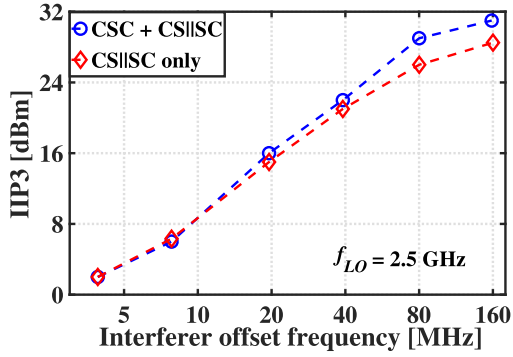PURUSHOTHAMAN *et al.*: LOW-POWER HIGH-LINEARITY MIXER-FIRST RECEIVER

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Fig. 16. Simulated IIP3 performance of the RX with the transformer at the input using (a) CS∥SC filter only and (b) both CS∥SC and CSC filters. Here, $C_R = 1.8$ pF, $C_B = 10$ pF, and $R_{SW} = 39$ Ω.

Fig. 17. Achievable receiver NF versus g_m in the baseband amplifier of the proposed RF front end and comparison with other RXs.

impedance is less than the expected $450 \, \Omega (= 50 \, \Omega \times (6/2)^2)$ due to limited magnetic coupling between the primary and secondary coils of the transformer [27].

The differential RF signal from the transformer secondary is filtered by both the 4-path CSC filter [11] and the proposed 4-path CS∥SC filter. The cascade of CSC and CS∥SC filter is used here as it achieves better out-of-band linearity performance than a stand-alone CS∥SC filter, as shown in Fig. 16. A similar linearity improvement can be achieved by increasing the RF capacitance and the switch size of the CS∥SC filter instead of using a CSC pre-filter at the input. For ease of optimization, the filtering capacitor, C_R, and switches used in both these filters are chosen to be identical. The filtered and voltage-boosted RF signal is down-converted from the bottom plates of C_R in the CS∥SC filter using a differential I/Q mixer with load capacitor, C_B. As discussed earlier, the total parasitic capacitance of all C_R's determines the impedance matching in the proposed receiver. Hence, C_R is chosen to be 1.8 pF for a $S_{11} \leq -15$ dB over the operating frequency range. The baseband capacitors, C_B, are sized to be 10 pF to provide -3-dB RF bandwidth, $f_{-3\,\mathrm{dB,RF}} \approx 15$ MHz, and ≥ 20-dB attenuation for interferers at ≥ 80-MHz offset frequency. Such attenuation filters the out-of-band interferers before they reach BB-LNA and improves the overall linearity of the receiver. Due to the step-up XFMR, the $C_R + C_B$ value of 11.8 pF is far less than 74 pF (see Section II-E) for the desired BW. All capacitors are implemented as alternate-polarity metal–oxide–metal capacitors. Post-layout RC extraction indicates that the parasitic capacitance is about 1.3% of actual capacitance at each terminal of the capacitor.

Small nMOS transistors with $W/L = 7.2 \, \mu$m/20 nm and ON-resistance of 39 Ω are used as switches in both filters and I/Q mixer. The transformer up-converts 50 Ω at the antenna input to 270 Ω at the filter input, thereby resulting in a larger R_S/R_{SW} ratio. This allows the RF front end to achieve an OB-IIP3 of 30 dBm with an R_{SW} that is $\geq 10 \times$ larger than the R_{SW} in [4], [11], and [12], thereby saving LO power. A self-biased transconductor, connected to the center tap of the transformer, sets periodically the dc bias of the switches in the CSC filter via common-mode switches (not shown in the figure) that are $4 \times$ smaller than mixer switches [11], [22].
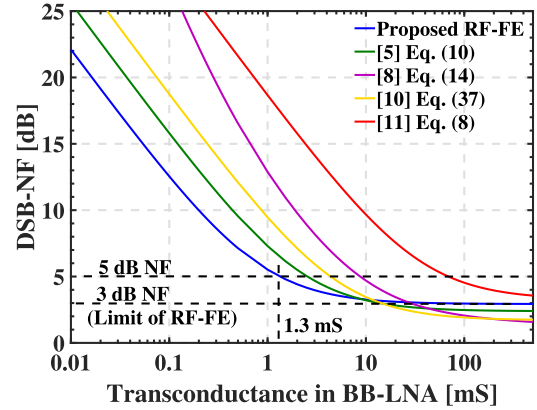
It also sets the dc bias of the RF input, while switches in the mixer are dc-biased by baseband amplifiers.

The switches are driven by four-phase non-overlapping LO signals with a 25% duty cycle. The LO signals are generated using an on-chip divide-by-2 circuit and logic gates from an external clock with twice the LO frequency [22]. The LO signals are capacitively coupled to the gates of switches and are dc-biased with an external voltage of $5 \cdot V_{DD}/8$ via a high-ohmic resistor. Based on post-layout simulations, at 2.4-GHz LO, the all-passive RF front end achieves 17.5-dB voltage conversion gain, 3.5-dB NF, and an OB-IIP3 of ~29 dBm for interferers at 80-MHz offset. The RF front end operates in the frequency range of 1.8–2.8 GHz, with ≤ 3-dB gain variation and a -3-dB RF bandwidth of 15 MHz. Multi-phase LO generation circuitry consumes 1.2–2 mW of power in this operating frequency range.

B. Baseband Amplifier

Since impedance matching is realized via parasitic capacitance of the switched capacitors, the proposed receiver requires a baseband voltage amplifier with high input impedance. Hence, the amplifier is realized as a cascade of low-noise transconductor (LNTA) and TIA. Due to 18-dB passive voltage gain from the RF front end, the LNTA requires g_m of only 1.3 mS to achieve an RX NF of ≤ 5 dB. As illustrated in Fig. 17, the proposed receiver requires $\geq 4 \times$ smaller g_m than that of [10], [11] for a 5-dB NF. On the other hand, the minimum achievable NF of the RX is limited to 3 dB, determined by the lossy RF front end (see Section II-E).

As shown in Fig. 18, LNTA and TIA are implemented using pseudo-differential CMOS inverters with $g_m = 2.4$ and 1.2 mS, respectively for their high g_m/I_D efficiency and good large-signal handling capability [29], [30]. Long-channel transistors (L = 0.4 μm) are employed to achieve low flicker noise and large intrinsic gain. A shunt impedance, Z_F, of 12 kΩ ∥ 4.5 pF is used as TIA feedback. Furthermore, a capacitor, C_S, of 5-pF capacitance is used at the LNTA output to shunt the out-of-band interferers to the ground. Together with shunt feedback, this keeps the voltage swing

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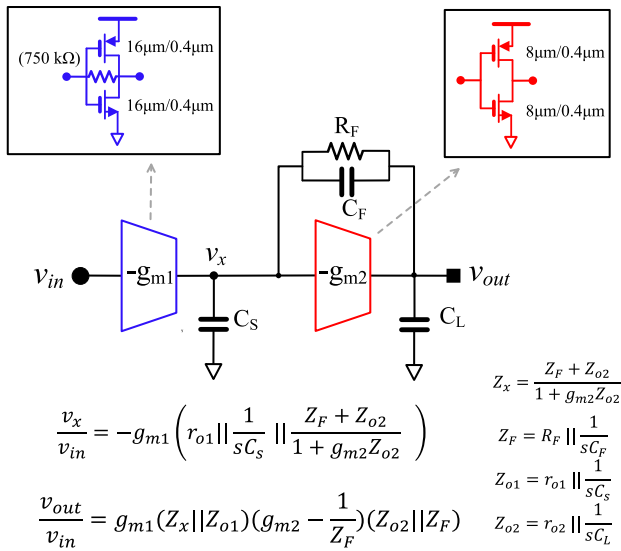

Fig. 18. Schematic and voltage transfer function of the baseband amplifier. (Single-ended version is shown here. RX uses pseudo-differential implementation.).
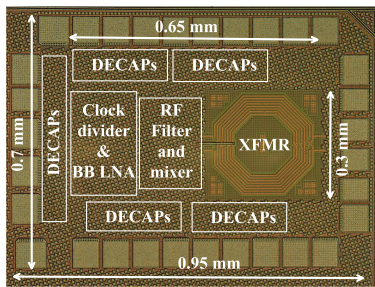

Fig. 19. Die micrograph, indicating major blocks of the front end.

at the TIA input low and, thereby, reduces the drain-voltage related non-linearity at the LNTA output [31]. At its output, the baseband amplifier is loaded by a measurement probe, modeled as C_L in the figure. LNTAs are self-biased using 750-kΩ resistors, while the feedback resistance, R_F, biases the inverter-TIA.

From post-layout simulations, the baseband amplifier achieves a maximum gain of 29 dB and a -3-dB bandwidth, $f_{-3\ \text{dB}} \approx 3$ MHz. It also achieves an input-referred noise voltage of 3.7 nV/$\sqrt{\text{Hz}}$ at 1-MHz frequency. Operating with a supply voltage of 0.8 V, the I/Q baseband amplifiers consume only 0.35 mW of power. The amplifier achieves an OB-IIP3 $\geq$5 dBm for frequency offsets, $\Delta f \geq 20$ MHz. Due to >20 dB filtering from the front end, the achieved BB-LNA linearity is sufficient to meet the design target of $\geq$25-dBm OB-IIP3 for the overall RX front end.

IV. EXPERIMENTAL RESULTS

The proposed mixer-first receiver was fabricated in 22-nm CMOS FDSOI technology and mounted on a 5×5 QFN40 package for experimental verification. Fig. 19 shows the die micrograph, highlighting the major blocks. The total
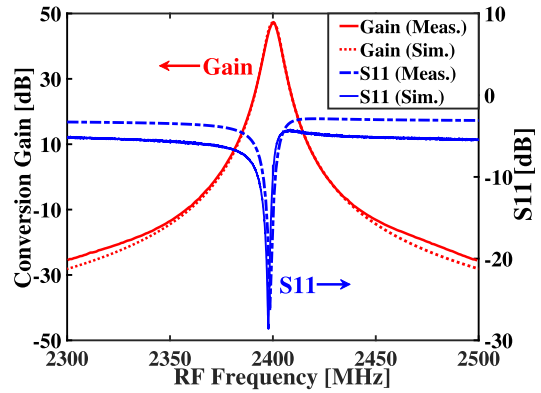

Fig. 20. Measured and simulated conversion gain and S_{11} of the RX for $f_{\text{LO}} = 2.4$ GHz.

area of the receiver, including bond pads and de-coupling capacitors, is 0.67 mm^2, while the active area, including transformer, is only 0.2 mm^2. A supply voltage of 0.8 V is used for both multi-phase LO generation and baseband LNAs. Differential LO signals are provided to the chip using an off-chip hybrid. LO inputs are placed at the opposite side of the RF inputs to reduce coupling between them. An external measurement buffer (Teledyne LeCroy AP033 Active Differential probe) with high input impedance is used at the output of the baseband amplifiers to drive the spectrum analyzer. The cable losses are de-embedded from all the measurement results, except for the results of S_{11}.

A. Gain/S_{11}

Fig. 20 shows the measured voltage gain and S_{11} performance of the receiver as a function of RF frequency for 2.4-GHz LO. The proposed receiver achieves a peak voltage gain of 47 dB and $S_{11} < -20$ dB. Due to tuning capacitors at the transformer input and parasitic capacitance of bond pads, the S_{11} minimum shifts to a frequency lower than 2.4-GHz LO [5], [8], [11]. Furthermore, the RX front end provides $\geq$55-dB attenuation for input at a 40-MHz offset from the LO. This is in good agreement with the simulation results, as shown in the figure. However, the measured S_{11} deviates from the simulation results at higher frequency offsets. This is likely due to parasitic capacitance in the bond wires and PCB traces, which was not modeled in the simulation. Fig. 21 shows the measured conversion gain and S_{11} over an LO frequency range of 1.8–2.8 GHz. Over this LO frequency range, the receiver achieves a peak conversion gain of 45–48 dB and $S_{11} \leq -20$ dB, thereby illustrating its wideband frequency tunability. At high LO frequencies, the gain of the RX front end degrades due to limited transformer bandwidth and loss due to parasitic capacitance of proposed filter/mixer topology, similar to [11], [22].

B. NF and LO Leakage

The measured double-sideband noise figure and the conversion gain of the receiver as a function of baseband frequency for 2.4-GHz LO are shown in Fig. 22. The noise of
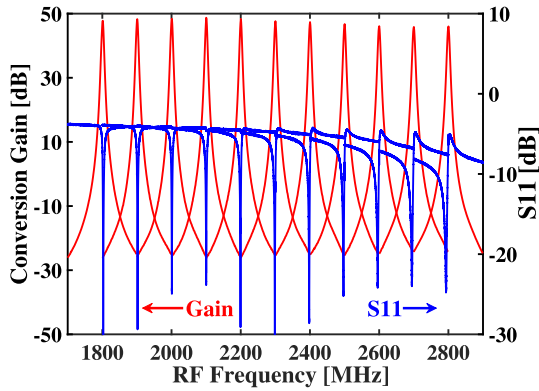
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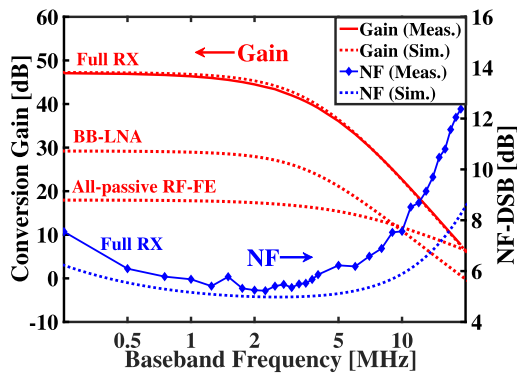Fig. 21. Measured conversion gain and S_{11} performance of the RX versus RF frequency.

Fig. 22. Measured and simulated conversion gain and NF of the RX versus baseband frequency at $f_{LO} = 2.4$ GHz.
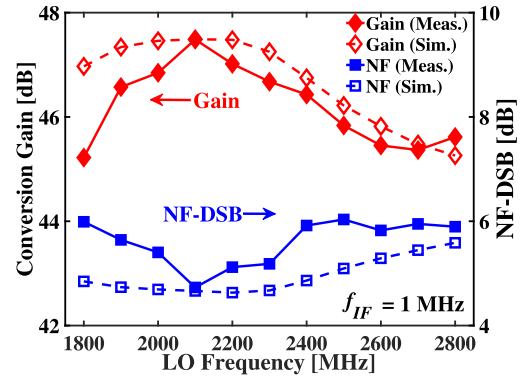

Fig. 23. Measured and simulated RX conversion gain and NF at $f_{IF} = 1$ MHz as a function of LO frequency.

Fig. 24. Measured LO leakage as a function of LO frequency for four different RX samples.

Fig. 25. Measured B1dB, IIP2, and IIP3 as function of interferer frequency offset for $f_{LO} = 2.4$ GHz.

the external LeCroy probe is de-embedded from the results. As seen in the figure, the proposed receiver achieves a noise figure of 5–6 dB, a −3-dB bandwidth, and $f_{-3\,\text{dB,BB}}$ of 2 MHz. Compared to simulation results, a ∼1-dB degradation in the noise figure is observed. This might be due to either parasitic loss at the RF input because of bond wires and PCB traces or additional insertion loss in the transformer. A marginal reduction in bandwidth is also observed due to ∼2-pF extra load capacitance, provided by traces in the PCB, connecting the RX baseband output to the external probe. The measured double-sideband noise figure of the receiver as a function of LO frequency at an IF frequency of 1 MHz is shown in Fig. 23. In the measured LO frequency range of 1.8–2.8 GHz, the noise figure varies between 4.7 and 6 dB, and it is largely determined by the insertion loss and voltage gain of the transformer. This is evident in the figure, as the best noise figure and the maximum conversion gain are achieved at an LO of 2.1 GHz, which is close to the center frequency of transformer bandwidth, defined by the tuning capacitors. In addition, in the operating LO frequency range, the receiver achieves ≤−62-dBm LO leakage, as shown in Fig. 24. The figure reports the measured LO-RF leakage performance for four different receiver samples from the same batch. The leakage degrades with an increase in LO frequency, largely due to layout mismatches and imbalance across the secondary terminals of the transformer.

C. Large-Signal Performance

The large-signal behavior of the receiver is evaluated using two-tone intermodulation tests (IP2/IP3) and a single-tone blocker 1-dB compression point (B1dB) test. In the intermodulation tests, two test tones are applied at $f_1 = f_{LO} - \Delta f$ and $f_2 = f_{LO} - \Delta f + 1$ MHz for IP2 measurements. Similarly, for IP3 measurements, test tones are introduced at $f_1 = f_{LO} - \Delta f$ and $f_2 = f_{LO} - 2\Delta f + 1$ MHz. The measured IIP2 and IIP3 of the receiver as a function of interferer frequency offset, Δf, are shown in Fig. 25. RX achieves −11 dBm IIP3 and 20 dBm IIP2 at a 4-MHz frequency offset, which increases to >10-dBm IIP3 and 60-dBm IIP2 at a 20-MHz offset. The maximum achievable IIP2 and IIP3 of the RX flatten out

Fig. 26. Measured IIP3/IIP2/B1dB as function of LO frequency at $\Delta f = 40$ MHz for four different RX samples.

Fig. 27. Measured blocker noise figure of the RX for $f_{\rm LO} = 2.4$ GHz.

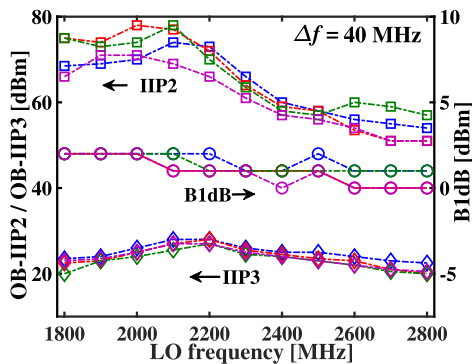at 24 and 60–62 dBm for $\Delta f > 40$ MHz. Poor common-mode rejection ratio and the linearity of the baseband amplifier limit the overall IIP2/IIP3 of the RX at in-band frequencies. For far-off frequencies, the linearity of the proposed CS‖SC filter/mixer limits the overall IIP3 performance and can be improved by reducing the switch resistance at the cost of LO power consumption. The OB-IIP2 performance of the RX depends on the mismatch between switches in the CS‖SC filter/mixer, the LO clock imbalances [23], and layout asymmetries.

Fig. 25 also shows the measured B1dB of the RX as a function of blocker frequency offset, Δf, for $f_{\rm LO} = 2.4$ GHz. For this measurement, a weak desired input signal is introduced at 1-MHz offset from LO, and the minimum blocker signal power is measured for 1-dB degradation in the conversion gain of the desired input. This is repeated for multiple blocker frequency offsets. As seen in the figure, the proposed RX achieves a B1dB of 1 dBm for $\Delta f = 80$ MHz. Please note that Bluetooth 5.2 standard specifies -40 dBm as required IIP3 for the receiver 5-MHz offset and -27 dBm as out-of-band blocker tolerance level for 85–400-MHz frequency offset [32]. Similarly, NB-IoT expects the receiver to operate in the presence of -15-dBm blockers at an 85-MHz frequency offset [22]. As such, the measured 24-dBm IIP3 and 1-dBm B1dB of the implemented RX at 40-MHz offset are much larger than the requirements of these targeted IoT standards.

The measured B1dB, IIP2, and IIP3 performance of the 4 RX samples at an interferer frequency offset of $\Delta f = 40$ MHz are shown in Fig. 26. Due to the limited bandwidth of XFMR, the up-converted R_s, seen by the mixer switches, decreases at low and high LO frequencies. Consequently, the OB-IIP3 also reduces at these frequencies [15]. The imbalance in XFMR and parasitic loss due to layout mismatches deteriorate the OB-IIP2 performance of RX at high frequencies. In the best case scenario, the proposed RX achieves a B1dB of 2 dBm, IIP2 of >75 dBm, and IIP3 of 28 dBm at an LO frequency of 2.2 GHz.

D. Blocker Noise Figure

The blocker signal increases the noise floor at the mixer output via reciprocal mixing and reduces achievable noise figure [26], [30]. Due to its large voltage excursions,
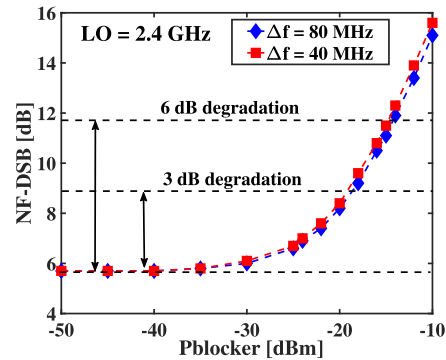
the voltage-shifted RF signal at the input of the second mixer further worsens the blocker noise figure in this receiver. This noise degradation is evaluated by applying blocker signals at a 40-/80-MHz offset from the 2.4-GHz LO and measuring the double-sideband NF at a 1-MHz baseband frequency. The measured NF as a function of blocker power is shown in Fig. 27. The receiver NF degrades by 3 dB for a -20-dBm blocker located at 40 MHz, and the degradation increases to 6 dB for a blocker power of -15 dBm. With >0 dBm B1dB, the NF degradation is largely due to the LO phase noise of the clock generation circuit. From post-layout simulations, the LO phase noise at the clock divider output is -152 dBc/Hz, which is significantly worse than high-performance mixer-first RX [8], [11]. In this receiver implementation, the LO phase noise is traded for low power consumption. On the other hand, the achieved noise figure of 9 dB for a -20-dBm blocker located 40-MHz offset is competitive with the reported performance of other state-of-the-art low-power RXs—a 13.7-dB NF for a -20-dBm blocker at a 50-MHz offset [33] and an 18-dB NF for a -10-dBm blocker at a 400-MHz offset [17]. In addition, the targeted IoT standards, such as Bluetooth and NB-IoT, expect their receivers to tolerate -27-dBm/-30-dBm blocker at 80-/60-MHz offset. As such, the implemented RX can tolerate -20-dBm blockers at 40 MHz with only 3-dB NF degradation, thereby meeting the requirement of these applications.

E. Performance Comparison

The performance of the proposed RX is summarized and compared with other state-of-the-art mixer-first receivers in Table I. The RX achieves ≥ 20-dBm OB-IIP3 for far-off interferers while consuming 1.3–2.1 mW of LO dynamic power in the operating LO frequency range of 1.8–2.8 GHz. For the reported OB-IIP3, the proposed RX consumes at least $5\times$ lower LO dynamic power[1] compared to high-performance mixer-first RXs [5], [6], [9]. This is due to the use of small nMOS switches combined with the step-up XFMR and the almost equal driving capability of nMOS and pMOS in 22-nm FDSOI, used in the on-chip divider and LO buffers. Similarly,

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[1]LO dynamic power does not include the power required to generate the external master clock. This is the usual reporting convention in the literature for passive mixer-first RXs and, thus, applied for all the RXs in Table I.

TABLE I
RESULT SUMMARY AND COMPARISON WITH PASSIVE MIXER-FIRST RECEIVERS

Features	This work	High Performance RX				Low power RX	
		JSSC10 [5]	RFIC15 [6]	JSSC19 [11]	JSSC20 [9]	ISSCC15 [21]	JSSC20 [22]
Technology	22 nm FDSOI	65 nm	65 nm	28 nm	28 nm	65 nm	22 nm FDSOI
Frequency [GHz]	1.8 - 2.8	0.1 - 2.4	0.7 - 3.8	0.1 - 2.0	0.5 - 2.0	0.1 - 1.5	0.6 - 1.3
Power (Analog) [mW]	0.38	30	8.16	30	21.6	11 @ 1.5 GHz[a]	0 [b]
Power (Clock) [mW]	1.3 - 2.1	7.2 - 39.6	19.2 - 67.2	4 - 66	3.9 - 15.6		0.4 - 0.78
Gain [dB]	45 - 47	40 - 70	40	16	32.4	38	9 - 14
BB-BW [MHz]	2	10	3 - 10	6.5	130	2	16
DSB-NF [dB]	4.7 - 6	3 - 5	2.5 - 4.5	4.1 - 10.3	5.5	2.9	5 - 9
OB-IIP3 [dBm] (near interferers)	3 [c] $\Delta f/\text{BW} = 5$	N.A.	0 [d] $\Delta f = 40\,\text{MHz}$	36 [d] $\Delta f/\text{BW} = 5$	21 [d] $\Delta f/\text{BW} = 3$	0 - 1 [d] $\Delta f/\text{BW} = 5$	22 [b,d] $\Delta f/\text{BW} = 5$
OB-IIP3 [dBm] (maximum)	24 [c] $\Delta f/\text{BW} = 20$	25 $\Delta f/\text{BW} = 10$	26 $\Delta f = 100\,\text{MHz}$	44 $\Delta f/\text{BW} = 12.3$	22 $\Delta f = 500\,\text{MHz}$	13 $\Delta f/\text{BW} = 15$	25 $\Delta f/\text{BW} = 10$
OB-IIP2 [dBm]	60 [c] $\Delta f/\text{BW} = 20$	56 $\Delta f/\text{BW} = 10$	65 $\Delta f = 100\,\text{MHz}$	90 $\Delta f/\text{BW} = 12.3$	70 $\Delta f/\text{BW} = 3.8$	47 $\Delta f/\text{BW} = 15$	66 $\Delta f/\text{BW} = 10$
B1dB [dBm]	1 [c] $\Delta f/\text{BW} = 20$	10 $\Delta f/\text{BW} = 10$	3 $\Delta f = 100\,\text{MHz}$	13 $\Delta f/\text{BW} = 12.3$	3 $\Delta f/\text{BW} = 6.15$	-6 $\Delta f/\text{BW} = 15$	1 $\Delta f/\text{BW} = 10$
Blocker NF [dB]	9 -20 dBm / 40 MHz [e]	N.A.	N.A	8.1 0 dBm / 80 MHz [e]	9.7 0 dBm / 960 MHz [e]	13.5 0 dBm / 80 MHz [e]	10.5 -15 dBm / 80 MHz [e]
LO-leakage [dBm]	<-62 [f]	<-65	<-60	N.A.	N.A	N.A	<-70 [f]
Supply [V]	0.8	1.2/2.5	1.2	1.2/1.0	1.8/1.2	0.7/1.2	0.8
Active-Area [mm^2]	0.20	0.75	0.23	0.49	0.16	0.028	0.23
External components	None	None	Bal-un	180° Hybrid Coupler [g]	1:1 Bal-un	None	1:2 XFMR

N.A. Not Available   [a] No separate power consumption for analog and clock circuitry   [b] No integrated baseband frequency   [d] extrapolated from the figure   [e] Blocker power and offset frequency   [f] Measured for 4 different samples   [g] Coupler provides 100 Ω at differential RF input   [c] For 2.4 GHz LO

the BB-LNA in the proposed RX consumes at least 10× less power (only 0.35 mW for four BB-LNAs) to achieve <6-dB NF. This is because of the 18-dB passive voltage gain provided by the proposed voltage-boosting mixer and XFMR. On the other hand, the passive voltage gain limits the achievable blocker tolerance to moderate numbers. The first-order impedance roll-off at the baseband outputs of the mixer and the voltage-mode BB-LNA limit the achievable linearity of the proposed RX front end in the presence of nearby blockers in the transition band. In comparison to our previous work, as presented in [22], this RX front end, with on-chip XFMR and baseband amplifier, achieves higher passive gain via implicit capacitive stacking, comparable OB linearity, and better noise figure while operating at $2-3\times$ higher LO frequency. Finally, among low-power (≤ 10 mW) mixer-first RX topologies, the proposed front end achieves the highest reported far-off OB-IIP3 while maintaining ≤6-dB noise figure, as shown in Fig. 2.

V. CONCLUSION

This article proposes a low-power widely frequency-tunable passive mixer-first receiver topology, achieving high linearity without compromising its noise figure. The proposed receiver employs a new N-path filter/mixer that achieves 3× voltage

gain by implicit capacitive stacking technique and uses at least 2× smaller capacitance to achieve the same filtering at the RF input. Encompassing an on-chip 2:6 transformer and a highly-linear baseband LNA, the proposed 22-nm-FDSOI receiver achieves ≥24-dBm OB-IIP3, ≤6-dB NF, and ≥1-dBm OB-B1dB while consuming only 2.2 mW of power at 2.4-GHz LO. As such, it provides an integrated solution for large interferer tolerance in low-power IoT radio front ends.

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