# A Predistortion-less Digital Transmitter with –50 dB ACLR Exploiting Output Conductance Linearization

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***Abstract*—Switched capacitor power amplifiers (SCPAs) are a class of digital transmitters which have shown promising results for high linearity with good drain efficiency (DE). Their linearity is limited by AM-PM distortion, caused by a difference in output conductance in switching and non-switching driver cells. Often, digital predistortion (DPD) is required to transmit higher order modulation schemes. In this letter, a driver cell implementation as an inverter with drain resistors is proposed which has equal output conductance in both cases, aiming to eliminate AM-PM distortion. An SCPA with these driver cells is implemented in a 22nm fully depleted silicon-on-insulator (FD-SOI) CMOS process which demonstrates excellent DPD-less linearity with an adjacent channel leakage ratio (ACLR) of –50 dB and an error vector magnitude (EVM) of –45.5 dB for 5 MHz 1024 QAM signals at a DE of 8.8%. A matching network exploiting bondwires as high-Q inductors removes on-chip inductors and significantly reduces chip area.**

***Index Terms*—CMOS integrated circuits, power amplifiers, linearity, nonlinear distortion, switched capacitor power amplifiers (SCPA), digital transmitters**

## I. Introduction

In order to support ever rising data rates in an increasingly dense spectrum, higher order modulation schemes such as 1024 QAM or OFDM are applied to increase spectral efficiency. These schemes have stringent linearity specifications on both error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR), to ensure enough signal to distortion to demodulate these large constellations, and to keep the interference in the next band within acceptable levels.

In many transmitters, the intrinsic linearity of the power amplifier (PA) is not sufficient to meet the ACLR and EVM requirements for 1024 QAM, and digital predistortion (DPD) is added to compensate. DPD does however have its drawbacks. Firstly, to construct the inverse non-linear function of the PA, an accurate characterization of the PA is required [1]. This characterization is even more complex in systems with significant memory effects [2]. Furthermore, not all nonlinearity can be canceled, e.g. because of bandwidth extension between the polar and Carthesian domain in polar transmitters, or due to the unpractical required nonlinear order [1]. Lastly, the required DPD can significantly increase system power consumption, especially in scenarios with high bandwidth, high DPD complexity, and low PA output power [3]–[5]. All these problems are avoided with a PA with sufficient intrinsic linearity for 1024 QAM to omit DPD.

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Radio frequency digital-to-analog converters (RF-DACs) have shown good intrinsic linearity [4]–[12]. This has been further enhanced with e.g. non-uniform element scaling [4], phase feedback [6], clock overlap and non-switching NMOS/PMOS linearization [5], [7], series linearization resistors [8] and wideband power supplies [9].

Switched capacitor power amplifiers (SCPAs) are digital transmitters with good drain efficiency (DE) and high linearity due to accurately matched capacitor ratios [5], [7], [10]–[12]. Their behavior is modelled in Figure 1 as an array of $N$ switched voltages and a capacitive divider with total capacitance of $C_s$. This capacitance, inductance $L_s$ and the load antenna form a bandpass filter around the carrier frequency. The switch series resistance is modeled as $R_{cell}$. When implementing the switches as inverters, $R_{cell}$ is the inverter output resistance. Mismatch between $R_{cell}$ of switching and non-switching cells will result in AM-AM and AM-PM distortion [5], [7], [10], [11]. In this letter, a driver with equal $R_{cell}$ for switching and non-switching cells is proposed, aiming to eliminate this form of distortion for high DPD-less linearity.

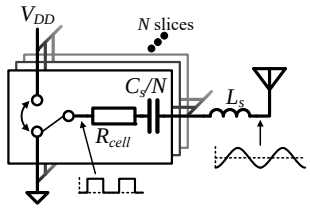



Fig. 1. Model of a SCPA with cell output resistance $R_{cell}$.

Section II analyzes the AM-PM distortion in SCPAs due to this $R_{cell}$ variation. Section III introduces a circuit with equal output conductance for switching and non-switching cells, to remove AM-PM distortion. A matching network using bondwires as inductors is proposed in Section IV. In Section V, an implementation in 22nm fully depleted silicon-on-insulator (FD-SOI) is presented. Section VI provides measured performance of the system. Section VII concludes the work.

## II. SCPA Linearity

### A. CMOS Inverter Output Conductance

The SCPA model in Figure 1 does not contain nonlinear elements and therefore is perfectly linear. When implementing the switch as a CMOS inverter, the output resistance of a non-switching cell $R_{nsw}$ is determined by the transistor on-resistance $R_{on}$. For switching cells, even when assuming NMOS and PMOS with equal on-resistance, the output conductance will not be constant over input voltage. For typical

supply voltages, both transistors are in the saturation region halfway a logic transition, and have a high output resistance. The effective output resistance of a switching cell $R_{sw}$ is thus higher than that of a non-switching cell [5], [7], [10], [11]. This means that $R_{cell}$ is nonlinear and can be either $R_{sw}$ or $R_{nsw}$, dependent on whether an inverter is switching.

### B. AM-PM Distortion in SCPAs

The unequal $R_{sw}$ and $R_{nsw}$ result in a code-dependent output impedance and consequently in nonlinearity, typically dominatated by AM-PM distortion [5], [7], [10], [11]. For a polar SCPA, the AM-PM distortion is given by [11]:

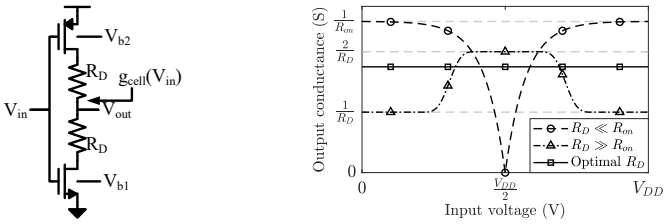
$$\text{AM-PM}\,(k) \approx \omega N R_{nsw} C_s \left(\frac{R_{sw}}{R_{nsw}} - 1\right)(k-1) \quad [\text{rads}] \tag{1}$$

Where $k$ is the normalized amplitude for a polar transmitter, $\omega$ is the angular frequency, and $C_s$ is the array capacitance. In quadrature SCPAs, the same mechanism results in 2-D distortion of the transmitted constellation. From Equation 1, it can be observed that when $R_{sw} = R_{nsw}$, the phase response is constant over amplitude, and a linear transfer is achieved. Apart from Equation 1, supply related distortion can also be present, especially at high output power [9].

In prior art, SCPA linearization techniques have been proposed to approach this equality. In [7], clock overlap is applied, such that during a part of the transition, both transistors are conducting . This increases output conductance during a transition, and improves linearity. In [5], additional decrease of the output conductance of non-switching cells in a polar SCPA is simulated to further improve upon this technique. In this work, a driver cell is proposed that aims at a constant output conductance to achieve $R_{sw} = R_{nsw}$.

## III. Constant Output Conductance Cells

Figure 2a shows the proposed constant output conductance driver cells, as an inverter with added drain resistors $R_D$. In the extreme scenario when $R_D \ll R_{on}$, the drain resistors can be neglected, resulting the same output conductance as a standard CMOS inverter. This is indicated in Figure 2b: the output conductance in the 'high' or 'low' logic states equals the on-conductance of the transistors, and a minimum in conductance can be found around $V_{in} = V_{DD}/2$. When $R_D \gg R_{on}$, the transistors can be regarded as almost ideal switches which are open or closed, dependent on $V_{in}$. The resulting output conductance is indicated in Figure 2b as well. In the 'high' or 'low' logic input states this equals the drain resistor conductance, and halfway during the transition the output conductance is the parallel of the two drain resistors, which is twice that of the clipped states. Contrary to the CMOS inverter, $g_{cell}$ now shows a peak around $V_{in} = V_{DD}/2$. By tuning the drain resistors, a value can be found where the conductance in the extreme states equals that of the average during the transition, indicated by the middle line in Figure 2b. Even when this line is not completely flat, a value for $R_D$ can be found which results in $R_{sw} = R_{nsw}$. This eliminates the AM-PM nonlinearity in Equation 1.




(a) (b)

Fig. 2. Proposed constant output conductance driver cell. (a) Circuit. (b) Output conductance.

Output power and DE loss due to the added resistance is kept low by scaling the driver width to achieve a low transmitter output impedance relative to the load.

## IV. Inductorless Matching and Impedance Transformation

Chip area for SCPAs is often largely determined by integrated inductors or transformers in the output matching network [7], [10]. These integrated components have the additional drawback of a low quality factor in the low-GHz range, decreasing output power and DE.

The matching network in Figure 3 has been used for matching and impedance transformation. The SCPA has been modeled as a Thevenin equivalent differential voltage $v_{rf+}/v_{rf-}$ with series capacitance $C_s$ [10]. The matching and impedance transformation network is based on the well known fourth order Type I Chebyshev bandpass filter, with transformation of the inductive tee to the mirror-image tee to achieve impedance transformation [1]. The inductors have been implemented as parallel bondwires to a QFN leadframe with a length of 1500µm. Mutual coupling has been taken into account during design. No integrated inductors have been used, saving considerable chip area. The design does however require external components. The 17.5µm diameter gold bondwires allow for a higher quality factor than what would have been possible in the much thinner metal layers in the chip metal stack, reducing loss in the matching network. The transformation ratio of this network is determined by the ratio of the inductors $L_s$ and $L_p$. Deviation from optimal values in production will thus not lead to a change in impedance transformation, as long as the inductors deviate in the same way, e.g. due to increased length. This correlated deviation does shift the center frequency of the pass-band, but considering fourth order Type I Chebyshev filters can have bandwidths exceeding an octave, the carrier frequency can still be inside the filter pass-band.

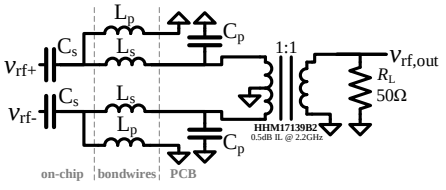



Fig. 3. Chebyshev matching network with bondwires as inductors.

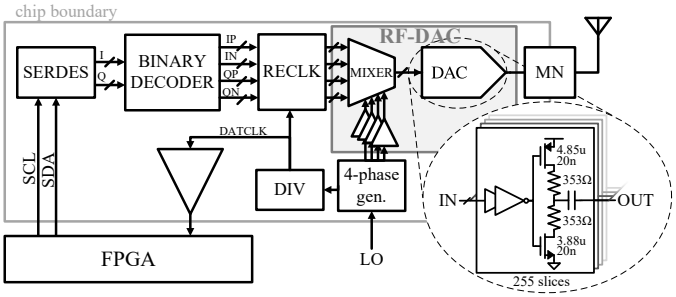



Fig. 4. Overview of the transmitter implementation. Single-ended equivalent is shown, actual implementation is differential.

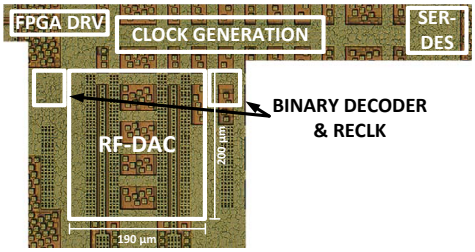



Fig. 5. Die photograph of the SCPA. Total active area for theRF-DAC, decoder and reclocking is 0.042 mm$^2$

The differential implementation has the benefit that the return path for the output current is not via ground or the supply, which could introduce an output-dependent supply ripple or ground bounce, resulting in non-linear effects. It does however mean that an off-chip power combiner is required for a single-ended output. This design uses an external balun. For narrowband applications, this could replaced by a combiner in PCB structures to further reduce the bill of materials, or an inherently differential dipole antenna could be used.

## V. Circuit Implementation

A quadrature 8-bit SCPA transmitter is designed as indicated in Figure 4, with 5 unary bits and 3 binary bits. Driver $W/L$ and $R_D$ are dimensioned for an output conductance of 2.4mS per cell, giving a transmitter output impedance of 1.6Ω for both pseudo-differential 8-bit RF-DACs. An FPGA is used to generate digital baseband data, synchronized to the divided LO. Though the quadrature SCPA is less power efficient than its polar counterpart [12], it does not suffer from non-linearity introduced by finite bandwidth of the control signals, or delay between the phase and amplitude control paths [13].

The design is implemented in 22nm FD-SOI CMOS technology and is supplied with 0.9 V. A die photograph is shown in Figure 5. The combined area for the RF-DAC, decoders and reclocking is $0.042$ mm$^2$. The auxiliary circuits for clock generation and interfacing to the FPGA occupy an additional $0.023$ mm$^2$. The FD-SOI technology enables for controllable forward back-biasing of the transistor back gate voltages [14]. This allows for fine-tuning of the $g_{drv}(V_{in})$ characteristic by adjusting back-bias voltages $V_{b1}$ and $V_{b2}$ in Figure 2a to compensate for process corners.

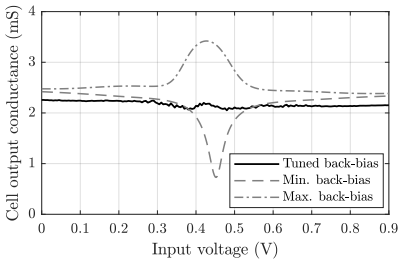
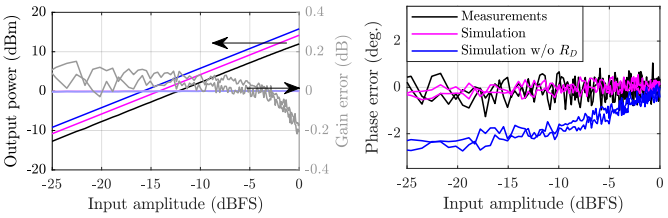



Fig. 6. Measured $g_{cell}(V_{in})$ with calibrated back-bias and simulated calibration range. Offset indicates the measured device is in the slower corner.

## VI. Experimental Results

The output conductance $g_{drv}(V_{in})$ of a single driver cell has been characterized using DC measurements. A small current was forced into the cell output node, and the output conductance has been calculated from the resulting voltage change. The back-bias has been tuned for maximum linearity. Figure 6 demonstrates the output conductance is constant within 6% of the mean conductance over the full input range.

The AM-AM and AM-PM distortion have been measured without the use of DPD, and are plotted in Figure 7a and Figure 7b, respectively. Simulated results with and without added drain resistors are shown for comparison. Drain resistors improve AM-PM distortion from a maximum deviation of 2.7° to $\ll 1°$. Due to the increased output resistance, the drain resistors decrease output power by 1.6dB in simulation.




(a) (b)

Fig. 7. Measured AM-AM and AM-PM response with equal I and Q codes. Amplitude is referred to full-scale. Double lines to display both positive and negative codes. (a) AM-AM and (b) AM-PM distortion.

1024 QAM signals with a carrier frequency of 2.2 GHz carrier and 6.9 dB PAPR are transmitted without DPD. The spectrum in Figure 8a indicates an ACLR of –50.1/–50.3 dB at 5MHz bandwidth. Digital IQ-imbalance compensation is applied to correct for a static 0.45° quadrature phase error, –0.30 dB quadrature gain error and –28 dB LO leakage with respect to peak power. The received 5MHz constellation in Figure 8b indicates an EVM$_{\text{rms}}$ of –45.5 dB.

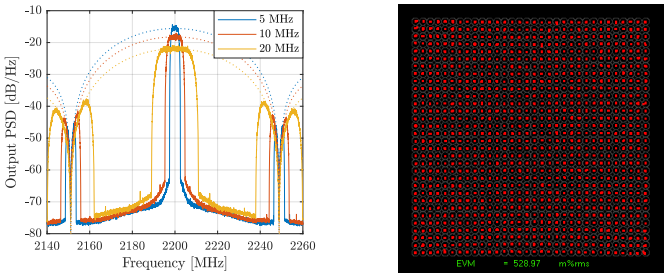
The DE and output voltage of the RF-DAC are shown in Figure 9a and Figure 9b, respectively. For the 5MHz signals in Figure 8, the RF-DAC has an average DE of 8.8%. Simulations use a matching network model as in Figure 3. In the actual setup, packaging and PCB effects impair impedance transformation and add additional losses, reducing output power and consequently drain efficiency.

Table I shows the comparison to state-of-the-art highly linear digital transmitter designs, indicating excellent DE for a transmitter capable of DPD-less 1024 QAM.

TABLE I
PERFORMANCE OVERVIEW AND COMPARISON TO STATE-OF-THE-ART

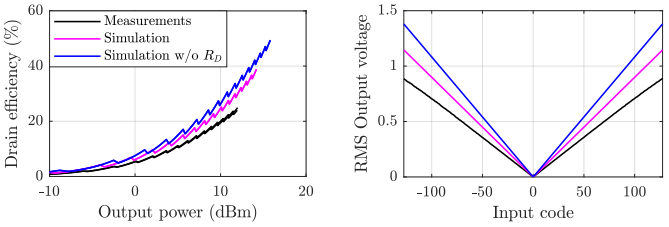
| Reference | [4] | [6] | [7] | [8] | [9] | **This work** |
|---|---|---|---|---|---|---|
| Architecture | Segmented class-E | Digital class-D$^{-1}$ | SCPA | Capacitive DAC | SCPA | SCPA |
| Frequency [GHz] | 2.2 | 5.5 | 2.2 | 1.9[a] | 1.95 | 2.2 |
| $P_{peak}$ [dBm] | 14.6 | 11 | 13.0[c] | 5.6 | - | 12.0 |
| $\eta_{DE,peak}$ | 43.8 | 20.3 | - | 0.69 | - | 24.9 |
| Modulation | 64 QAM | 1024 QAM | 802.11ax 1024 QAM | 1024 QAM OFDM | 4G LTE20 | 1024 QAM |
| $P_{avg}$ [dBm] | 7.8 | –2.7[a] | –3[c] | - | 6 | 5.1 |
| $\eta_{avg}$ [%] | 12.6 | 1.2[a] | 1.0[c] | - | - | 8.8 |
| Bandwidth [MHz] | 20 | 2.5 | 40 | 20[a] | 20 | 5 / 10 / 20 |
| ACLR [dB] | –41/–40 | –36[a] | –47/–47[b] | –72[a] | –45.7 | –50.3 / –49.1 / –47.6 |
| EVM [dB] | –35 | –41.3[a] | –42.2 | –49[a] | –31.7 | –45.5 / –43.4 / –35.3[e] |
| DPD | No | Yes | No | Mismatch correction | No | No |
| Technology | 40nm CMOS | 28nm CMOS | 65nm CMOS | 16nm FinFET | 28nm CMOS | 22nm FD-SOI |
| Supply voltage [V] | 0.5 | 0.9 | 1.2 | 1.2 | 1.3/1.1 | 0.9 |
| Matching network | on-chip | on-chip | on-chip | on-chip | on-chip | bondwires + external |
| Active area [mm$^2$] | 0.45 | 0.29[b] | 0.26 | 0.26 | 1.3[d] | 0.042 |

[a] Values for maximum reported linearity. [b] Estimated from figure. [c] Please note the large back-off. [d] Includes three RF-DACs and biasing. [e] As EVM degrades much faster than ACLR, it is expected that EVM at 20 MHz is limited by intersymbol interference rather than non-linearity.




(a) (b)

Fig. 8. 1024QAM measurement results. (a) Spectrum for 5/10/20 MHz 1024 QAM with dotted sinc function. Alias amplitudes can be reduced by e.g. increasing the baseband sample rate (48.89MHz in this demonstrator) (b) Constellation with 0.53% EVM RMS for 5 MHz 1024 QAM




(a) (b)

Fig. 9. (a) Drain efficiency. (b) RMS output voltage over code for equal I/Q. The drain resistors reduce the simulated maximum output power by 1.6 dB and consequently reduce the simulated drain efficiency from 49.4% to 38.8%.

## VII. Conclusion

A constant output conductance cell is proposed to mitigate AM-PM distortion in SCPAs for high DPD-less linearity. By using inverters with added drain series resistors as driver cells, the output conductance can be designed such that switching and non-switching cells have equal output conductance, eliminating this source of non-linearity. FD-SOI backgate bias allows for tuning of the output conductance over process corners. An implementation in 22nm FD-SOI technology demonstrates an AM-PM distortion $\ll 1°$, allowing for DPD-less transmission of 1024QAM signals, with EVM of –45.5 dB and ACLR of –50/–50 dB. The DE of 8.8% is excellent for transmitters capable of transmitting DPD-less 1024 QAM. A matching network using an external balun and bondwires as inductors reduces the active area of the design to 0.042mm$^2$.

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