Low-Frequency Envelope of DC/DC Converters due Differences in the Control Hardware Features

Waseem El Sayed[1,2,3], Hermes Loschi[1,2,3], Amr Madi[1,2] , Niek Moonen[2], Robert Smolenski[1], and Frank Leferink[2]
[1]Institute of Automatic Control, Electronics and Electrical Engineering, University of Zielona Gora, Poland
[2]Electrical Engineering, Mathematics & Computer Science (EEMCS), University of Twente, Enschede, The Netherlands
[3]George Green Institute for Electromagnetics Research, University of Nottingham, Nottingham NG7 2RD, United Kingdom
amr.madi@ieee.org,w.wafiksaadelsayed@utwente.nl, eng.hermes.loschi@ieee.org, niek.moonen@utwente.nl, r.smolenski@iee.uz.zgora.pl, and frank.leferink@utwente.nl.

***Abstract*- In conjunction with concerns about electromagnetic compatibility (EMC), the low-frequency envelope provided by the frequency beat produced from the aggregation of harmonics generated by multiple power electronic converters. The low-frequency envelope becomes worrisome as the variations in the amplitude of electromagnetic interference (EMI) in the time domain, can influence the performance of the EMI detectors, e.g., average detector (AV). Therefore, this paper addresses the low-frequency envelope provided by the frequency beat, using two DC/DC converters controlled by two different controllers: PXI-7854R and Atmega328P. The practical setup and EMI measurements are discussed in the EMC framework.**

***Keywords* — Electromagnetic interference, Electromagnetic compatibility, Low-frequency envelope, and DC/DC Converters.**

I. Introduction

Smart grid is an unprecedented opportunity to create a reliable and efficient electrical system, which provides efficient electricity transmission, energy management, reduced peak demand, allows the integration of renewable energy utilization, due to the micro and nano grids [1]. The previous advantages will help utilities conserve energy, increase reliability and make processes more efficient. Also offering benefits, including enhancing cybersecurity and protection to the consequences of weather disasters due to isolation operation [2].

Nevertheless, due to the exponential increase in power electronics systems and infrastructure, micro and nano grids confront many challenges to assure electromagnetic compatibility (EMC), particularly on renewable energy systems [3], [4]. To avoid the improper operation or failure of power electronic converters, EMC standards and regulations were deducted to govern the equipment electromagnetic interference (EMI) emissions level, especially for conducted EMI scenarios [5].

Thus, nowadays, the conducted EMI measurement procedure is vital to establish conformity and assure the EMC of power electronics systems and infrastructure. However, one of the main drawbacks of micro and nano grids, from the EMI measurement point of view, can be attributed to the electrical installation's topologies. In particular, a peculiar phenomenon has been gaining notoriety and being the subject of recent research, i.e., the low-frequency envelope provided by the frequency beat.

Although, the low-frequency components are believed to be filtered by the converters' output low pass filter [6]. In [7] is showing that for voltage mode-controlled converters, there will be a low-frequency EMI component. Also, [4] and [8] indicate the low-frequency envelopes, resulting from frequency beating accompanying aggregation of harmonic components of similar frequencies.

Hence a non-convergence between the operation of power electronic converters, into parallel electrical installations topologies, and the EMC requirements begin to be evident. Mainly because many of the reported phenomena by [4], [6]-[8], may come from changes in time-domain, such as time displacement between control signals, and the difference in power conversion equipment clock signals, once each crystal oscillator provides one specific frequency stability.

Therefore, in this paper, it is shown that the 2D conventional EMC test standard based on frequency scanning might not be sufficient to appropriately provided an EMI assessment. The EMI measurements were carried out with two DC/DC converters into the concept of parallel electrical installations topologies. Besides, to investigate the possible associated phenomena further, the EMI measurements were carried out in the outputs voltage and current. Once these waveforms have different time-domain shapes (rectangular and triangular waves), different behavior in the spectrum of frequency might be expected.

This paper is divided as follows: Section II introduces the basic theoretical background for the frequency beat phenomena. Section III introduces a simulation to show the phenomena. The hardware implementation is presented in Section IV. Results are shown and discussed in Section V. Finally, Section VI shows the conclusions.

II. Theoretical Background

The frequency beat phenomena appear when two or several converters are connected in the same circuit but with a slight difference between the utilized switching frequency of each converter. This difference in switching frequency could appear due to the instability of the onboard clock of the used controller during the operation.

Hence, considering two converters operating together in the same circuit, the output envelope of the aggregated signal could be represented as

$$Env_{f_1 f_2} = \left| 2\cos\left(2\pi \frac{f_1 - f_2}{2} t\right) \right| \quad (1)$$

where f_1 and f_2 are the switching frequencies of converters one and two respectively. In order to study the phenomena in the case of buck converters, let's assume that we have to square signal have the same duty cycle of 50 %, in the case two rectangular pulse trains $\left(X_{(T)}\right)$ are adding.

This paper is part of a project that has received funding from the European Union's Horizon 2020 research and innovation program under the Marie Sklodowska-Curie grant agreement No 812391 – SCENT.

978-1-7281-7621-5/21/$31.00 ©2021 IEEE

Also, based on the trigonometric form of the Fourier series, and in the concept of adding two sinusoidal oscillations $\left(X_{(T)_{sum}}\right)$ expressed as

$$X_{(T)_{sum}} = 2A_{sum}\cos(\bar{\omega}t)\cos\left(\left(\frac{\Delta\omega}{2}\right)t\right) \quad (2)$$

where $\bar{\omega}$ and $\Delta\omega$ are the mean and differential values of the two (angular) frequencies, and the term $2A_{sum}$ represents the adding of the amplitudes of two equal sinusoidal oscillations. Considering Eq.2 represents the sum of for N harmonic orders, $X_{(T)_{sum}}$ could be represented as:

$$X_{(T)_{sum}} = \sum_{n=1}^{N} 2A_{n_{sum}}\cos(n\bar{\omega}t)\cos\left(n\left(\frac{\Delta\omega}{2}\right)t\right) \quad (3)$$

where

$$A_{n_{sum}} = \frac{2}{T}\int_{-T/2}^{T/2} A\cos(2\pi n\,(f+\Delta f)t)\,dt$$

III. The Frequency Beat Simulation

The simulation was implemented in MATLAB, considering two square waves with a 50% duty cycle, the frequency of the first signal is 20 Hz and the second is 19 Hz. Both signals are added to each other following Eq.1. Fig. 1 shows the performance of the two $X_{(T)}$. Also, both $X_{(T)}$ presented in Fig.1A and Fig.1B, consider the interval of integration centered around the origin, i.e., 0.

The difference between both $X_{(T)}$ presented in Fig. 1A and Fig.1B is related to the values of frequency. Fig.1A considers $f_1 = 20$ Hz and Fig.1B considers $f_2 = 19$ Hz. Thus, Eq. 1 provides the beat at $\left|-\frac{1}{(f_1-f_2)} < t < \frac{1}{(f_1-f_2)}\right|$, as is possible to observe in Fig.1C for a $t = 2$ s.

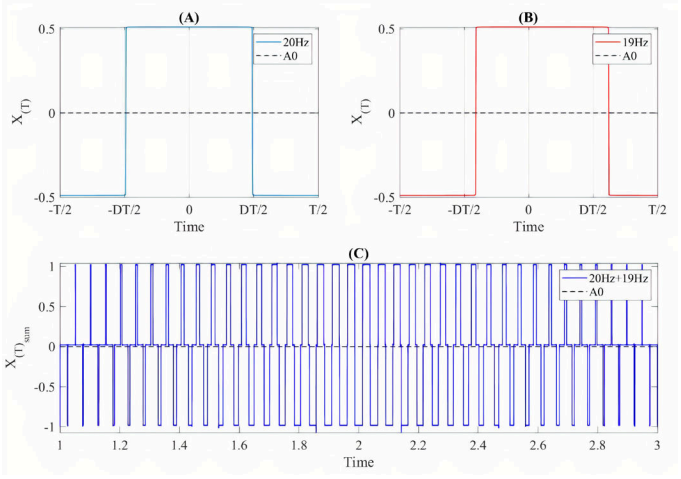

Fig. 1. The adding of two $X_{(T)}$, with both values of D=50%: (A) $f_0 = 20$ Hz, (B) $f_0 = 19$ Hz and (C) $X_{(T)_{sum}}$.

IV. Experimental Setup Description

The testbed was built utilizing two Buck converters controlled by two separate controllers. The main parameters of the used converters are presented in Table I. Also, both Buck converters are connected to the same load as shown in Fig.2.

Hence, the setup provides controlling the switching signal based on pulse width modulation (PWM) [9], [10].

Two types of commercial controllers were used. The Field Programmable Gate Arrays - FPGA-7854R from National Instrument (NI) and Atmega328p from Atmel used in Arduino UNO board.

TABLE I. Converter Parameters

Item	Value
Transistors type	IGBT – IXGH40N60C2D1
Input Voltage	40 V
Input current	0.5 A
Output Voltage	20 V
Output current	1 A
Switching frequency	60 kHz
Duty cycle	50%

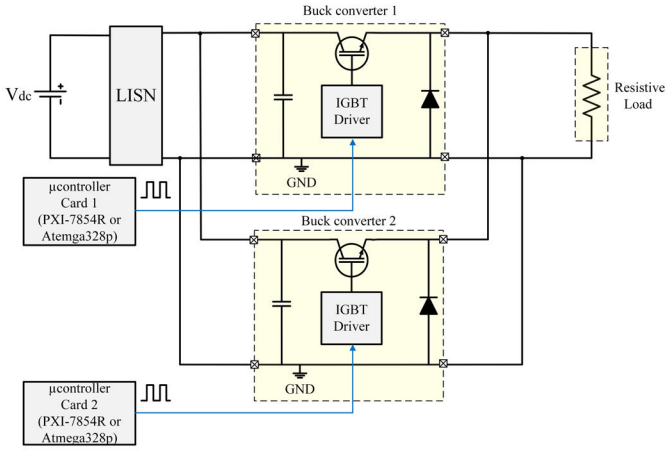

Fig. 2. Experimental setup connection diagram

The FPGA-7854R controllers use a crystal of 40 MHz with a maximum variation of ± 100 ppm, while the Atmega328p controllers use one of 16 MHz with a maximum variation of ± 50 ppm. The frequency stability variation in the case of FPGA-7854R might be between 54 to 66 kHz with 60 ± 6 kHz variation around the main switching frequency, while in the case of Atmega328p, might be between 57 to 63 kHz with 60 ± 3 kHz variation around the main switching frequency.

V. Results Discussions

The average detector (AV) with the intermediate frequency bandwidth (IFBW) = 200 Hz was used in all results following CISPR A standard. The beat appears faster in the case of using two Atmega328p controllers than in the case of using two FPGA-7854R. The beat variation of amplitude appears in the case of Atmega328p every 0.6 seconds as shown in Fig.3. Thus, the frequency stability variation is in the range of 60000 ± 1.6 Hz. In the case of FPGA-7854R, The beat variation of amplitude is repeated every 150 seconds as shown in Fig.4. Thus, the frequency stability variation is 60000 ± 0.0066Hz.

The frequency spectrum amplitude of the output voltage presents different behavior from the case of output current. In the case of the voltage, the measured signal is a rectangular pulse train. The spectrum amplitude of the harmonics decreases with the increase of the harmonic order. The highest amplitude of EMI appears in the harmonics related to the fundamental switching frequency used to control the DC/DC converters, i.e., 115 dBµV. The amplitude of the 2nd and 3rd harmonics are 108 dBµV and 105 dBµV, respectively, as shown in Fig.3 and Fig.4. It's noteworthy that the amplitude of the even and odd harmonics decreased gradually by a definite pattern.

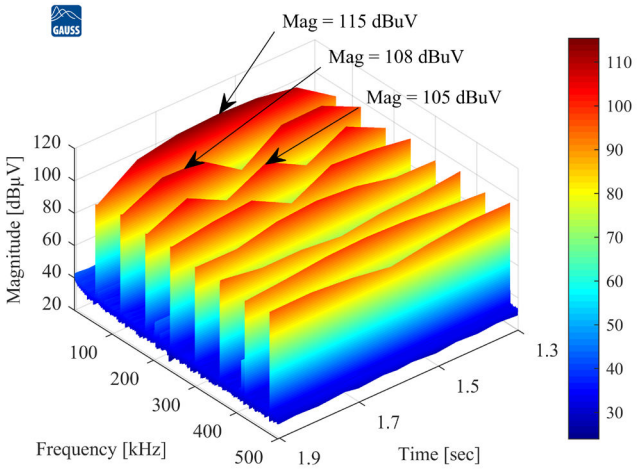

Fig. 3. 3D Spectrogram of the output voltage in case of using two Atmega328p controllers.

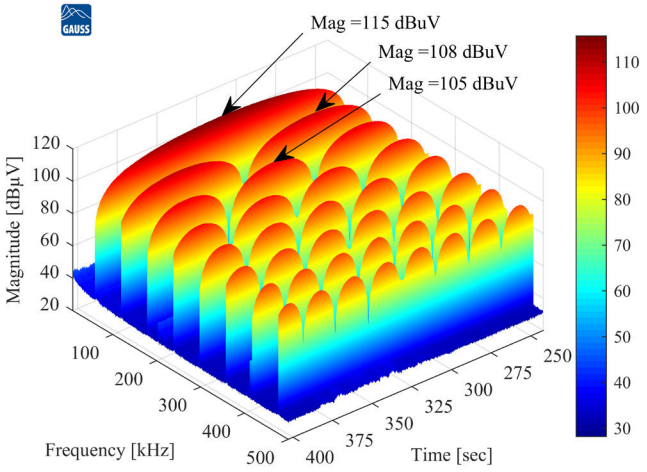

Fig. 4. 3D Spectrogram of the output voltage in case of using two FPGA-7854R controllers.

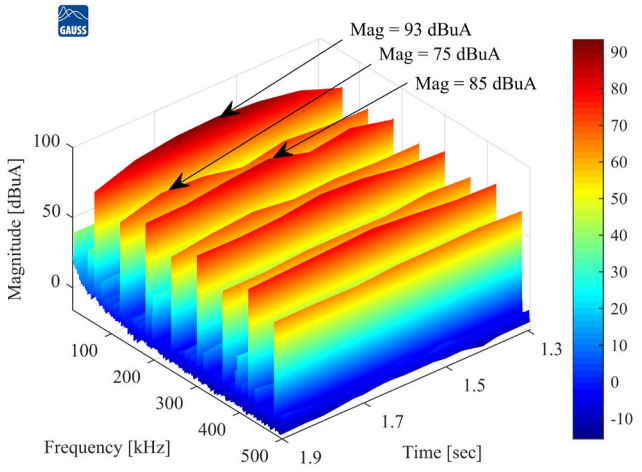

Fig. 5. 3D Spectrogram of the output in case of using two Atmega328p controllers.

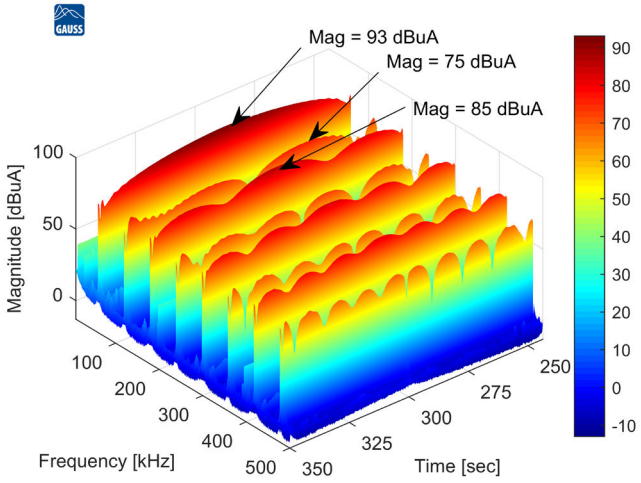

Fig. 6. 3D Spectrogram of the output current in case of using two FPGA-7854R controllers.

On the other hand, in the case of output current, the even harmonics spectrum amplitude is lower than that in odd harmonics. Fig. 5 and Fig. 6 show the amplitude of the 3rd harmonic higher than the 2nd harmonic by 10 dB.

Once these waveforms have different time-domain shapes (rectangular and triangular), different behavior in the spectrum of frequency was presented in Fig. 3 to Fig. 6. Moreover, the frequency stability variation related to the power conversion equipment clock signals, i.e., control hardware, was within the expected range. However, better performance was the FPGA-7854R frequency stability, verified through the EMI measurements carried.

VI. Conclusion

This paper focuses on the comprehension of phenomena associated with power electronic converters into parallel electrical installations topologies. The emphasis on the low-frequency envelope provided by the frequency beat was the core motivation of this paper, especially to assess the output voltage and output current through EMI measurements. Once these waveforms have different time-domain shapes (rectangular and triangular wave), the results of Fig.3 to Fig. 6 showed different behaviors in the frequency spectrum. Highlighting how this peculiar phenomenon, originating from the time domain, can influence the performance of the 2D conventional EMC test standard based on frequency scanning.

Once the frequency stability variation behavior depends on the variation of the controller's onboard crystal frequency, which may be affected by other parameters such as the temperature, circuit impedance, and ground, or the quality of the manufactured crystal. The control signal from FPGA-7854R, at the hardware level, is provided by the NI SCB-68A shielded connector block. Combined with the shielded cables, it provides rugged, very low-noise signal termination to the transistor gate drive. Thus, as verified through the EMI measurements carried, providing better performance in terms of frequency variation stability, i.e., 60000 ± 0.0066Hz.

Acknowledgment

The authors would like to thanks the Institute of Automatic Control, Electronics, and Electrical Engineering at the University of Zielona Gora for the facilities and equipment for carrying out the EMI measurements.

References

[1] Boyuan Zhu, D. Leskarac, J. Lu, and M. Wishart, "Electromagnetic Interference Investigation of Solar PV System for Microgrid Structure," in *7th Asia Pacific International Symposium on Electromagnetic Compatibility*, pp. 456–459.

[2] S. Acharya, G. S. Member, and Y. Dvorkin, "Cybersecurity of Smart Electric Vehicle Charging : A Power Grid Perspective," *IEEE Access*, vol. 8, 2020.

[3] R. Smolenski, J. Bojarski, A. Kempski, and J. Luszcz, "Aggregated Conducted Interferences Generated by Group of Asynchronous Drives with Deterministic and Random Modulation," in *Asia-Pacific Symposium on Electromagnetic Compatibility*, 2012, pp. 6–9.

[4] R. Smolenski, P. Lezynski, J. Bojarski, W. Drozdz, and C. Long, "Electromagnetic Compatibility Assessment in Multiconverter Power Systems - Conducted Interference Issues ?," *Measurement*, p. 108119, 2020.

[5] F. Leferink, "Conducted interference, challenges and interference cases," *IEEE Electromagn. Compat. Mag.*, vol. 4, no. 1, pp. 78–85, 2015.

[6] X. Yue, D. Boroyevich, F. C. Lee, F. Chen, R. Burgos, and F. Zhuo, "Beat Frequency Oscillation Analysis for Power Electronic Converters in DC Nanogrid Based on Crossed Frequency Output Impedance Matrix Model," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3052–3064, 2018.

[7] Y. Qiu, M. Xu, K. Yao, J. Sun, and F. C. Lee, "Multifrequency Small-Signal Model for Buck and Multiphase Buck Converters," *IEEE Trans. POWER Electron.*, vol. 21, no. 5, pp. 1185–1192, 2006.

[8] H. Loschi, R. Smolenski, P. Lezynski, D. Nascimento, and G. Demidova, "Aggregated Conducted Electromagnetic Interference Generated by DC/DC Converters with Deterministic and Random Modulation," *Energies*, 2020.

[9] H. Loschi, P. Lezynski, R. Smolenski, D. Nascimento, and W. Sleszynski, "FPGA-Based System for Electromagnetic Interference Evaluation in Random Modulated DC / DC Converters," *Energies 2020*, vol. 13, no. 2389, pp. 1–14, 2020.

[10] H. Loschi, R. Smolenski, P. Lezynski, and D. Nascimento, "Reduction of Conducted Emissions in DC / DC Converters with FPGA-based Random Modulation," in *2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020.