A 22-nm FDSOI CMOS Low Noise Active Balun Achieving < -44-dBc HD3 up to 1.5-V_{p-p} Output Swing over 0.01-5.4-GHz for Direct RF Sampling Applications

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***Abstract*—In this article, we propose a CMOS active balun targeting high linearity up to high voltage swing and over wide bandwidth for direct RF sampling applications. All the blocks of this active balun are derived using a common highly linear building block (HLBB). The HLBB is designed using an inverter with strong source degeneration. To increase the linearity of this HLBB further, its nonlinearity mechanisms are analyzed in detail. A bootstrapping technique is included in the HLBB to reduce the dominant nonlinearity. Furthermore, a pre-distortion technique cancels most of the non-linearity of the output driving stages. All the linearization techniques proposed are robust to PVT changes. The measured results of the active balun realized on chip in a 22-nm FDSOI CMOS shows < -44-dBc HD3 up to 1.5-V_{p-p} output swing over 0.01-5.4-GHz. The measured gain and phase errors of the balun action are less than 0.5dB and $\pm 5^{\circ}$ respectively. The chip is powered from a 5V supply and dissipates 925mW.**

***Index Terms*—active balun, direct RF sampling, gigahertz ADC front-end, degeneration, bootstrapping, pre-distortion, PVT robust, HD3.**

I. Introduction

Advances in gigahertz Analog-to-Digital Converters (ADC) [1]–[4] greatly benefit many existing and emerging direct RF sampling applications. Measurement instruments like oscilloscopes [5]–[7] and communication testers [8] directly digitize signals with >4GHz analog bandwidth with >8 bits resolution. Such high performance gigahertz ADCs are also enabling direct RF sampling radios for electronic intelligence (ELINT) [9], data over cable service interface specification (DOCSIS) standards [10], and base station applications [11].

Fig. 1 shows a typical signal chain of a direct RF sampling application. A programmable gain amplifier (PGA) is followed by a filter that is optional and depends on the application, for example, an anti-aliasing or band-select filter. The ADC is preceded by a high performance block shown inside the dashed box. There are two main challenges this block needs to address. The first is to drive the input of the ADC up to its full scale voltage with high linearity over a wide bandwidth.

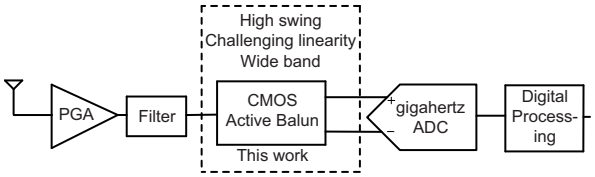

Fig. 1. Typical signal chain of a direct RF sampling application.

The second challenge arises because most of the above-mentioned RF sampling front-ends, i.e., inputs of oscilloscopes and in/outputs of PGA and filter are single-ended in nature. However, the signal from these single-ended inputs need to be converted into differential to feed the input of the ADC. Note that the input of gigahertz ADCs is generally differential in nature with each single-ended input terminating to ground with a 50Ω matching resistance [2], [3].

The existing realizations of such high performance blocks are either passive [12] or use exotic processes like SiGe [13] and BiCMOS [14]. Hence it is desired to implement this block in a CMOS process enabling further CMOS integration in direct RF sampling applications.

Due to the power-hungry gigahertz ADCs ([1]–[4]) which dissipate multiples of Watts, the aforementioned direct RF sampling applications trade-off power for the required high performance. Hence, the power consumption in the range less than a Watt is less of a concern in realizing the block shown in the dashed box to achieve high performance and CMOS integration capability to match the advances in the gigahertz ADCs.

A. Prior Art

The SiGe [13] and BiCMOS [14] active balun solutions achieve high linearity up to high voltage swings. But since they use feedback based architectures, their bandwidth is limited to 4GHz and 2GHz respectively.

Existing CMOS active baluns [15]–[19] mainly target heterodyne receiver applications and are designed for low voltage swings. This is because they are mostly followed by a

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down-converter and then an additional gain block at the base band frequencies (IF amplifier) to drive the ADC.

Nevertheless, such baluns can be succeeded by a highly linear, wide band differential amplifier (operating at RF frequencies) capable of delivering high voltage swings to realize the high performance block shown inside dashed box in Fig. 1. However, the voltage-swing ($< 0.9V_{p-p}$) and bandwidth ($<$ 4.5GHz) of existing CMOS highly linear differential amplifiers [20], [21] are still lower compared to our target. Moreover, the linearity performance of these amplifiers strongly depends on PVT values, and hence need sophisticated calibration circuits before their practical implementation. It is worth pointing out that the requirement to drive a matched output load in such wide band, highly linear, and high swing designs lead to significant power consumption. For example, $> 4\times$ power is dissipated in the buffer stage driving the matched output load in [20] compared to the power dissipated in the amplifier itself.

Though passive baluns can achieve high linearity without consuming dc power, they also require high-performance amplifiers to drive the ADC as discussed in the above paragraph. Moreover, passive baluns have their limitations in covering the frequency ranges from lower megahertz to upper gigahertz [22]. For example, flux-based baluns are more suitable at the lower megahertz range, whereas the capacitive coupled/transmission line-based baluns are more practical at the higher gigahertz range [22]. Though passive baluns that cover such a wide frequency range exist, they show performance degradation in one or more characteristics such as phase error [23], insertion loss [24], form-factor, etc.

In this work, we propose a CMOS active balun which operates over 0.01-5.4GHz while achieving < -44dBc HD3 when driving a matched load with up to $1.5V_{p-p}$ differential swing. The corresponding IIP3 is 17dBm with a 1dB gain compression at $2.8V_{p-p}$ differential output swing. The single-ended to differential voltage gain is 11dB. The gain and phase error of the balun action are less than 0.5dB and $\pm 5^\circ$ respectively, comparable to that of a passive balun [12]. The stacking capability and low bulk parasitics of the FDSOI technology aids to the various techniques proposed in this work to achieve high performance.

B. Architecture

Fig. 2 shows the proposed architecture. The first stage consists of 50Ω input matching and a low noise amplifier (LNA) to relax the noise requirement of the subsequent stages. It is loaded with a PVT robust pre-distorter (PD), followed by the actual balun and two output drivers. All these blocks are derived from a common highly linear building block (HLBB). The evolution, analysis and design of this HLBB is described in the next section.

II. Highly Linear Building Block

Fig. 3 shows the evolution of the common HLBB circuit that is used to derive all the blocks in Fig. 2. The evolution begins with an inverter (Fig. 3 (a)). Compared to its common source (nMOS or pMOS) amplifier counterparts, an inverter

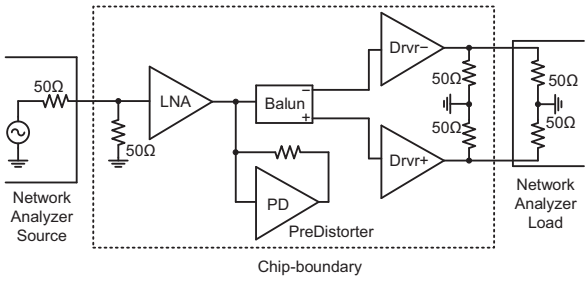


Fig. 2. Proposed CMOS active balun architecture.

provides higher g_m/I_d due to current reuse and higher linearity for higher voltage swings due to its complementary class-AB action. Minimum length transistors (20nm) are used for both nMOS and pMOS devices to maximize speed. However, a simple inverter cannot achieve the required linearity.

Feedback is a PVT robust way of increasing the linearity of a circuit. Global feedback around the CMOS active balun of Fig. 2 to achieve high linearity needs high loop gain up to 5.4GHz. This requires a very high unity gain bandwidth (UGB) of the loop, the stabilization of which becomes impractical in the presence of routing parasitics.

On the other hand, local feedback in the form of resistive source degeneration can operate till high frequencies and has less stability concerns. Thus, as shown in Fig. 3 (b), resistive source degeneration is employed as a first step to achieve high linearity. Many LNAs/LNTAs reported in the literature (e.g. [25]–[28]) utilize either resistive or inductive source degeneration to increase linearity. However, these works mainly target low power applications and hence employ weak or moderate source degeneration. In this work, power dissipation is less of a concern and a strong degeneration is used, which changes the dominant non-linearity and has implications for the circuit design as will be explained in the next section. Also in Fig. 3 (b), cascode transistors M_{nc} and M_{pc} were added for isolation.

A. Non-linearity mechanisms

To lower distortion further, M_{nb} and M_{pb} are inserted as shown in Fig. 3 (c). To explain the motivation for this, let us analyze the linearity of Fig. 3 (b) first. Here we examine the contribution of g_m and g_{ds} nonlinearities of M_{na} to the third order distortion of the output current i_L of the HLBB shown in Fig. 3(b) for various $g_{m1}R_S$ values, where $g_{m1}R_S$ represents the strength of the local feedback. Note that without loss of generality only nMOS M_{na} is considered in this analysis and also focus is on HD3, however, it can be extended to pMOS M_{pa} as well and also to the analysis of the HD2.

The strength of the local feedback $g_{m1}R_S$ is varied by scaling the dc current and width of M_{na} together. Cascode transistor M_{nc} is also scaled accordingly to support the dc current. R_S is kept constant since it determines the noise of the HLBB in moderate/strong degeneration cases.

Consider M_{na} in Fig. 3(b). The drain-source current i_{ds} of M_{na} can be characterized for its g_m nonlinearity by obtaining

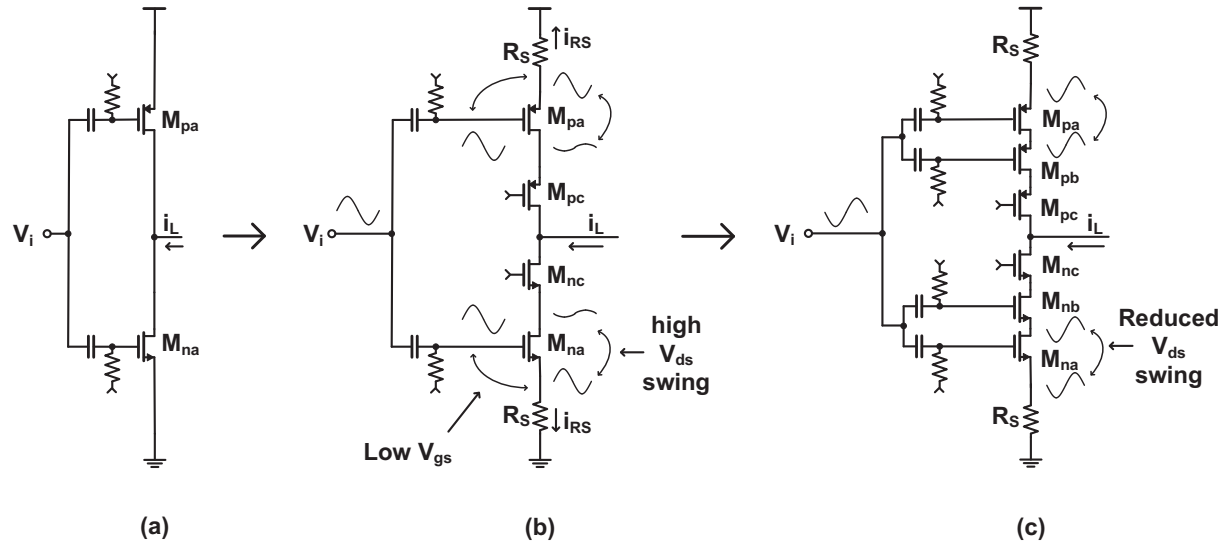


Fig. 3. Evolution of the HLBB from (a) inverter with (b) source degeneration to increase g_m linearity, and (c) bootstrap technique to increase g_{ds} linearity.

i_{ds} as a polynomial function of v_{gs} while keeping drain-source and bulk-source voltages of M_{na} constant:

$$i_{ds}(v_{gs}) = g_{m1}v_{gs} + g_{m2}{v_{gs}}^2 + g_{m3}{v_{gs}}^3 + g_{m4}{v_{gs}}^4 + .. \quad (1)$$

Similarly, i_{ds} can be characterized for its g_{ds} nonlinearity by plotting i_{ds}-v_{ds} characteristics of M_{na} while keeping its gate-source and bulk-source voltages constant:

$$i_{ds}(v_{ds}) = g_{ds1}v_{ds} + g_{ds2}{v_{ds}}^2 + g_{ds3}{v_{ds}}^3 + g_{ds4}{v_{ds}}^4 + .. \quad (2)$$

We follow the technique from [29]–[31] for linearity analysis. The technique applied to analyze the effect of g_m and g_{ds} nonlinearities of M_{na} on third order distortion of i_L is briefly described in the following steps:

1) Draw the linear small-signal circuit model of Fig. 3 (b) and symbolically obtain v_{gs} and v_{ds} of the transistors whose nonlinearity is analyzed, as a function of v_i.
2) Enter the expressions of v_{gs} and v_{ds} from the previous step in (1) and (2) to obtain an expression for the third-order non-linear currents $g_{m3}v_{gs}^3$ and $g_{ds3}v_{ds}^3$.
3) Treat these nonlinear currents as small signal currents and determine their contribution to the output current once again using the small-signal circuit model.

For an applied input voltage of v_i to the HLBB, the gate-source voltage v_{gs} of M_{na} can be calculated using the linear circuit model as:

$$v_{gs} = \frac{1}{1 + g_{m1}R_S} \times v_i \quad (3)$$

Note that g_{ds1} is neglected in (3) since g_{m1}/g_{ds1} (≈ 21 in our case, from simulations) is high.

Now, the third order nonlinear current generated in M_{na} due to g_{m3} is:

$$g_{m3}{v_{gs}}^3 = g_{m3} \times \frac{{v_i}^3}{(1 + g_{m1}R_S)^3} \quad (4)$$

Similarly, the voltage swing v_{ds} also can be approximately calculated to be $-v_i$ assuming dc bias condition and dimension of M_{nc} to be similar to that of M_{na}. Hence, the third order nonlinear current generated in M_{na} due to g_{ds3} of (2) and v_{ds} swing is:

$$g_{ds3}{v_{ds}}^3 = -g_{ds3}{v_i}^3 \quad (5)$$

Now, the contributions of (4) and (5) on third order distortion of i_L need to be calculated. For this, observe that the third order current i_{RS} flowing into R_S also flows completely into the output, i.e., i_L. Hence, the contribution of (4) and (5) to i_L can be evaluated by calculating their contribution to i_{RS}.

Treating (4) as small signal current, it divides between R_S and $1/g_m$ and the amount that ends up in R_S and hence at output is:

$$i_{L,gm3} = g_{m3} \times \frac{{v_i}^3}{(1 + g_{m1}R_S)^3} \frac{1}{(1 + g_{m1}R_S)} \quad (6)$$

It is worth pointing out that (6) can be obtained by using feedback theory as well [32], [33], where $g_{m1}R_S$ represents the loop gain. However, we use the technique from [29]–[31] which simplifies not only the analysis when the g_{ds} nonlinearity is included but also the calculations of the individual nonlinearity contributions.

Similar to (6), the contribution of g_{ds3} to the third order distortion of i_L can be calculated as:

$$i_{L,gds3} = -g_{ds3}{v_i}^3 \frac{1}{(1 + g_{m1}R_S)} \quad (7)$$

Now, (6) and (7) can be used to study the contributions of g_m and g_{ds} nonlinearities of M_{na} to the third order output current of i_L as a function of strength of source degeneration, $g_{m1}R_S$. When $g_{m1}R_S$ is increased by scaling M_{na} as mentioned before, $i_{L,gm3}$ in (6) decreases approximately as a cube of the scaling factor. This is because, though the denominator of (6) increases approximately as a fourth power

of the scaling factor, g_{m3} in the numerator also increases linearly due to the scaling of M_{na}.

However, $i_{L,gds3}$, even though initially increases slightly when $g_{m1}R_S$ is increased from lower values (≈ 1), becomes constant, as for higher $g_{m1}R_S$ values both the numerator and denominator increase linearly and cancel each other's effect.

Thus, by increasing $g_{m1}R_S$ the effect of g_m nonlinearity will decrease, but the effect of g_{ds} nonlinearity remains approximately constant such that it will become dominant. The $g_{m1}R_S$ value at which the contribution of g_{ds} nonlinearity becomes equal to that of g_m nonlinearity can be calculated by equating (6) and (7):

$$g_{m1}R_S = \sqrt[3]{\frac{g_{m3}}{g_{ds3}}} - 1 \tag{8}$$

Note that due to the minimum length transistor (20nm), g_{ds} nonlinearity is higher due to the increased short channel effects and starts to dominate the overall nonlinearity at lower source degeneration strength ($g_{m1}R_S$) compared to that of a transistor with higher channel length.

To quantitatively verify this analysis, we still need to find the actual values of g_{m1}, g_{m3}, and g_{ds3} used in the above equations. g_{m1} and g_{m3} are obtained by extracting the polynomial in (1). For this, a circuit simulator is used to plot the i_{ds}-v_{gs} characteristics of the individual M_{na} transistor. Note that, for this simulation, the source of M_{na} is grounded, and constant drain-source and bulk-source voltages are maintained such that they are equal to the corresponding biasing voltages of M_{na} in Fig. 3 (b). Similarly, parameters in (2) are obtained by plotting the i_{ds}-v_{ds} characteristics of M_{na} while keeping its gate-source and bulk-source voltages constant.

Fig. 4 shows the simulation result of the third order output distortion current $i_{L,3}$ for a v_i of $400mV_{p-p}$ sinusoidal at $100MHz$ across $g_{m1}R_S$ values ($R_S = 19\Omega$). The dotted and dashed lines in Fig. 4 show respectively the calculated contributions of g_{m3} and g_{ds3}. Both (6) and (7) are divided by four[1] to calculate the resulting current at the third harmonic. The intersection point of the dotted and dashed lines in Fig. 4 indicates the calculated $g_{m1}R_S(\approx 3)$ at which transition of dominant g_m nonlinearity to g_{ds} nonlinearity occurs.

As shown in Fig. 4, this point coincides well with the point where the overall simulated $i_{L,3}$ stops decreasing and a further increase in $g_{m1}R_S$ is ineffective. Therefore, to further increase the linearity of the HLBB, a technique to reduce g_{ds} nonlinearity of the input transistors is required.

Fig. 5 shows the simulated v_{gs} and v_{ds} swings of M_{na} for $g_{m1}R_S$ of 1.6 and 3.2 when $v_i = 400mV_{p-p}$ at $f_{in} = 100MHz$. It can be observed that v_{gs} decreases with the increase in $g_{m1}R_S$ whereas v_{ds} swing does not change.

It is worth pointing out that in addition to g_{m3} and g_{ds3} of (1) and (2) respectively, there are more nonlinearity mechanisms that can contribute to the simulated $i_{L,3}$. The cross terms [34] of M_{na}, i.e., $g_{m1ds2}v_{gs}{v_{ds}}^2$ and $g_{m2ds1}{v_{gs}}^2v_{ds}$, are two among such nonlinearity mechanisms. However, since the simulated $g_{m3}{v_{gs}}^3$ and $g_{ds3}{v_{ds}}^3$ are much

[1] $cos^3(\omega t) = \frac{cos(3\omega t)}{4} + 3\frac{cos\omega t}{4}$

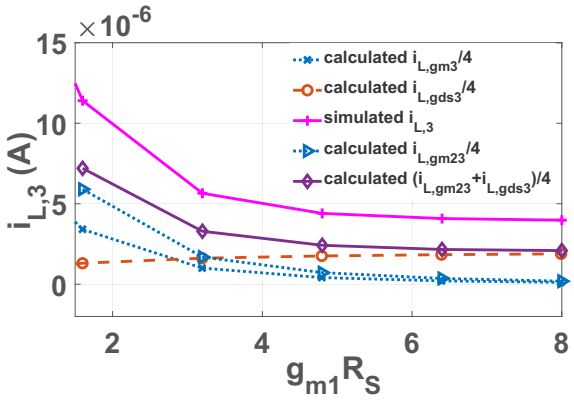


Fig. 4. Simulated third order output distortion current along with the calculated g_m and g_{ds} nonlinearity contributions of M_{na} for $v_i = 400mV_{p-p}$ and $f_{in} = 100MHz$.

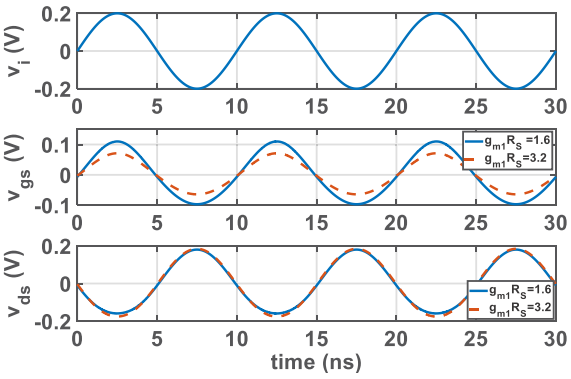


Fig. 5. Simulated transient voltage swings v_i, v_{gs}, and v_{ds} for $v_i = 400mV_{p-p}$ at $f_{in} = 100MHz$ when $g_{m1}R_S$=1.6 and 3.2.

higher than $g_{m1ds2}v_{gs}{v_{ds}}^2 + g_{m2ds1}{v_{gs}}^2v_{ds}$ for all $g_{m1}R_S$ values in our case, the cross terms are not included in the analysis.

Another nonlinearity mechanism that adds considerably to the simulated $i_{L,3}$ is the contribution of the quadratic term in (1) due to the feedback [28]. (6) can be modified to include this contribution from the quadratic term [32], [33] and hence the overall contribution of g_m nonlinearity is:

$$i_{L,gm23} = (g_{m3} - \frac{2{g_{m2}}^2}{g_{m1}}) \times \frac{{v_i}^3}{(1+g_{m1}R_S)^4} \tag{9}$$

It can be seen from Fig. 4 that the inclusion of the quadratic term increases the accuracy of the calculated nonlinearity. However, this contribution of the quadratic term only slightly changes $g_{m1}R_S$ at which g_{ds} nonlinearity becomes equal to that of g_m nonlinearity. Fig. 4 also includes the total calculated contributions of g_m and g_{ds} nonlinearities.

Volterra series [35] can be used to further increase the accuracy of the calculated $i_{L,3}$, but it is also more complex. Since the simpler model used in this work gives insight into the distortion mechanisms and is still fairly accurate, the Volterra analysis is not used.

B. Bootstrapping

Addressing the dominant g_{ds} nonlinearity, transistors M_{nb} and M_{pb} in saturation region are inserted as shown in Fig. 3 (c). This reduces the v_{ds} swing across M_{na} and M_{pa} significantly such that according to (5), g_{ds} nonlinearity of M_{na} and M_{pa} does not limit the output distortion at high $g_{m1}R_S$ values.

Although the high v_{ds} swing now shifts to M_{nb} and M_{pb}, the contribution of g_{ds} non-linearity of these transistors to the output current is much lower. Assuming identical M_{na}, M_{nb}, and M_{nc}, the v_{ds} swing of M_{nb} will be the same as with M_{na} before and (5) is still valid. However, this nonlinear current now divides between $1/g_{m1}$ of M_{nb} and the impedance looking into the drain of M_{na} and ends up in the output current as:

$$i_{L,gds3btst} = -g_{ds3}{v_i}^3 \frac{1}{(1 + g_{m1}R_S \times \frac{g_{m1}}{g_{ds1}})} \tag{10}$$

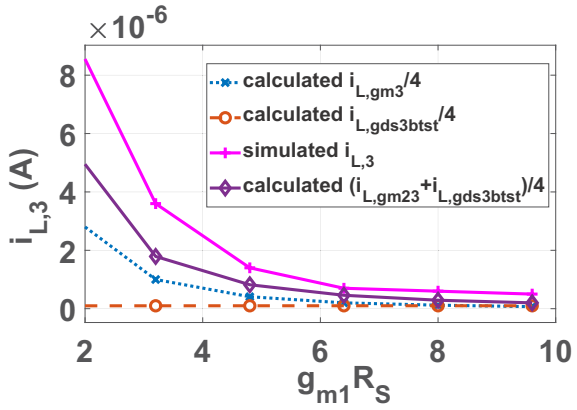


Fig. 6. Simulated third order distortion current when the bootstrapping technique is used to reduce the g_{ds} nonlinearity contribution of M_{na}, calculated g_m nonlinearity of M_{na} and g_{ds} nonlinearity of M_{nb} are also shown; $v_i = 400mV_{p-p}$ and $f_{in} = 100MHz$.

Therefore, the g_{ds} nonlinearity contribution of M_{nb} (10) is lower by a factor of g_{m1}/g_{ds1} compared to that of M_{na} (7) without bootstrapping.

Fig. 6 shows the simulated $i_{L,3}$ with bootstrapping and the same conditions as Fig. 4. $i_{L,3}$ flattens out at higher $g_{m1}R_S$ values than before and the resulting distortion is therefore also lower.

Fig. 7 shows v_{gs} and v_{ds} of M_{na} after bootstrapping for $g_{m1}R_S$ of 3.2 and 8 when $v_i = 400mV_{p-p}$ at $f_{in}100MHz$. v_{gs} swing decreases with the increase in $g_{m1}R_S$ as expected. Note that v_{ds} of M_{na} becomes negligible due to bootstrapping. Fig. 7 also shows that high v_{ds} swing now shifts to M_{nb}.

For $v_i = 400mV_{p-p}$ used for the simulation and analysis of the nonlinearity mechanisms of the HLBB, the contributions of the higher order (> 3) terms of the polynomials (1) and (2) to $i_{L,3}$ are negligible. However, for larger input signal levels, their contributions increase. This becomes more relevant for the HLBBs that are used as drivers in Fig. 2 as they experience maximum input/output swing. Furthermore, it is worth pointing out that at input power levels of the active balun approaching $CP1dB$, cascode transistors M_{nc} and M_{pc} of the

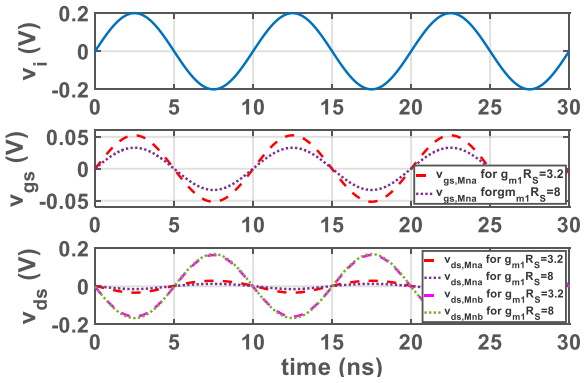


Fig. 7. Simulated transient voltage swings v_i, v_{gs}, and v_{ds} for $v_i = 400mV_{p-p}$ at $f_{in} = 100MHz$ when $g_{m1}R_S$=3.2 and 8.

HLBBs used as drivers enter the triode region and dominate the nonlinearity. A pre-distortion technique that improves both the small signal and large signal linearity of the drivers will be discussed in Section III-D.

C. Comparison of Bootstrapping and Increasing the Channel Length

Since the bootstrapping technique as shown in Fig. 3 (c) requires headroom for drain-source voltages of two additional transistors, it needs higher supply voltage compared to that of Fig. 3 (b). Hence, it is worth analyzing the linearity improvement obtained by increasing the channel length of the HLBB without bootstrapping (Fig. 3 (b)). For this, consider Fig. 8 which shows simulated third order output distortion current of the HLBB with and without bootstrapping when minimum length transistors (20nm) are used. $v_i = 400mV_{p-p}$ and $f_{in} = 100MHz$ are used for this simulation.

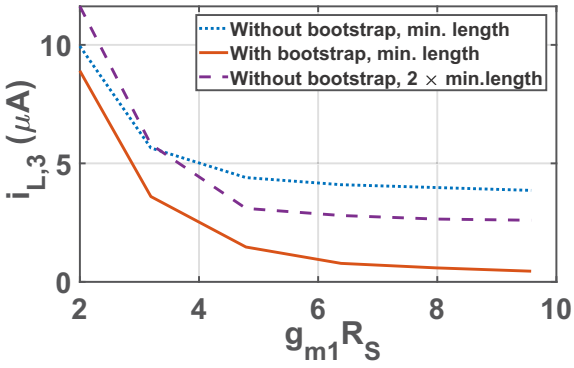


Fig. 8. Simulated third order output distortion current of nMOS half circuit of the HLBB comparing the bootstrapping technique (Fig. 3 (c)) with minimum length transistors to that without bootstrapping technique (Fig. 3 (b)) but using transistors with 2× minimum length for $v_i = 400mV_{p-p}$ and $f_{in} = 100MHz$.

Fig. 8 also shows the corresponding simulation results when the length of the transistors in the HLBB without bootstrapping (Fig. 3 (b)) is increased by two times (40nm). The width of the transistors is adjusted such that the same g_{m1} is obtained for a given dc current as in the case of minimum length transistors. When compared to the HLBBs

using minimum length transistors, its linearity is higher than the case without bootstrapping, but is much lower than the case with bootstrapping. Moreover, gate-source and gate-drain capacitances increases by about 2.7× when the transistor lengths are doubled. This will decrease the bandwidth of the active balun proportionally as will be shown in Section III-F and IV-A. Thus, the HLBB with bootstrapping using minimum length transistors outperforms the HLBB without bootstrapping using higher channel length transistors when it comes to achieving high linearity over wide bandwidth.

D. Biasing

A high I_{dc} is needed in the HLBB to achieve high $g_{m1}R_S$ for high linearity with low R_S for low noise. Hence there is a significant $I_{dc} \times R_S$ drop across R_S resulting in high supply-voltage and power-dissipation. A source degenerated current bleeder is used to reduce this power as shown in Fig. 9(a). The parallel branches containing M_{nd}/M_{pd} handle a significant part of I_{dc} reducing the voltage across R_S.

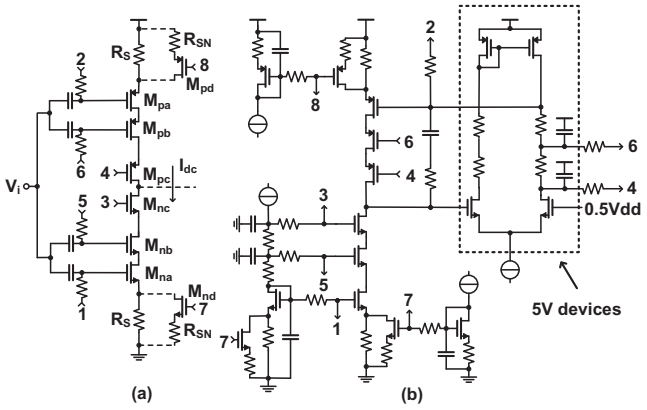


Fig. 9. Circuit diagram of the (a) HLBB with low noise source degenerated current bleeding, and (b) replica bias circuit of the HLBB

Fig. 9(b) depicts the replica bias circuit for the HLBB to stack up the low-voltage (0.88V) transistors in the high-voltage (5V) supply. The simulated maximum gate-source voltage during the ramp-up of 5V supply is <420mV which is lower than 0.88V. The corresponding maximum gate-drain (<850mV) and drain-source voltages(<820mV) during this simulation are also well below the maximum limit (2.4V) at which they can be used [36]. Because of the isolation between the D/S and back-gate terminals of the transistors in the FDSOI technology, there is no risks of the forward-bias diode formation like that in a bulk process. This has enabled stacking 8 transistors in 5V supply to realize the HLBB.

III. Active Balun: Analysis and Design

Fig. 10 shows the full schematic of the CMOS active balun. All blocks are derived from impedance scaled versions of the common HLBB. The LNA is obtained by impedance scaling the HLBB for low noise. The LNA is loaded by the pre-distorter (PD), another impedance scaled version of the HLBB. The PD block required for this is obtained by diode connecting the input and output of the HLBB. The PD block cancels most of the nonlinearity of the driver stages as will be described in section III-D. The balun stage is also an HLBB where the single ended voltage v_{ib} at the gates of the transistors M_1/M_2 is converted into differential voltages ${v_{ob}}^+$ and ${v_{ob}}^-$ at the sources of M_1/M_2 and drains of M_3/M_4 respectively. The drivers are HLBBs driving the matched output load.

A detailed analysis of the various properties of the CMOS active balun along with the design considerations for its different blocks is provided next.

A. Matching

A 50 Ω (R_i) resistor in series with inductor L_S is used at the input of the LNA for input matching. L_S provides gain peaking and extends the input matching bandwidth limited by the capacitance at the gate of the transistors of the LNA. The output differential matching is obtained by two series 50Ω (R_o) resistors between the output of the driver amplifiers with C_{CM} (50pF) providing common mode output matching.

B. Gain

Due to the strong source degeneration, the effective transconductance of the HLBB is mainly determined by its source degeneration resistances. Overall voltage gain is therefore:

$$\frac{{v_o}^+ - {v_o}^-}{v_i} \approx \frac{R_{PD}}{R_{LNA}} \times \frac{R_{BLN} + R_{OB}}{R_{BLN}} \times \frac{R_o \parallel R_L}{R_{DRV}} \quad (11)$$

The overall 12dB voltage gain is divided as 4, 5, and 3dB respectively among the LNA, balun, and the driver stages and was chosen as a trade-off between a high LNA gain relaxing the noise requirements on the subsequent stages at the cost of increased distortion due to the higher swings. This designed gain reduces to 11.6dB after the extracted simulations because of the attenuation in the ac-coupling capacitors between the stages due to the layout parasitics.

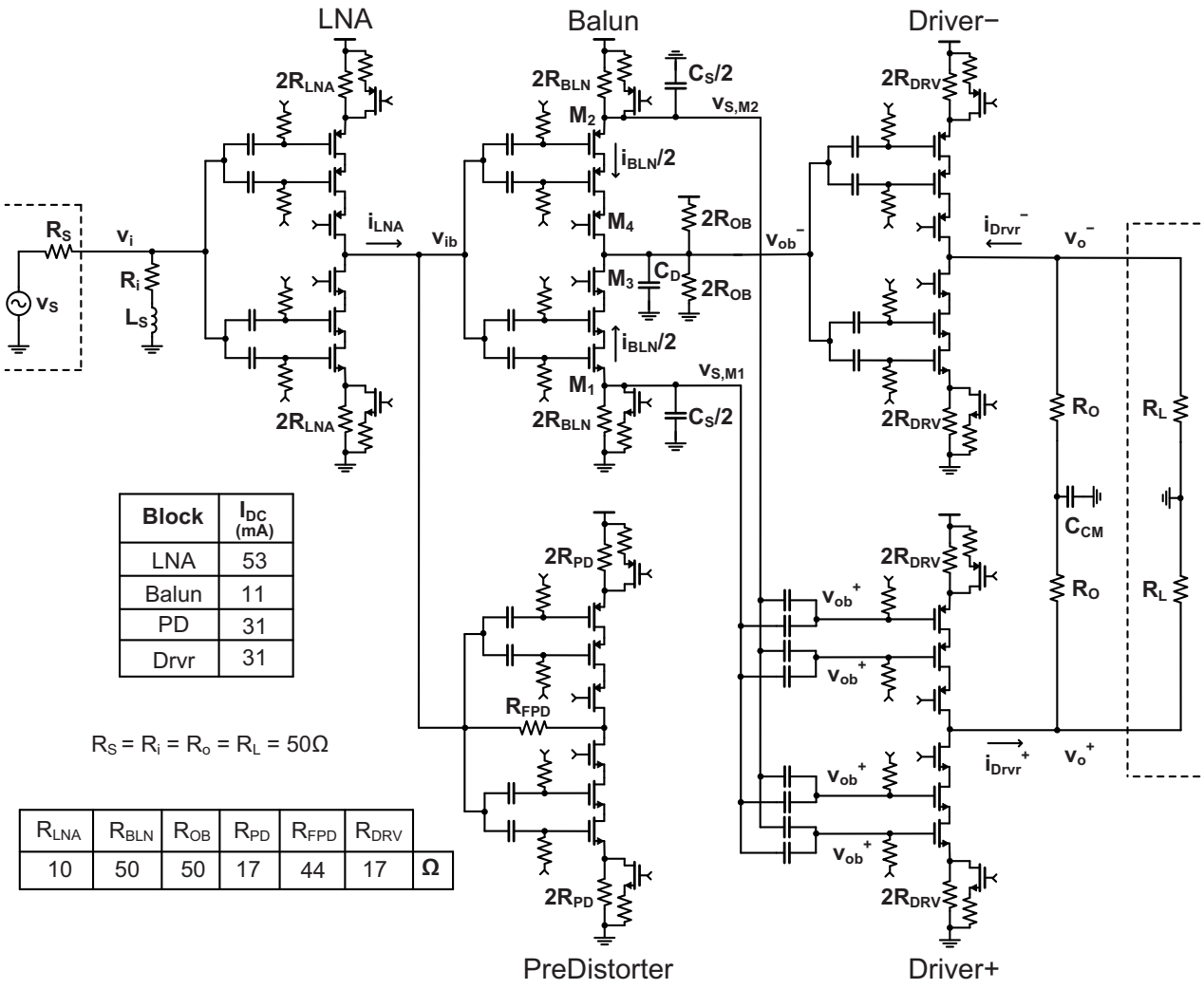
C. Balance

The balun block converts the single-ended input voltage to a differential output voltage. Since g_m/C_{gs} of the minimum length transistors is much higher than the targeted bandwidth, the output differential voltages ${v_{ob}}^+$ and ${v_{ob}}^-$ of the balun as shown in Fig. 10 can be written as functions of its single-ended input v_i as:

$$\frac{{v_{ob}}^+(s)}{v_{ib}(s)} = \frac{g_m R_{BLN}}{1 + g_m R_{BLN}} \quad (12)$$

$$\frac{{v_{ob}}^-(s)}{v_{ib}(s)} = -\frac{g_m R_{OB}}{1 + g_m R_{BLN}} \left(\frac{1 + sR_{BLN}C_S}{1 + sR_{OB}C_D} \right) \quad (13)$$

where g_m is the sum of the transconductance of M_1 and M_2, C_S represents the parallel combination of the effective capacitance from the source of M_1 and M_2 to the ground, and C_D indicates the effective capacitance from the drains of M_3 and M_4 to the ground.



Block	I_{DC} (mA)
LNA	53
Balun	11
PD	31
Drvr	31

$R_S = R_i = R_o = R_L = 50\Omega$

R_{LNA}	R_{BLN}	R_{OB}	R_{PD}	R_{FPD}	R_{DRV}	
10	50	50	17	44	17	Ω

Fig. 10. Full schematic of the CMOS active balun.

The low frequency gain of (12) and (13) are balanced by matching R_{BLN} and R_{OB}, and their high frequency phase are balanced by matching C_S and C_D. C_S and C_D track each other over process and temperature variations as both mainly consist of gate-to-channel and overlap capacitances due to the negligible bulk parasitics in the FDSOI technology.

Fig. 11 shows the simulated gain and phase errors across PVT changes. The overall variation in the gain and phase errors are $< \pm 0.6$dB and $< \pm 6°$ respectively. Fig. 12 shows the Monte Carlo simulations for 300 runs under nominal conditions. For this simulation, mismatch is enabled for all the components in the balun and driver blocks of the active balun. It can be observed that the effect of the mismatch on the gain and phase errors is negligible due to the large device sizes used (to obtain high transconductance and low resistance values).

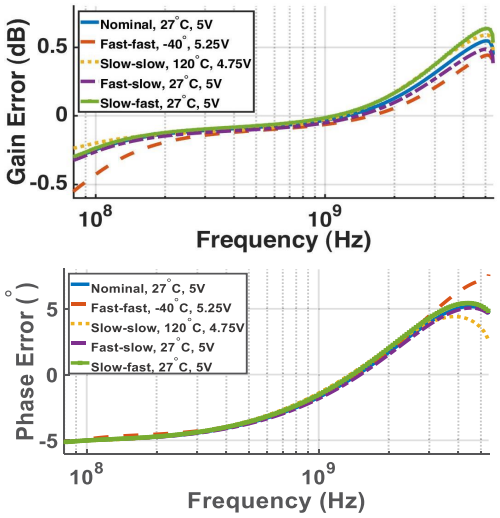


Fig. 11. Simulated results of the balance action of the active balun across PVT variations.

D. Linearity

In Section II the strong degeneration and bootstrapping technique was discussed that improved the HLBB linearity. To improve the linearity even further, pre-distortion is applied.

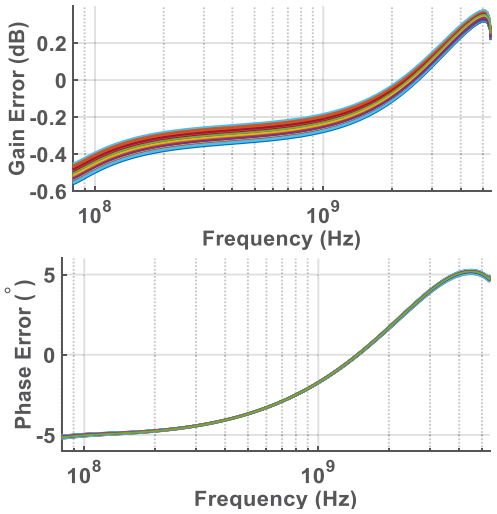


Fig. 12. Monte Carlo Simulations (300 points) of the active balun under nominal condition.

The dashed line in Fig. 13 (a) shows the simulated HD3 of Fig. 10 as a function of P_{in} at 100MHz. This simulation mainly illustrates the nonlinearity contribution of the LNA and balun as the drivers are replaced with ideal blocks and the PD block is replaced with its equivalent input resistance.

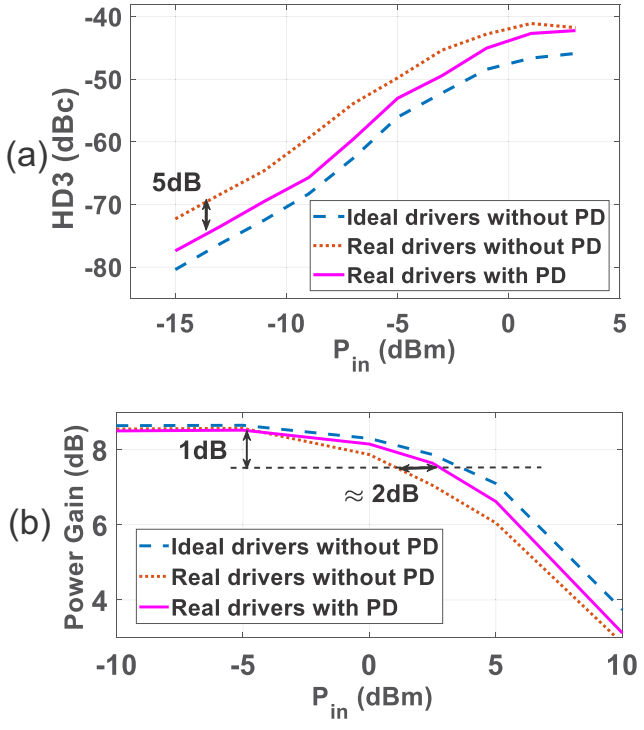


Fig. 13. (a) HD3 and (b) CP1dB simulations of the active balun across P_{in} (at 100MHz) showing linearity benefits of the proposed pre-distortion technique.

The dotted line in Fig. 13 (a) shows the simulated HD3 when the ideal driver blocks are replaced with their real counterparts adding significant distortion due to the high voltage swings. The HD3 increases by about 8dB at lower input power levels compared to that when the drivers are ideal. Furthermore, the compression point decreases by approximately 3dB as shown in the CP1dB simulations in Fig. 13 (b).

The PD block as shown in Fig. 10 cancels the nonlinear current generated by the drivers and thereby not only increases the overall linearity of the active balun at lower power levels, but also improves its compression point. As shown in Fig. 14, the PD block with feedback resistor R_{FPD} creates a low input impedance such that most of the signal current i_{LNA} flows through R_{FPD}. Similar to a current mirror, this will create a non-linear input voltage for the PD to absorb this current. The balun transfers this voltage to the input of the drivers which in turn generate output currents that are as linear as i_{LNA}.

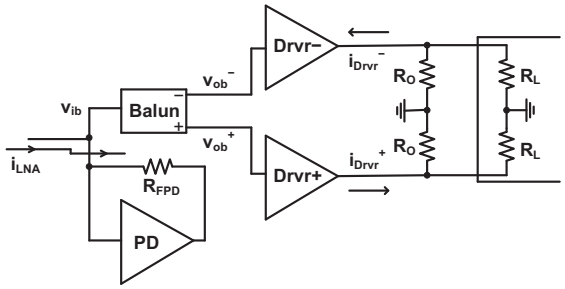


Fig. 14. Part of the block diagram of the active balun to illustrate pre-distortion linearization.

Note that for the technique to be effective, the pre-distorter and the drivers are designed with the same transistor and resistor dimensions and also for the same gain. This becomes particularly important at higher signal power levels as the nonlinearity due to output voltage swing dominates. This is because of the cascode transistors transitioning from the saturation region to the triode region. Thus, the proposed pre-distortion technique improves the active balun's HD3 and large signal CP1dB. From Fig. 10, for the gains of the PD and the drivers to be the same:

$$\frac{R_{FPD}}{R_{PD}} - 1 = \frac{R_o \parallel R_L}{R_{DRV}} \tag{14}$$

Note that the gains of the PD and the drivers are ratios of the resistors, and hence track well across PVT. This is a significant advantage, for example, compared to the technique such as post-distortion in [37], which measured $>$ 15dBm lower IIP3 (equivalently $30dB$ higher HD3) than their simulation due to the increased g_{ds} nonlinearity as the gains of the driver amplifier and the post-distorter did not track each other across PVT.

Because of the large devices used in the PD and driver blocks (to obtain high trans-conductances and low resistances) of our design, the proposed pre-distortion is less sensitive to mismatch as well. Furthermore, only one pre-distorter is sufficient to improve the linearity of both the drivers. However, note that though the technique decreases both the even and odd-order nonlinearity of the $Driver^+$ block, it only reduces the odd-order nonlinearity of the $Driver^-$ block.

The pre-distortion analysis presented here focuses on highlighting the characteristics of the proposed technique and

its merits/demerits. Further analysis of such pre-distortion and post-distortion techniques can be found in [37], [38], and [39].

The solid line in Fig. 13 shows the simulated HD3 and power gain when the PD block is included. Thus this simulation contains all the real blocks in Fig. 10. Compared to the case without the PD (and with real drivers), an improvement of 5dB is obtained in the HD3, while CP1dB is improved by 2dB. The HD3 and CP1 dB are slightly worse than the case with the real drivers indicating the nonlinearity cancellation of the driver blocks is imperfect. This is attributed to the slightly lower I/O swing of the driver blocks compared to that of the PD due to slightly < 1 voltage transfer by the balun block.

E. PVT robustness of the linearity

The dashed lines in Fig. 15 shows the simulated PVT variation of the HD3 without the PD. Hence this simulation mainly illustrates the PVT variation of the strong source degeneration and the bootstrapping techniques. The HD3 varies 7dB across the simulated PVT variation. This corresponds to an OIP3 change of 3.5dB which is significantly less than some other techniques achieving high linearity [21], [40], so calibration circuits are not required to optimize the linearity.

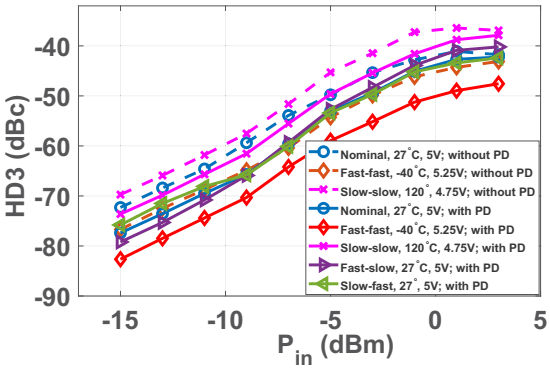


Fig. 15. HD3 simulations of the active balun across P_{in} (at 100MHz) for various PVT combinations.

The solid lines in Fig. 15 show the corresponding HD3 across PVT when the PD block is included and hence demonstrate PVT robustness of the proposed pre-distortion technique. Compared to the case without PD (dashed line), the HD3 improves between 4 and 6dB across PVT. Note that since the gains of the PD and driver amplifiers are ratios of resistors, their input/output swings track each other across PVT. Hence the reduction in both g_m and g_{ds} nonlinearities due to the pre-distortion is robust across PVT. In addition to its robustness across PVT, the proposed pre-distortion technique also does not require tuning at various input power levels like in [20]. The nonlinearity cancellation due to the pre-distortion in [20] needs to be optimized for each given input power level (gain setting).

The overall variation in the linearity across PVT is <9dB as shown in the solid lines of Fig. 15. Since both the nMOS and pMOS are used in the design, the skewed process corner (slow nMOS, fast pMOS and vice versa) conditions are also simulated. Since the linearization techniques do not depend on any cancellation/correlation between the nMOS and pMOS devices, variation in the HD3 due to skewed corners is less than that due to the fast-fast and slow-slow corners.

F. Noise and bandwidth

Because of the strong source degeneration, the overall output noise mainly consists of noise contribution of the source degeneration resistors of the various blocks apart from that of the input matching resistor. The noise of R_{FPD} at the input of the PD is negligible and it mostly appears at the output of the PD, which is not used. The noise due to R_{OB} and R_{BLN} appears mainly at the $v_o{}^-$ output. Hence, the simulated noise figure (NF) with respect to single ended output ports as depicted in Fig. 16 shows higher NF for the $v_o{}^-$ port compared to that of the $v_o{}^+$ port. Fig. 16 also shows the simulated overall NF. The simulated degradation in the noise figure with respect to input power is <0.05dB up to $P_{in} = -5dBm$ at $f_{in} = 100MHz$. However, it degrades by 0.76dB for P_{in} corresponding to CP1dB.

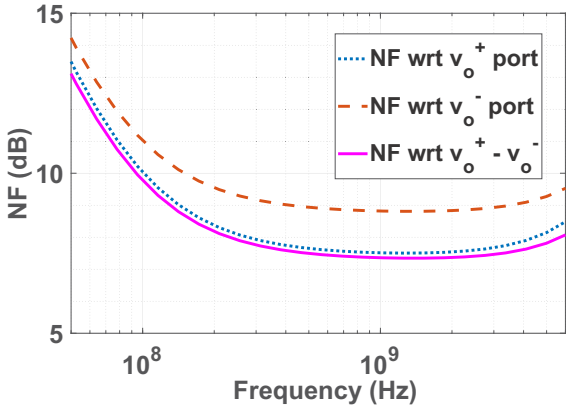


Fig. 16. Simulated NF.

The simulated lower and upper cut-off frequencies of the active balun are 4.22MHz and 5.85GHz respectively. The lower cut-off frequency is determined by the ac coupling in it. Though the simulated bandwidths of the individual HLBBs are >7GHz, their cascading effect and inclusion of the bondwire/bondpad parasitics limit the overall upper cut-off frequency.

IV. Experimental Results

The active balun was realized on chip in a 22-nm FDSOI CMOS process. A 5 V supply powers the chip. Fig. 17 shows the chip photo. The layout of the HLBBs is folded around the output node of each HLBB such that the supply and ground are close together and can be decoupled well. Top layer thick metals are stacked to route the supply and ground to minimize the voltage drop in these routings due to the large dc currents. The chip is mounted on the ground plane of a PCB using a thermal glue. The bond-wires to the PCB are 400μm long and avoid bandwidth limitations due to packaging.

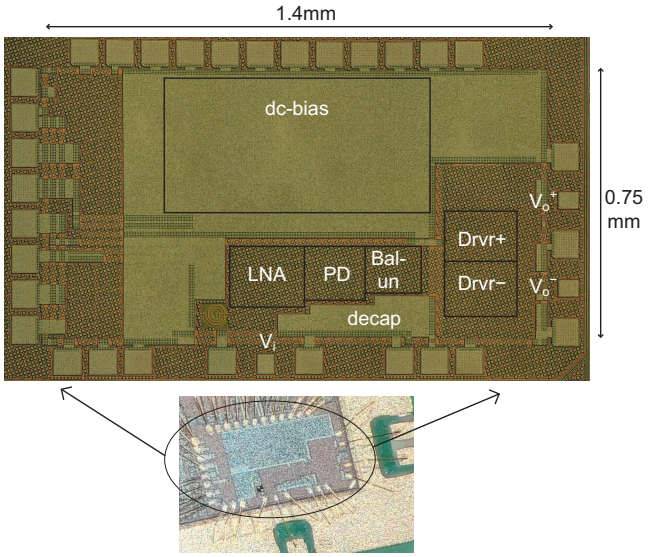


Fig. 17. Chip photograph showing the placement of various blocks; the chip is directly mounted on a PCB and wire-bonded.

A. Measurement Results

I/O matching and the gain of the active balun are characterized using a vector network analyzer (VNA). Fig. 18 shows the measured i/o matching. S_{11} reduces to $-8dB$ at 5.4GHz mainly due to the loading from the gate-drain capacitances of the bootstrapping transistors of the LNA. S_{dd22} and S_{cc22} in Fig. 18 represents the differential and common mode output matching. The output matching also degrades at higher frequencies ($-10dB$ at 5.4GHz) due to the gate-drain capacitances of the cascode transistors of the driver amplifiers. Since i/o matching measurements also include the transmission line (approximately 2cm long for both input and output) effects on the PCB, they contain ripples compared to their simulated counterparts (dashed lines).

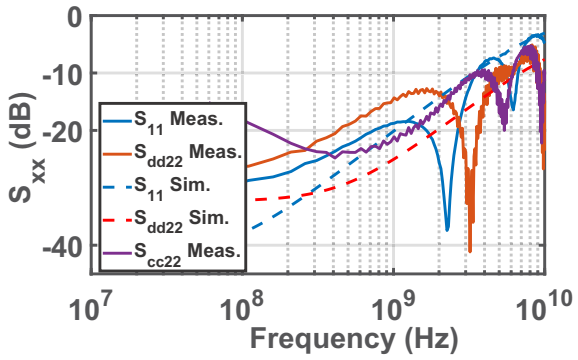


Fig. 18. Measured input and output matching of the active balun.

Fig. 19 shows the measured single-ended to differential voltage gain. The measured gain is around 11dB which is 0.6dB lower compared to the extracted simulations (dashed line). The lower side frequency of the measured gain is limited by the vector network analyzer used.

Fig. 20 shows the measured NF. An external wide band passive balun is used to feed the differential output into the single-ended input port of the measurement equipment. The measured NF is 7.8dB (0.4dB worse compared to the extracted simulation). The measured flicker corner is around 100MHz as expected in the simulation.

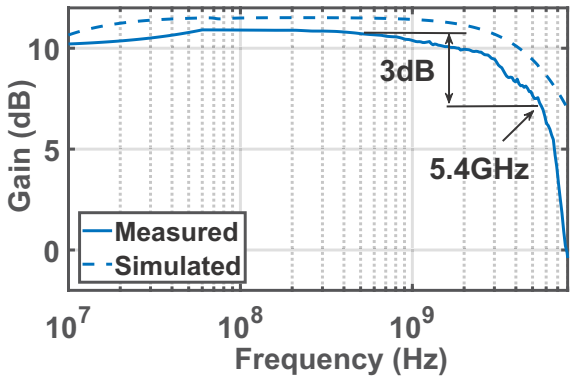


Fig. 19. Measured gain of the active balun.

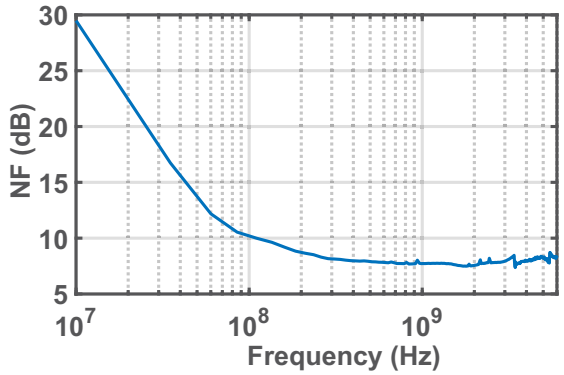


Fig. 20. Measured NF of the active balun.

The measured gain and phase imbalance of the active balun are shown in Fig. 21. One input terminal and two output terminals of the active balun are connected to three single-ended ports of a vector network analyzer for this measurement. The measured gain and phase errors are less than $\pm 0.5dB$ and $\pm 5^\circ$ respectively up to 5.4GHz.

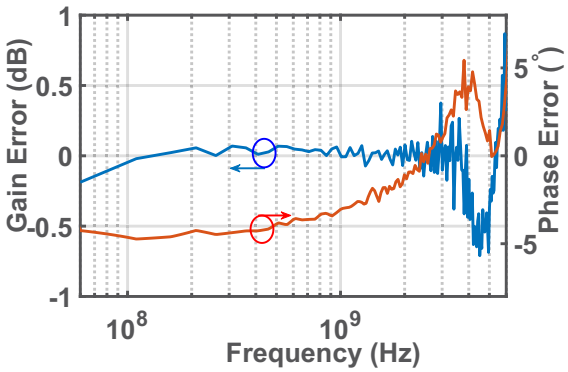


Fig. 21. Measured gain and phase imbalance of the active balun.

Fig. 22 (a) shows the measured HD2 and HD3 at an input frequency of 100MHz. The measured HD2 and HD3 are

$< -47dBC$ and $< -51dBc$ respectively up to $-4dBm$ input power. Fig. 22 (a) also shows the measured compression point which is 2dBm when referred to the input. Fig. 22 (b) shows the measured HD2/HD3 across various input frequencies at $P_{in} = -4dBm$. The HD3 degrades from $-51dBc$ at an input frequency of 100MHz to around $-44dBc$ at 1GHz. The HD3 decreases with increasing frequency as the nonlinear capacitors in the active balun start to contribute to the third order output distortion at higher frequencies. However, due to the minimum length transistors used and the negligible bulk capacitances (which are mostly nonlinear), the reduction of the HD3 at higher frequencies is significantly lower compared to the prior art [13], [14]. Nevertheless, high frequency nonlinear MOS capacitance linearization techniques such as [41] can be investigated to improve the HD3 at high frequencies.

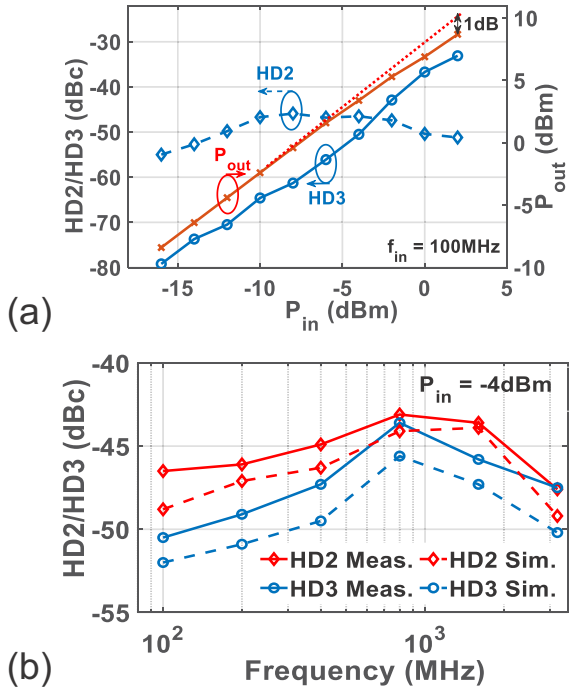


Fig. 22. Measured (a) HD2, HD3, 1dB compression point at 100MHz input, and (b) HD2, HD3 across input frequency.

Note that the harmonic distortion products are filtered at higher input frequencies due to the bandwidth limitation of the circuit, resulting in an improvement in the corresponding measured HD2 and HD3. However, this is not the case for the IMD3 products which fall inside the band. This can be observed in the measured IIP3 in Fig. 23 which monotonically decreases with the increasing frequency. Nevertheless, an IIP3 $> 14dBm$ is measured up to 3.2GHz. For this measurement, two tones are apart at 50MHz from the center frequencies and the IIP3 is obtained at P_{in} (per tone) of $-10dBm$. This P_{in} corresponds to the same input/output voltage swing as that of the (single-tone) HD3 measurement with P_{in}=$-4dBm$. Fig. 23 also shows the measured IIP2 for the same set up.

B. Robustness Measurements

Fig. 24 (a), (b), and (c) shows the measured gain error and phase error for variation in the supply voltage, temperature

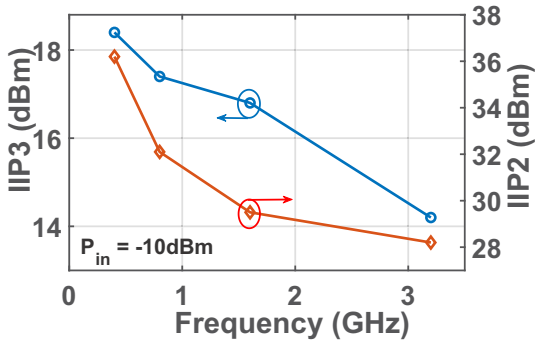


Fig. 23. Measured IIP3, IIP2 across input frequency.

and samples. The overall variation in the gain error and phase error are less than $\pm$0.4dB and $\pm6^\circ$ respectively. This verifies the effectiveness of employing the minimum length transistors in achieving wide band balance action while simultaneously attaining high linearity by using them in strong source degeneration. Though the measured four samples are from the same batch, it gives an indication of the sample-to-sample variation.

Fig. 25 (a), (b), and (c) shows the measured HD3 at $f_{in} = 100MHz$ across supply voltage, temperature and samples respectively. It can be observed that the change in HD3 is negligible against variation in supply voltage from 3.5V to 5.5V. This is mainly because the variation in supply voltage is divided among eight stacked transistors and the source degenerated resistors, hence reducing the headroom of the individual transistors only slightly. This can also be seen from the measured output power of the active balun against P_{in} for various supply voltages shown in Fig. 26. It can be observed that compared to for a 5V supply, the gain of the active balun reduces by 0.8dB (at low P_{in}) and CP1dB decreases by $\approx$3dB for a 3.5V supply. The measured variation in HD3 is 4.4dB across 0-80°C change in temperature.

C. Comparison

Table I lists the performance summary of the circuit and compares it with the state of the art. References [13] and [14] also target direct RF sampling applications and achieve HD3 comparable to this work. Note that Table I also includes the measured performance of the active balun with supply voltage of 4V along with that with 5V. This is because the output voltage swing $2.8V_{p-p}$ of the active balun corresponding to its 1dB compression point with 5V supply is much higher than the output voltage swing at which [13] and [14] report their linearity (HD3/HD2). With 4V supply, the active balun achieves comparable maximum output swing.

Both [13] and [14] employ feedback around differential amplifiers to achieve high linearity and their bandwidths are limited to 4GHz and 2GHz respectively compared to 5.4GHz of this work. NF of [13], [14] (12.1dB and 9.5dB respectively) are much higher compared to 7.8dB of this work. This better performance does, however, come at the cost of a higher power consumption. Furthermore, unlike [13], [14] which use SiGe

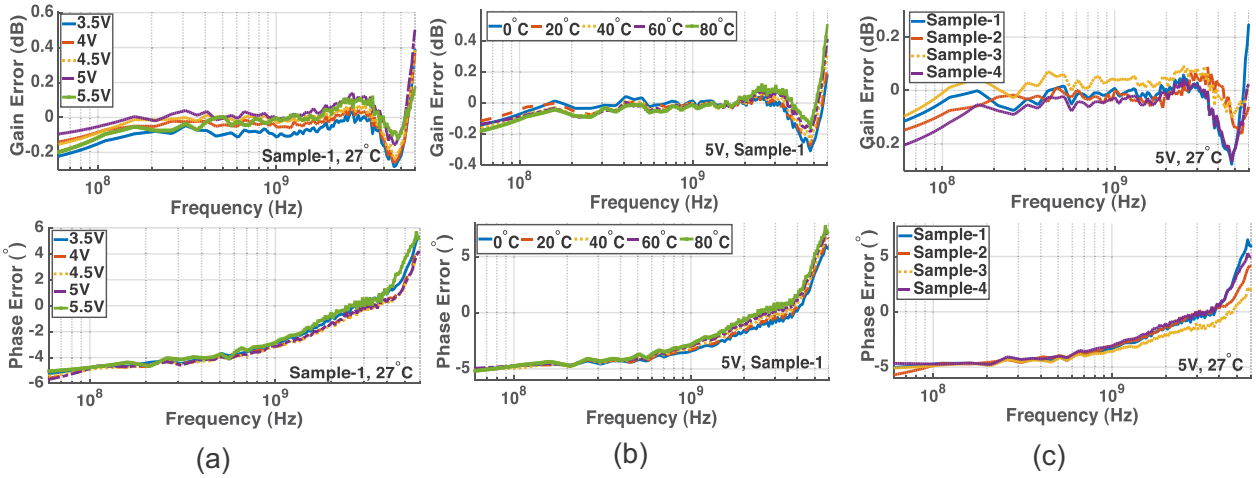


Fig. 24. Measured robustness of the balance action of the active balun across (a) supply voltage, (b) temperature, and (c) sample variations.

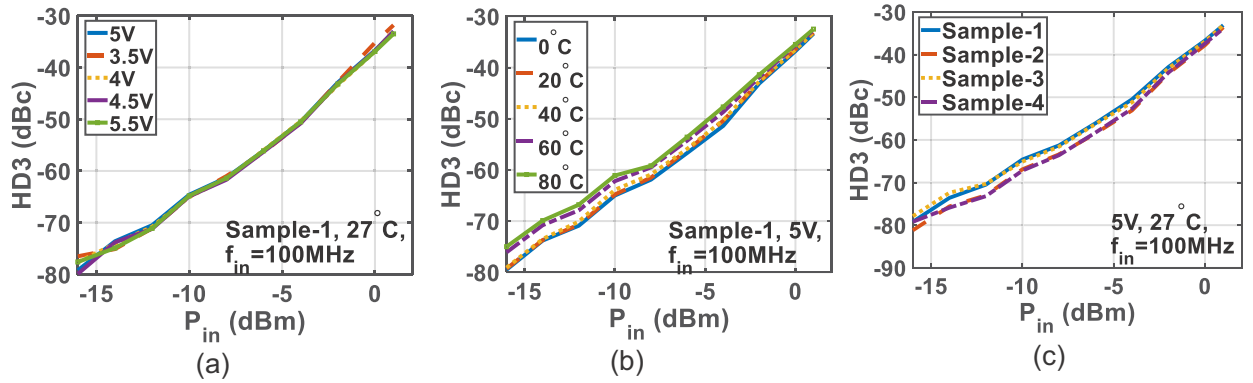


Fig. 25. Measured robustness of the HD3 of the active balun across (a) supply voltage, (b) temperature, and (c) sample variations at 100MHz input.

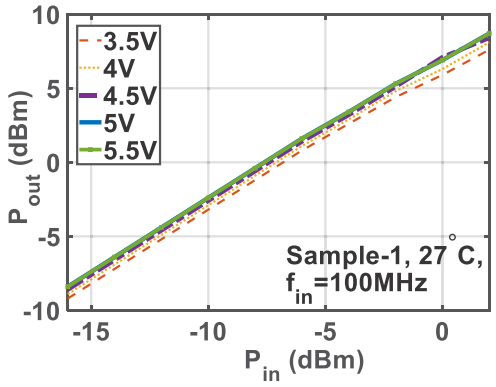


Fig. 26. Measured P_{out} against P_{in} across supply voltage variations at 100MHz input.

and BiCMOS processes respectively, this work is realized fully in CMOS.

Table I also shows prior art CMOS active baluns [17]–[19] . The active balun in [17] lacks gain and measured much higher gain-error and noise compared to this work. Furthermore, [17] achieves lower output voltage swing than ours and did not measure HD3/IIP3. Though [20] does not include balun functionality, it is included in the table as it also aims to drive gigahertz ADCs. Compared to this work, [20] achieves higher IIP3 but lower bandwidth and output voltage swing. The high linearity of [20] depends on the optimization of the implemented pre-distortion at every gain settings without which its IM3 degrades by more than 20dB.

Other CMOS active baluns [18], [19] in the table achieve much lower linearity at much lower i/o voltage swings compared to our work. However, they target low power applications such as front ends of a user equipment and hence require relaxed linearity specifications. It is worth pointing out that the performance metrics (of this work and the state of the art) reported in Table I are based on the respective measurements at nominal conditions unless specified otherwise.

V. Conclusion

The proposed CMOS active balun achieves high linearity over 0.01-5.4GHz bandwidth while driving matched load with up to $2.8V_{p-p}$ differential swing. Strong source degeneration is used along with the bootstrapping technique to increase the

TABLE I
RESULT SUMMARY AND COMPARISON WITH PRIOR ART

	Unit	This Work		[13]	[14]	[17]	[18]	[19]	[20]
Technology		CMOS 22nm FDX	CMOS 22nm FDX	SiGe	BiCMOS	CMOS 130nm	CMOS 28nm	CMOS 65nm	CMOS 28nm FDX
Bandwidth	GHz	0.005-5.4	0.005-5.55	DC-4	DC-2	1-8	1-6.2	0.05-1.3	0.4-4.5
HD3*[a]/IIP3[a]	dBc / dBm	-44^{b}/ 14.2^{c}	-43^{b}/ 13.8^{c}	-48^{c}/ 11^{c}	-56^{b}/ -	- / -[d]	- / −10	- / −2.2	-/ 21
Max. working i/o swing ◇	$Vpp,in/Vpp,out$	0.4/1.4	0.31/1.1	0.14/1	0.25/1	0.5/1	20m/200m	2m/30m	0.23/0.65
O/P matching		Yes	Yes	No	No	Yes	No	No	Yes
Balun		Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Voltage gain	dB	11	10.2	17	12	-1.2 / 0^{Δ}	20	24	9
NF	dB	7.8	8.3	12.1	9.5	11.2 / 10.2^{Δ}	2.2	3	7.25
Gain/phase error	dB / °	±0.5 / ±5	±0.5 / ±5	-	±0.35†/ -	3.6 / 5.6	-	0.08 / 0.5	-
HD2*[e]/IIP2[e]	dBc / dBm	−44 / 31.8	−40.5 / 28.2	−46.5 / -	−54 / -	- / -	- / -	- / 19.6	- / 11.2
Supply Voltage	V	5	4	5	5	3	1	1	1.5
Power	mW	925	540	430	275	93	7.4	5.7	120
Area	mm^2	1	1	7.5⋆⋆	5.25⋆⋆	0.14	0.08	0.046	1

∗ at $1.5V_{pp,out}$
a Worst case HD3/IIP3 in their respective frequency range of operation (bandwidth)
b at 1GHz
c at 3.2GHz
d IIP3 not measured (CP1dB = 6.1dB)
e Worst case HD2/IIP2 in their respective frequency range of operation (bandwidth)
◇ i/o swings per tone of the two tone test up to which OIM3 follows 3dB/dB
Δ Measured separately for plus and minus output ports
† calculated from the ratio of single-ended to common-mode gain and single-ended to differential gain (S_{cs21}/S_{ds21})
⋆⋆ Package

linearity of the HLBB used as the fundamental building block. The proposed pre-distortion method cancels most nonlinearity of the driver amplifiers. All linearization techniques proposed are robust across PVT. Minimum length transistors used along with the negligible bulk capacitance results in low phase imbalance at high frequencies. To the best of the authors' knowledge, no CMOS active balun realizations in literature feature the large signal linearity over wide bandwidth and low noise like the proposed circuit, paving the road toward further integration of high-performance RF blocks in direct RF sampling applications.

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