SAW-LESS RADIO RECEIVERS IN CMOS

Yuan-Ching Lien

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Yuan-Ching Lien
Born on 24th Feb. 1980 in Taipei, Taiwan

Dit proefschrift is goedgekeurd door:

de promotor prof.dr.ir. B. Nauta

de assistent-promotor dr.ing. E.A.M. Klumperink

Abstract

Smartphones play an essential role in our daily life. Connected to the internet, we can easily keep in touch with family and friends, even if far away, while ever more apps serve us in numerous ways. To support all of this, higher data rates are needed for ever more wireless users, leading to a very crowded radio frequency spectrum. To achieve high spectrum efficiency while reducing unwanted interference, high-quality band-pass filters are needed. Piezo-electrical Surface Acoustic Wave (SAW) filters are conventionally used for this purpose, but such filters need a dedicated design for each new band, are relatively bulky and also costly compared to integrated circuit chips. Instead, we would like to integrate the filters as part of the entire wireless transceiver with digital smartphone hardware on CMOS chips. The research described in this thesis targets this goal.

It has recently been shown that N-path filters based on passive switched-RC circuits can realize high-quality band-select filters on CMOS chips, where the center frequency of the filter is widely tunable by the switching-frequency. As CMOS downscaling following Moore's law brings us lower clock-switching power, lower switch on-resistance and more compact metal-to-metal capacitors, N-path filters look promising. This thesis targets SAW-less wireless receiver design, exploiting N-path filters. As SAW-filters are extremely linear and selective, it is very challenging to approximate this performance with CMOS N-path filters. The research in this thesis proposes and explores several techniques for extending the linearity and enhancing the selectivity of N-path switched-RC filters and mixers, and explores their application in CMOS receiver chip designs.

First the state-of-the-art in N-path filters and mixer-first receivers is reviewed. The requirements on the main receiver path are examined in case SAW-filters are removed or replaced by wideband circulators. The feasibility of a SAW-less Frequency Division Duplex (FDD) radio receiver is explored, targeting extreme linearity and compression

requirements. A bottom-plate mixing technique with switch sharing is proposed. It improves linearity by keeping both the gate-source and gate-drain voltage swing of the MOSFET-switches rather constant, while halving the switch resistance to reduce voltage swings. A new N-path switch-RC filter stage with floating capacitors and bottom-plate mixer-switches is proposed to achieve very high linearity and a second-order voltage-domain RF-bandpass filter around the LO frequency. Extra out-of-band (OOB) rejection is implemented combined with V-I conversion and zero-IF frequency down-conversion in a second cross-coupled switch-RC N-path stage. It offers a low-ohmic high-linearity current path for out-of-band interferers. A prototype chip fabricated in a 28 nm CMOS technology achieves an in-band IIP3 of +10 dBm , IIP2 of +42 dBm, out-of-band IIP3 of +44 dBm, IIP2 of +90 dBm and blocker 1-dB gain-compression point of +13 dBm for a blocker frequency offset of 80 MHz. At this offset frequency, the measured desensitization is only 0.6 dB for a 0-dBm blocker, and 3.5 dB for a 10-dBm blocker at 0.7 GHz operating frequency (i.e. 6 and 9 dB blocker noise figure). The chip consumes 38-96 mW for operating frequencies of 0.1-2 GHz and occupies an active area of 0.49 mm^2.

Next, targeting to cover all frequency bands up to 6 GHz and achieving a noise figure lower than 3 dB, a mixer-first receiver with enhanced selectivity and high dynamic range is proposed. Capacitive negative feedback across the baseband amplifier serves as a blocker bypassing path, while an extra capacitive positive feedback path offers further blocker rejection. This combination of feedback paths synthesizes a complex pole pair at the input of the baseband amplifier, which is up-converted to the RF port to obtain steeper RF-bandpass filter roll-off than the conventional up-converted real pole and reduced distortion. This thesis explains the circuit principle and analyzes receiver performance. A prototype chip fabricated in 45 nm Partially Depleted Silicon on Insulator (PDSOI) technology achieves high linearity (in-band IIP3 of +3 dBm, IIP2 of +56 dBm, out-of-band IIP3 = +39 dBm, IIP2 = +88 dB) combined with sub-3 dB noise figure. Desensitization due to a 0-dBm blocker is only 2.2 dB at 1.4 GHz operating frequency.

Finally, to demonstrate the performance of the implemented blocker-tolerant receiver chip designs, a test setup with a real mobile phone is built to verify the sensitivity of the receiver chip for different practical blocking scenarios.

Samenvatting

Smartphones spelen een essentiële rol in ons dagelijks leven. Verbonden met internet kunnen we gemakkelijk contact houden met familie en vrienden, zelfs als ze ver weg zijn, terwijl steeds meer apps ons op verschillende manieren van dienst zijn. Om dit alles te ondersteunen, zijn hogere datasnelheden nodig voor steeds meer draadloze gebruikers, wat leidt tot een zeer druk radiofrequentiespectrum. Om een hoge spectrumefficiëntie te bereiken en tegelijkertijd ongewenste interferentie te verminderen, zijn hoogwaardige banddoorlaatfilters nodig. Piëzo-elektrische SAW (Surface Acoustic Wave) filters worden gewoonlijk voor dit doel gebruikt, maar dergelijke filters hebben een specifiek ontwerp voor elke nieuwe band nodig. Bovendien zijn ze relatief groot en ook duur in vergelijking met chips met geïntegreerde schakelingen. In plaats daarvan zouden we de filters graag mee integreren op CMOS-chips. Het onderzoek beschreven in dit proefschrift richt zich op dit doel.

Recent is aangetoond dat zogenaamde “N-path filters” op basis van passief geschakelde RC-circuits hoogwaardige band-selectiefilters op CMOS-chips kunnen worden gerealiseerd, waarbij de centrumfrequentie van het filter over een groot bereik kan worden afgestemd door middel van de schakelfrequentie. Aangezien CMOS schaling volgens de wet van Moore resulteert in zuiniger klokcircuits, lagere switchweerstand en compactere metaal-oxide-metaalcondensatoren, ziet de toekomst voor N-path filters erveelbelovend uit. Dit proefschrift richt zich op het ontwerp van draadloze ontvangers zonder SAW-filters, waarbij gebruik wordt gemaakt van N-path filters. Omdat het SAW-filter extreem lineair en selectief is, is het zeer uitdagend om deze prestaties te benaderen met CMOS N-path filters. Het onderzoek in dit proefschrift bevat verschillende technieken voor het verbeteren van de lineariteit en de selectiviteit van N-path switched-RC filters en mixers, en onderzoekt hun toepassing in CMOS-ontvangers.

Eerst wordt de state-of-the-art in N-path filters en mixer-first-ontvangers besproken. De vereisten voor het voornaamste ontvanger traject worden onderzocht in het geval dat SAW-filters worden verwijderd of vervangen door breedband circulatoren. De haalbaarheid van een FDD (Frequency Division Duplex) radio-ontvanger zonder SAW filters wordt verkend, gericht op extreme lineariteit en compressie eisen. Daarvoor wordt een nieuwe “bottom-plate Mixing” techniek met switch-sharing voorgesteld. Deze verbetert de lineariteit door zowel de gate-source- als gate-drain-spanning van de MOSFET-schakelaars vrij constant te houden, terwijl de schakelaarweerstand gehalveerd wordt om spannings variaties te verminderen. Een nieuwe N-path switched-RC filtertrap met “floating capacitors” en bottom-plate mixer-schakelaars wordt voorgesteld om een zeer hoge lineariteit en een tweede orde voltage-domein RF-bandpassfilter rond de LO-frequentie te bereiken. Extra OOB (out-of-band) onderdrukking wordt geïmplementeerd in combinatie met V-I-omzetting en zero-IF frequentieconversie gebruik makend van twee kruisgekoppelde N-path trappen. Dit biedt een laagohmig stroompad met hoge lineariteit voor out-of-band-interferenties. Een prototype-chip gefabriceerd in een 28 nm CMOS-technologie bereikt een in-band IIP3 van + 10 dBm, IIP2 van + 42 dBm. Voor out-of-band is een IIP3 van +44 dBm, IIP2 van +90 dBm en blocker 1-dB compressiepunt van +13 dBm voor een blocker-frequency offset van 80 MHz gehaald. Hierbij is de gemeten desensitisatie slechts 0,6 dB voor een 0-dBm blocker en 3,5 dB voor een 10-dBm blocker bij een RF frequentie van 0,7 GHz (d.w.z. 6 en 9 dB blocker Noise Figure). De chip verbruikt 38-96 mW voor frequenties van 0,1-2 GHz en heeft een actief oppervlak van 0,49 mm^2.

Vervolgens wordt gepoogd om alle frequentiebanden tot 6 GHz te dekken en een ruisgetal van minder dan 3 dB te bereiken, via een mixer-first -ontvanger architectuur met verbeterde selectiviteit en een hoog dynamisch bereik. Negatieve capacitieve terugkoppeling over de basisbandversterker dient daarbij als filtering, terwijl een extra capacitief positief terugkoppelpad verdere blocker onderdrukking biedt. Deze combinatie van feedbackpaden synthetiseert een complex poolpaar aan de ingang van de

basisbandversterker, die omhoog wordt geconverteerd naar de RF-poort om steile RF-bandpassfiltering te verkrijgen en verminderde vervorming. Dit proefschrift verkent het circuitprincipe en analyseert de prestaties van de ontvanger. Een prototype-chip vervaardigd in 45 nm PDSOI (Partially Depleted Silicium On Isolator) technologie behaalt een hoge lineariteit (in-band IIP3 van +3 dBm, IIP2 van +56 dBm, out-of-band IIP3 = +39 dBm, IIP2 = +88 dB) gecombineerd met sub-3 dB ruisgetal. Desensibilisatie door een 0-dBm blocker is slechts 2,2 dB bij een werkfrequentie van 1,4 GHz.

Om de prestaties van de geïmplementeerde blocker-tolerante ontvangers te demonstreren, werd ten slotte een testopstelling met een echte mobiele telefoon gebouwd om de gevoeligheid van de ontvangerchip voor verschillende praktische blocker scenario's te verifiëren.

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CHAPTER 1
Introduction

1.1 Wireless Communication

Wireless communication plays an important role in our daily life. It exists everywhere and keeps growing. Different communication standards have been developed over time for various applications, adding new functionalities. For example, early GSM was developed for mobile full duplex (two-way) voice telephony, the Bluetooth standard allowed exchanging data over short distances, e.g. between phones and personal audio devices, while Wi-Fi technology and recent 3G and 4G phones standards offer wireless data-connections to the Internet. All the required radio transceiver hardware is preferably implemented in a single battery powered device. The first handheld mobile phone was produced by Motorola in 1973 and the prototype weighed 1.1 kg, while offering a talk time of just 30 minutes. Nowadays mobile phones have much more functionality and a longer lasting battery, while supporting multi-band and multi-standard radio connection in different radio frequency bands roughly between 500 MHz and 6 GHz [1]. This increased functionality is realized while size, weight and cost of mobile phones have been reduced generously. To make this happen, large efforts in research and development have been and are still made, and this thesis is a contribution to that.

1.2 Motivation

The development of powerful mobile phones is to a large extend based on the evolution of the Integrated Circuits (IC) or “chip”, which was invented by Jack Kilby in 1959 [2, 3].

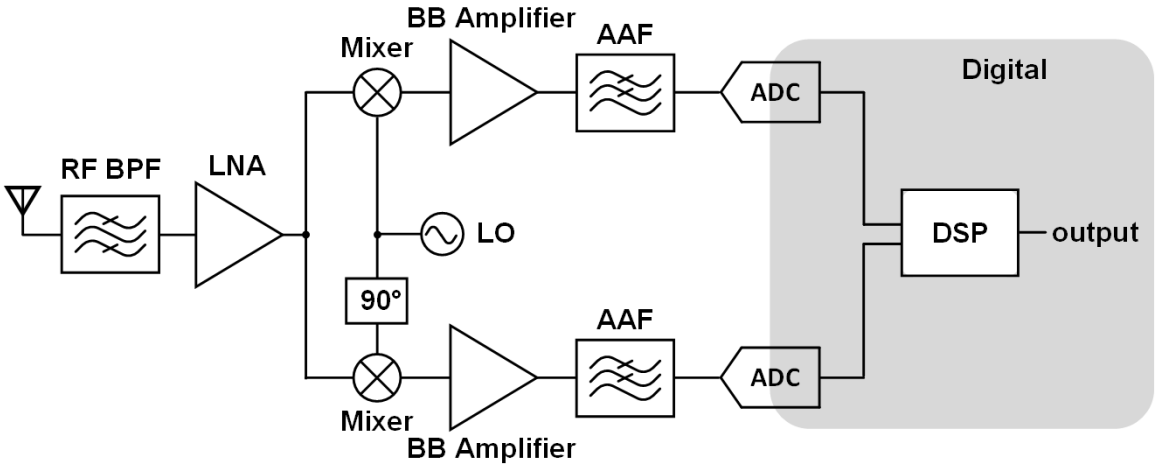

Fig. 1.1: An example of a radio receiver.

ICs contain a set of interconnected electronic components on a piece of semiconductor, usually silicon. Especially silicon chips with CMOS transistors (Complementary Metal-Oxide-Semiconductor, invented by Frank Wanlass in 1963 [4]) plays a crucial role, as both digital computer hardware and analog and radio frequency hardware can be combined on one chip. Already in 1965, Gordon Moore accurately predicted that the number of components on a CMOS IC would double every two years [5, 6], a prediction widely known as Moore's Law. By making components smaller, more complex systems can be integrated on a single chip, while speed improvements and power consumption reductions are also possible.

Fig. 1.1 shows the block diagram of a radio frequency (RF) receiver for one band or one standard [7, 8]. In this thesis, we will mainly focus on the radio frequency receiver part (excluding the digital signal processing), also referred to as the "analog front-end (AFE)". It consists of an antenna, RF bandpass filter (BPF), Low Noise Amplifier (LNA), down-conversion mixer driven by a Local Oscillator (LO), Baseband amplifiers, channel and anti-aliasing filter (AAF) and analog-to-digital converter (ADC). The radio signal

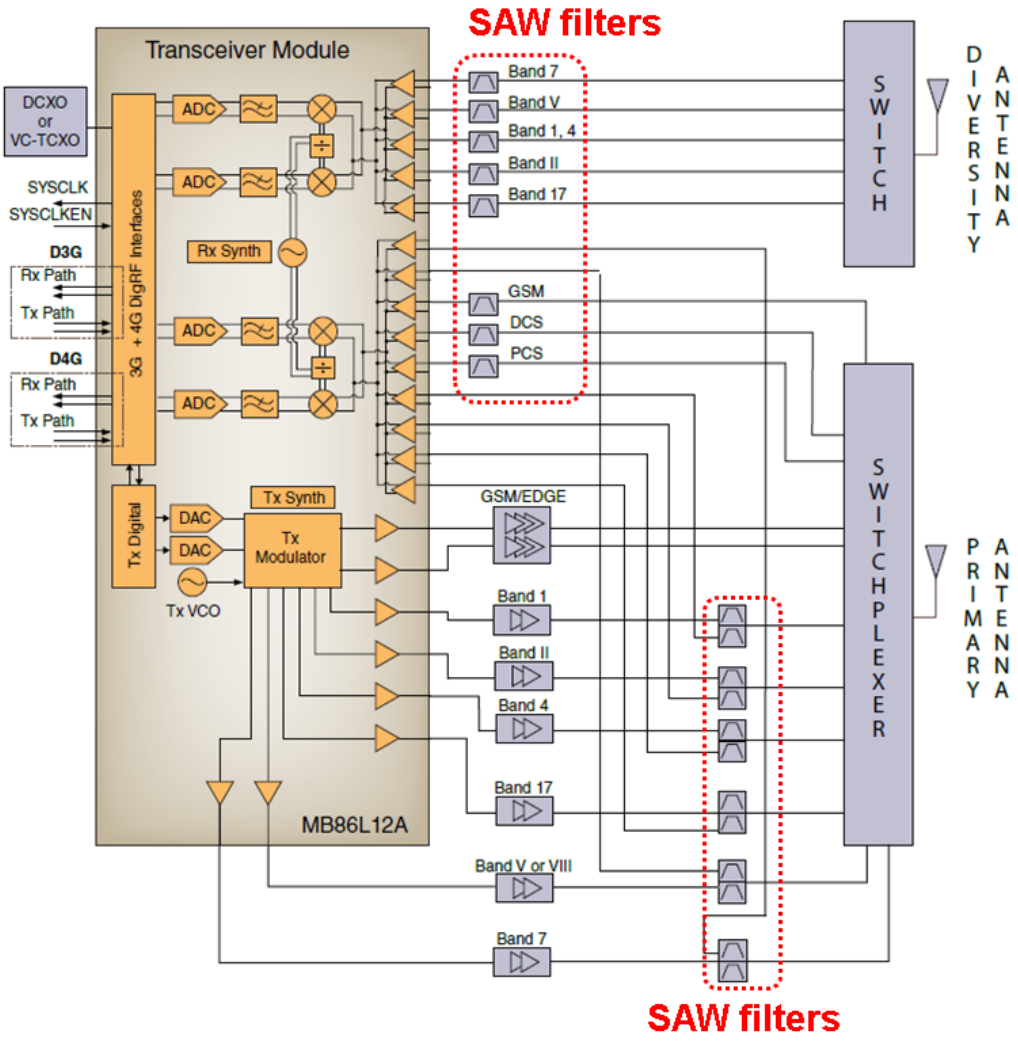

Fig. 1.2: Fujitsu MB86L12A Multi-standard transceiver.

demodulation and detection are nowadays commonly done in the digital domain [8], which is outside the scope of this thesis.

To realize two-way communication, the receiver and transmitter in a mobile phone can be operated at the same time, preferably with one shared antenna [9]. The transmitter signal is very strong and its power may well be $>10^{10}$ times higher than the receiver signal. It may hence saturate the radio receiver, causing malfunction. This is similar to the situation when you go to a nightclub where loud music is played and someone tries to talk to you,

but you cannot understand ("decode") the message due to the loud music. To solve this audio decoding problem, ear plugs which damp and filter the signal can be a solution. Similarly, a RF BPF as in Fig. 1.1 is commonly applied to reject strong interference.

Digital signal processing is at the heart of modern communication systems, as information is generally stored, processed and transferred in the form of digital bits. CMOS IC technology is the mainstream production technology for digital electronics. CMOS has low static power consumption and low propagation delay [10], which plays a role in today's digital communication development [11, 12]. To reduce cost and size, the trend is towards a system on chip (SoC) that integrates both analog and digital circuits on the same chip. Research over the past decades has shown that the circuit blocks in Fig. 1.1 can all be integrated in CMOS technology, except for the antenna and RF BPF. Since an antenna can be shared [9], it is not a main concern for supporting multi-standard.

In a conventional transceiver (i.e. transmitter + receiver) as shown in Fig. 1.2, surface acoustic wave (SAW) filters or bulk acoustic filters wave (BAW) are applied to serve as RF BPFs. SAW filters invented by Edward George Sydney Paige [13] are electromechnical devices widely used in radio frequency applications. A basic SAW filter contains input and output transducers. An electrical input signal is converted to an acoustic wave by the input transducer via the piezoelectric effect. The output transducer receives the acoustic waves and then converts it back to the electrical signal [14, 15]. A BAW filter is also an electromechnical device, exploiting a different acoustic wave principle and are implemented on different substrate materials. Comparing to a SAW filter, a BAW filter can operate at higher frequency, and can be smaller or thinner [16]. In general, SAW filters outperform BAW filters below about 1.5 GHz, while BAW filters tend to have better performance at higher frequencies [17].

As the current mobile phones are multi-standard, a dedicated SAW or BAW filter is required for each standard. A tunable filter solution is highly wanted to decrease the number of required filters. However until now, SAW and BAW filters are not tunable, while they are also bulky compared to a chip (i.e. a few mm^2 per filter) and expensive.

Given the trend to support more and more wireless communication standards, e.g. for 5th generation mobile networks (5G) [18], the demand for even more SAW or BAW filters becomes troublesome. To illustrate this point, Fig. 1.3 shows an open view (i.e. the black

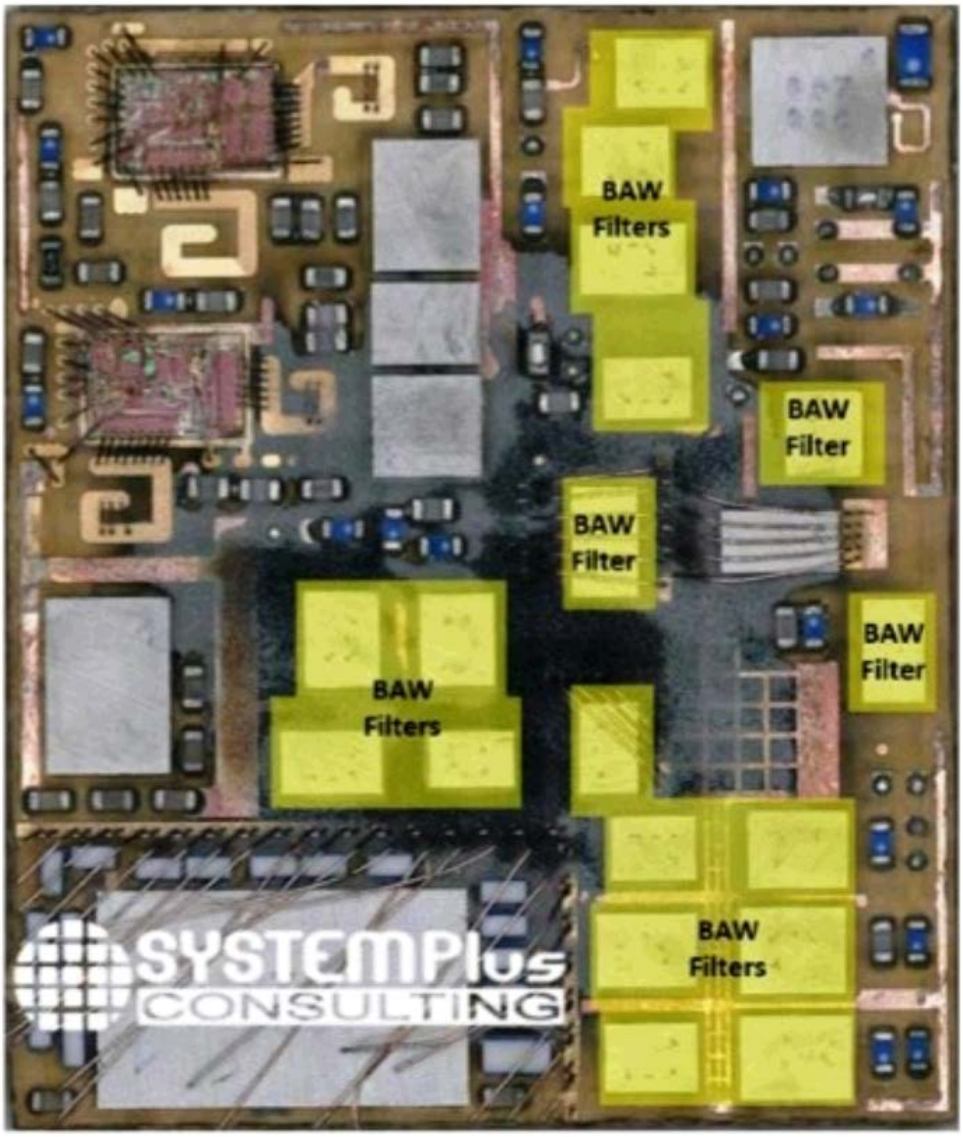

Fig. 1.3: The Broadcom AFE module for iPhoneX (source: System Plus Consulting).

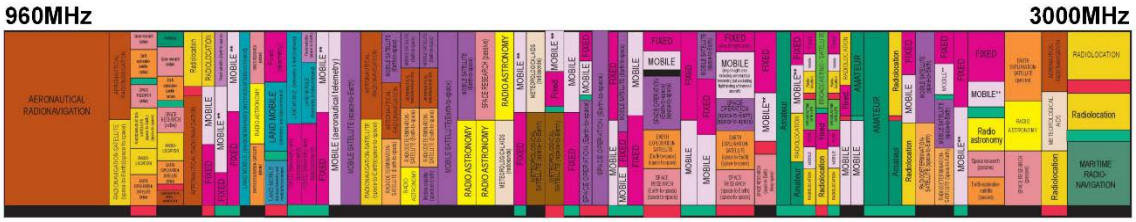

Fig. 1.4: Allocation of the radio spectrum in the US from 900 MHz to 3000 MHz (source: NTIA).

plastic material was removed) of a Broadcom RF AFE module for the iPhoneX. There are 18 off-chip BAW filters and which occupy a substantial part of the area.

The research in this thesis targets to contribute to an increase in the functionality of smartphones and reduction in their cost and size, which makes them affordable for more people. The goal is to innovate in circuit or receiver architecture to realize tunable on-chip RF band-pass filters that can be integrated with digital circuits in CMOS technology to remove the off-chip SAW or BAW filters.

1.3 Challenges

Fig. 1.4 shows an overview of the use of the Radio Frequency (RF) spectrum between 900 MHz and 3000 MHz, as published by the National Telecommunications and Information Administration (NTIA) in USA. Clearly the radio spectrum is very crowded. Still, more data capacity is wanted for instance for the Internet of Things (IoT) [19] and future 5th generation (5G) mobile networks [18]. The sensitivity of a receiver is defined as the minimum signal level that the receiver can detect with acceptable signal-to-noise ratio [8]. The desired signal and many out-of-band (OOB) signals exist simultaneously but are located at different frequencies. Some OOB signals are a lot stronger than the desired signal, and such OOB signals are often called blockers or interferers. Due to non-linearity

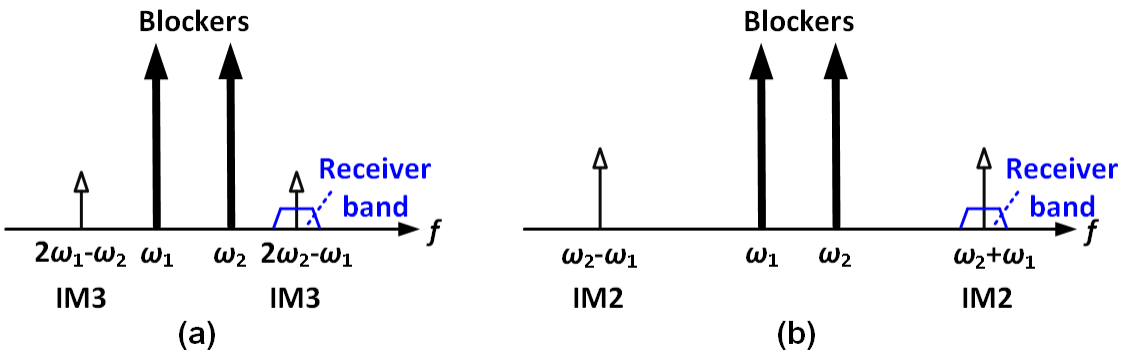

Fig. 1.5: Illustration of (a) IM3 and (b) IM2.

in a receiver, intermodulation distortion can be produced and may fall in the desired receiver frequency band [20]. Usually the main concerns regarding intermodulation are the second-order intermodulation (IM2) and third-order intermodulation (IM3). As shown in Fig. 1.5, the blockers located at ω_1 and ω_2 introduce IM2 at frequencies of $\omega_2 - \omega_1$ and $\omega_2 + \omega_1$, and IM3 at frequencies of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ [20]. The IM2 and IM3 are unwanted, and for modulated interferers often may be assumed randomized so that they will raise the effective noise floor of a receiver when falling in the same frequency band as the wanted signal. If the intermodulation products that fall in the receiver band are too strong, the receiver may become too noisy to detect the weak signal that is desired. When this situation occurs in wireless communication, we can say the receiver is desensitized. The strength of IM2 and IM3 is proportional and quadratically proportional to the strength of the blockers respectively [20]. In a conventional receiver (see Fig. 1.2), SAW filters are applied to greatly suppress the blockers. A SAW filter also produces some intermodulation products, but these are often negligible due to the excellent linearity of SAW filters.

The main challenge of this research is hence to find innovative CMOS solutions to replace the off-chip SAW or BAW filters whilst achieving a very high-linearity to maintain a satisfactory receiver sensitivity, even in the presence of strong interference.

1.4 Thesis Organization

This thesis is organized as follows:

In Chapter 2, the blocking scenarios in the practical mobile communications are discussed. The mechanisms of the receiver desensitization due to coexistence of desired signals and blockers are explained. Based on this analysis, the required linearity of the SAW-less receiver for maintaining satisfactory sensitivity can be determined.

Chapter 3 presents a survey of existing techniques for integrating RF analog front ends in CMOS, such as hybrid transformer-based duplexing, TX leakage cancellation, Q-enhanced LC BPF, g_m-C BPF, and passive switched-RC mixing. Their pros and cons will be discussed and quantified. The N-path filters or mixer-first receiver achieve good linearity, tunable center frequency, and improved performance under CMOS process downscaling, showing the potential for replacing off-chip SAW or BAW filters.

In Chapter 4, a high-linearity receiver architecture combined with N-path filter is introduced, targeting a SAW-less radio receiver in CMOS technology. A new "bottom-plate mixing technique" with switch sharing is proposed to extend the achievable linearity. Aiming for better filter roll-off, a cascade of passive V-V and V-I BPFs is proposed to perform up-front filtering before down-mixing and signal amplification by an active amplifier.

In Chapter 5, a mixer-first receiver enhanced with capacitive positive feedback is proposed to obtain a steeper filter roll-off and enhanced linearity, while achieving low noise figure <3dB. The combination of capacitive positive and negative feedback loops synthesizes complex poles at baseband that are up-converted to RF to offer better selectivity with high-linearity.

In Chapter 6, two ways to measure mixer noise performance, namely the "Y-factor method" and "gain method", are evaluated for characterizing mixers that show unwanted frequency conversions, e.g. image or harmonic mixing. The "Gain method" is selected to measure a receiver with a practical antenna impedance. Also, a system feasibility

demonstration for LTE band 5 is done, applying the new receiver architecture in a practical mobile phone environment.

Chapter 7 concludes and summarizes this thesis. The original contributions will be specified and directions for the future research will be discussed.

CHAPTER 2

Radio Receiver Trends and Design Challenges

2.1 Introduction

In this chapter, the blocking scenarios in a practical mobile phone systems will be discussed in order to have an idea of what we need to deal with. CMOS techniques that address blocking problems will be surveyed in next chapter (Chapter 3).

At the start of the project, the latest mobile communication standard for cellular networks was 4G (5G standardization was in progress). Hence 4G was selected as an example to explain the mechanisms of desensitization due to non-linearity when strong blockers are applied to a receiver.

2.2 LTE-Advanced Overview

Long-Term Evolution (LTE) is a step in moving forward from 3G (3^{rd} generation) mobile telecommunication towards 4G (4^{th} generation). It is a registered trademark owned by ETSI (European Telecommunications Standards Institute). The first discussion for developing LTE can be traced back to 2004 within the 3GPP (3^{rd} Generation Partnership Project) organization. Some objectives for LTE related to data communication are significantly increasing peak data rate, improving spectrum efficiency, lowering radio access network latency, and operating in both paired (FDD) and unpaired (TDD) spectrum [21, 22].

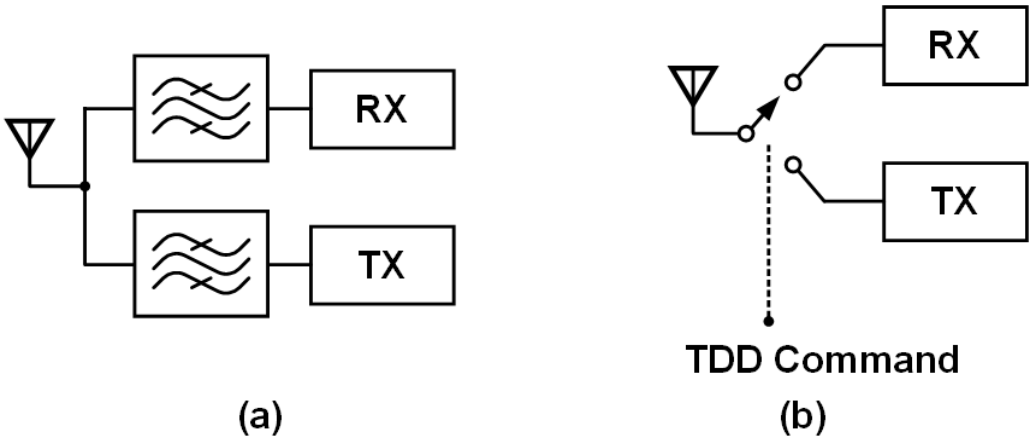

Fig. 2.1: (a) FDD and (b) TDD duplexing [8].

Frequency-division duplexing (FDD) means that a receiver (RX) and transmitter (TX) can operate at the same time but at different frequencies. As shown in Fig. 2.1(a), two BPFs are used to allow antenna sharing between the TX and RX. These BPFs commonly are SAW filters and are called SAW duplexers or duplex filters. In a time-division duplexing (TDD) system (see Fig. 2.1(b)), the RX and TX are connected to an antenna via a switch and operate in different time-slots.

Since the RX and TX work concurrently, FDD systems can have lower latency and higher data rate. FDD occupies two bands at the same time so that its spectrum efficiency is poorer compared to TDD. SAW filters are commonly used in FDD to prevent the corruption of the RX signal due to the presence of very strong TX signals, leading to higher cost for the user equipment, such as mobile phones.

In TDD, the RX and TX do not work at the same time, and if there are no blockers present, SAW filters can be avoided. Unfortunately, a SAW filter is often still required, for instance to deal with coexisting Wi-Fi signals that may be produced at the same time in the same phone. However, the requirements and cost of the SAW filter can be reduced because the Wi-Fi signal is not as strong as the TX signal.

FDD and TDD both have strengths and weaknesses and for a further discussion we refer to [23]. LTE-Advanced FDD and TDD are both applied sometimes even in the same

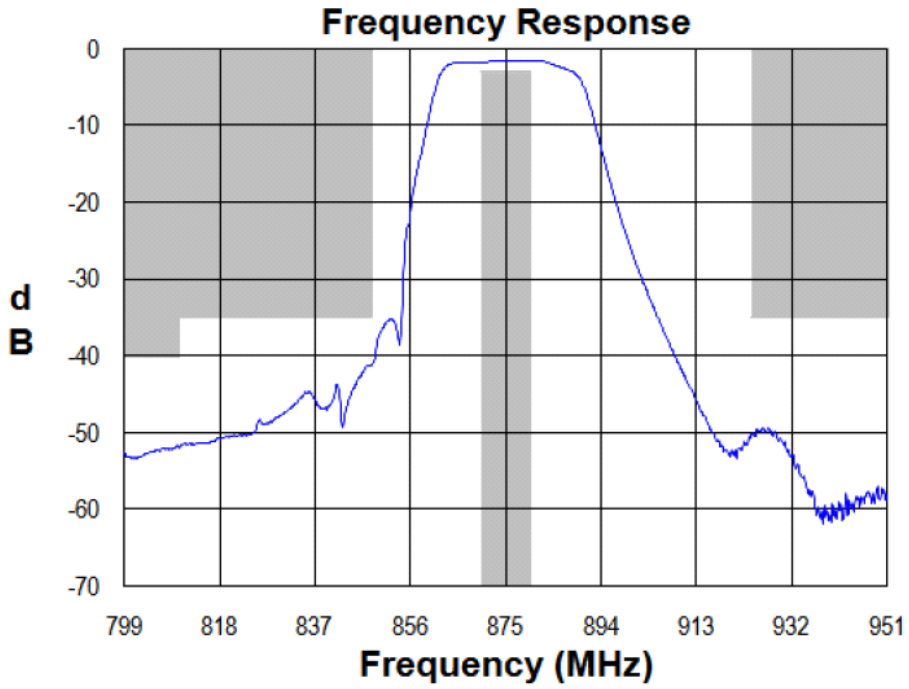

Fig. 2.2: Frequency response of the SAW filter (Part Number 856963[24]) manufactured by TriQuint Semiconductor.

region, e.g. in the North America. Here we focus on FDD which gives the toughest requirements.

A Practical SAW Filter Example

As shown in Fig. 2.1(a), SAW filters are normally applied to serve as BPFs to provide isolation between RX and TX in a FDD system. The frequency response of the SAW filter (Part Number: 856963) manufactured by TriQuint Semiconductor is shown in Fig. 2.2. The center frequency of the SAW filter is 875 MHz and usable bandwidth is 10 MHz (1.2 % of the center frequency). The insertion loss is defined as $10\log(P_{\mathrm{o}}/P_{\mathrm{in}})$ where P_{o} is power out and P_{in} is power in. A low insertion loss of 1.8 dB is achieved in this SAW filter. For the signal outside the passband, it is attenuated by 30 dB when the signal frequency is 30 MHz away from the center frequency. As the offset frequency from the bandpass center increases

from 20 MHz to 40 MHz, the out-of-band signal attenuation is about 30 dB. To achieve the same filter roll-off, a 10^{th} order bandpass filter has to be built.

3GPP uses a system of parallel "Releases" to structure the standards and LTE is specified in Release 8. In order to increase data rate and higher spectral efficiency, LTE was developed further towards LTE-Advanced (Release 10) that fulfills IMT-Advanced (International Mobile Telecommunications-Advanced) 4G requirements. The main new functionalities introduced in LTE-Advanced are Carrier Aggregation (CA) and enhanced use of MIMO techniques [21].

Carrier Aggregation (CA)

To offer users more capacity and faster data speeds, the most straightforward way is to add more bandwidth. The simplest CA scenario is intra-band contiguous CA which aggregates adjacent component carriers in a single frequency band (see Fig. 2.3). However, aggregating contiguous component carriers is not always possible during practical frequency allocation. Intra-band non-contiguous CA can be deployed in case the spectrum allocation is fragmented. It aggregates several separated component carriers in a single frequency band. Finally, Inter-band CA combines multiple component carriers in different frequency bands. It is more complex and more advanced transceivers are required.

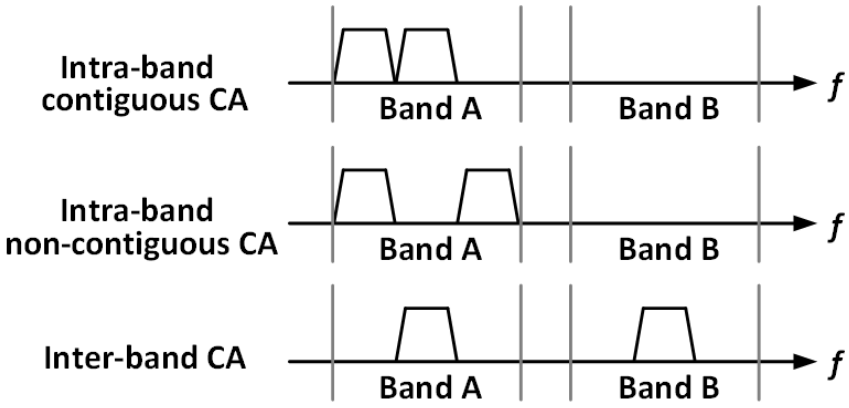

Fig. 2.3: Intra-band contiguous, intra-band non-contiguous and inter-band CA.

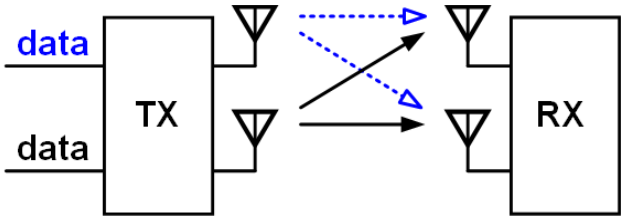

Fig. 2.4: A 2x2 MIMO (Spatial Multiplexing).

Multiple Input Multiple Output (MIMO)

As shown in Fig. 2.4, another important feature of LTE-Advanced is the deployment of MIMO antennas and multiple spatial streams in the same frequency channel for transmission and reception. These data streams can either be different to improve data rate, or be redundant to enhance reliability (exploit "antenna diversity").

As discussed before in Chapter 1 and shown in Fig. 1.2, the diversity antenna in LTE-Advanced is only used for reception. There is about 15-20 dB isolation between the main (primary) antenna and the diversity antenna [25]. The TX signal at this diversity antenna is hence about 15-20 dB smaller than for the main (primary) antenna, so that the linearity requirement for a SAW-less receiver in the diversity antenna path is relaxed.

LTE-Advanced Frequency Bands and Channel BW

In conventional LTE-Advanced receivers, SAW filters are required for both the FDD and TDD modes. FDD has to deal with a stronger blocker which is self-interference produced by the TX signal, while the strongest blocker in TDD mode is often the (weaker) Wi-Fi signal. The receiver designs in this thesis target the worst case, i.e. FDD applications.

The specified receiver channel bandwidths for LTE are 1.4, 3, 5, 10, 15, 20 MHz [21]. Higher channel bandwidth can result in higher data rate, but more spectrum is

occupied. Table 2.1 shows typical FDD frequency bands and their corresponding duplex spacing $f_{TX} - f_{RX}$ (i.e. center-to-center spacing). The required receiver operating frequency coverage is about 700 – 3600 MHz. When a higher receiver channel bandwidth (e.g. 20 MHz) is demanded for a band with smaller $f_{TX} - f_{RX}$ (e.g. 30 MHz), steeper filter roll-off for the BPF in front of the receiver is required.

E-UTRA Operating Band	TX operating band	RX operating band	f_{TX} - f_{RX}
	F_{UL_low} – F_{UL_high}	F_{DL_low} – F_{DL_high}	
1	1920 MHz – 1980 MHz	2110 MHz – 2170 MHz	190 MHz
2	1850 MHz – 1910 MHz	1930 MHz – 1990 MHz	80 MHz.
3	1710 MHz – 1785 MHz	1805 MHz – 1880 MHz	95 MHz.
4	1710 MHz – 1755 MHz	2110 MHz – 2155 MHz	400 MHz
5	824 MHz – 849 MHz	869 MHz – 894MHz	45 MHz
6	830 MHz – 840 MHz	875 MHz – 885 MHz	45 MHz
7	2500 MHz – 2570 MHz	2620 MHz – 2690 MHz	120 MHz
8	880 MHz – 915 MHz	925 MHz – 960 MHz	45 MHz
9	1749.9 MHz – 1784.9 MHz	1844.9 MHz – 1879.9 MHz	95 MHz
10	1710 MHz – 1770 MHz	2110 MHz – 2170 MHz	400 MHz
11	1427.9 MHz – 1447.9 MHz	1475.9 MHz – 1495.9 MHz	48 MHz
12	699 MHz – 716 MHz	729 MHz – 746 MHz	30 MHz
13	777 MHz – 787 MHz	746 MHz – 756 MHz	-31 MHz
14	788 MHz – 798 MHz	758 MHz – 768 MHz	-30 MHz
15	Reserved	Reserved	
16	Reserved	Reserved	
17	704 MHz – 716 MHz	734 MHz – 746 MHz	30 MHz
18	815 MHz – 830 MHz	860 MHz – 875 MHz	45 MHz
19	830 MHz – 845 MHz	875 MHz – 890 MHz	45 MHz
20	832 MHz – 862 MHz	791 MHz – 821 MHz	-41 MHz
21	1447.9 MHz – 1462.9 MHz	1495.9 MHz – 1510.9 MHz	48 MHz
22	3410 MHz – 3490 MHz	3510 MHz – 3590 MHz	100 MHz
23	2000 MHz – 2020 MHz	2180 MHz – 2200 MHz	180 MHz
24	1626.5 MHz – 1660.5 MHz	1525 MHz – 1559 MHz	-101.5 MHz
25	1850 MHz – 1915 MHz	1930 MHz – 1995 MHz	80 MHz.

TABLE 2.1: LTE-Advanced FDD operating bands and their separations [26].

2.3 Noise Performance Requirements

2.3.1 Noise Figure (NF) Requirement of the RX

The noise figure (NF) of a receiver can be defined as the signal-to-noise ratio at the input divided by the signal-to-noise ratio at the output [8]. From link budget equations, the NF requirement of a receiver can be related to sensitivity $P_{\text{sensitivity}}$ and the minimum required SNR for demodulation as:

$$NF = P_{\text{sensitivity}} - 10\log(\text{BW}) + 174[\text{dBm/Hz}] - SNR_{\text{MIN}} \tag{2.1}$$

Assuming there is 50- Ω matching, the noise from 50- Ω source is KT =–174 dBm/Hz. Typical numbers for LTE-Advanced with a channel BW=20 MHz are a required SNR_{MIN} of –1 dB and a reference sensitivity $P_{\text{sensitivity}}$ for QPSK modulation of –94 dBm [21], so that the noise floor is allowed to be –105 dBm and the required NF is 8 dB.

2.3.2 LO Phase Noise Requirement of the RX

Another potential NF degradation mechanism arises from reciprocal mixing. The term reciprocal mixing refers to the situation where a strong OOB blocker effectively acts as an LO-like signal that mixes a phase noise side-band of the (actual) LO to the same frequency as the wanted receiver signal.

The NF limitation related to a continuous-wave (CW) blocker with power P_{b} and a phase noise at the relevant offset frequency $\mathcal{L}_{\omega}\{\Delta\omega\}$ is:

$$NF_{\text{Reciprocal Mixing}} \approx 174[\text{dBm/Hz}] + P_{\text{b}}[\text{dBm}] + \mathcal{L}_{\omega}\{\Delta\omega\}[\text{dBc/Hz}] \tag{2.2}$$

This formula assumes that the blocker power does not exceed the compression point of the RX circuit. An important design trade-off now exists between phase noise of the LO on one hand and blocker attenuation on the other.

For example, to obtain <8 dB NF when there is a P_b=10 dBm without pre-filtering, a very challenging phase noise of ≈–176 dBc/Hz at the relevant offset frequency is required. With the help of a SAW filter that can offer >50 dB blocker rejection, the required clock phase noise at the relevant offset frequency could be greatly relaxed to ≈–126 dBc/Hz.

2.4 Non-linearities

An ideal receiver is linear. However a real receiver has non-linearities, causing the sensitivity degradation. In wireless communications, the input-referred third-order intercept point (IIP3), input-referred second-order intercept point (IIP2) and –1-dB gain compression point are popular performance metrics to characterize the non-linearities of practical circuits. Note that the concept of intercept points is based on the assumption of a weakly nonlinear circuit or system [20].

2.4.1 IIP3, IIP2 and Gain Compression

Assuming the input V_{in} is a combination of two CW signals (tones): $A_1 \cdot \cos(\omega_1 t) + A_2 \cdot \cos(\omega_2 t)$, and the output can be expressed by power series which is [20]:

$$V_{\text{out}} = a_1 \cdot V_{\text{in}} + a_2 \cdot V_{\text{in}}^2 + a_3 \cdot V_{\text{in}}^3 + \cdots \tag{2.3}$$

IIP3

The third order intermodulation products P_{IIM3} that are proportional to the input power are $\frac{3a_3A_1^2A_2}{4} \cdot \cos(2\omega_1 - \omega_2)t$ and $\frac{3a_3A_2^2A_1}{4} \cdot \cos(2\omega_2 - \omega_1)t$. IIP3 is the extrapolated point where P_{IIM3} is equal to input power. Note that IIP3 is a mathematical concept, because the weakly nonlinear assumption does not hold for such high power. IIP3 can be expressed as:

P_{IIM3} is located at $2\omega_2 - \omega_1$: $\qquad \text{IIP3} = P_2 + 0.5(P_1 - P_{\text{IIM3}})$ (2.4)

P_{IIM3} is located at $2\omega_1 - \omega_2$: $\mathrm{IIP3} = P_1 + 0.5(P_2 - P_{\mathrm{IIM3}})$ (2.5)

When two tones are equal ($P_1 = P_2 = P_{\mathrm{in}}$), the P_{IIM3} can be written as [8]:

$$\mathrm{IIP3} = P_{\mathrm{in}} + 0.5(P_{\mathrm{in}} - P_{\mathrm{IIM3}}) \quad (2.6)$$

IIP2

When V_{in} is two-tone with equal amplitude A, $a_2 \cdot V_{\mathrm{in}}^2$ in (2.3) can be derived as $a_2 \cdot V_{\mathrm{in}}^2 = a_2 \cdot A^2[1 + \cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t + 0.5\cos(2\omega_1)t + 0.5\cos(2\omega_2)t]$.

The IM2 products at $\omega_1 - \omega_2$ and $\omega_1 + \omega_2$, including the DC offset are expressed as $a_2 \cdot A^2[1 + \cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t]$. P_{IIM2} is also proportional to the input power and IIP2 is the extrapolated point where P_{IIM2} is equal to input power. IIP2 can be expressed as [27]:

$$\mathrm{IIP2} = 2P_{\mathrm{in}} - P_{\mathrm{IIM2}} \quad (2.7)$$

Two-tone test for IIP2 and IIP3 estimation is commonly implemented to quantify the non-linearities of a practical system or circuit. However, a blocker such as the TX signal might be a modulated signal in a real mobile system. The desensitization of a receiver due to modulated/unmodulated blockers can be linked to IIP2/IIP3 and will be discussed in the following sections.

Gain Compression Point

An alternative, but less accurate way to characterize non-linearity is –1-dB gain compression point (see Fig. 2.5). In general, as the input signal increases, the gain of a practical circuit or system decreases. The non-linearity can be viewed as the gain variation.

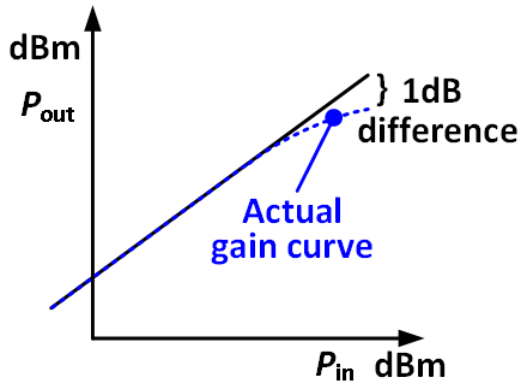

Fig. 2.5. Illustration of gain compression.

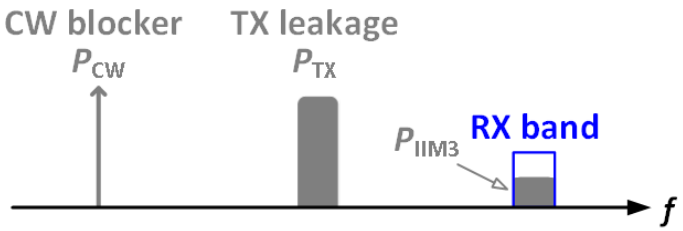

Fig. 2.6: CW blocker and modulated TX leakage are spaced such that 3rd order intermodulation falls in RX band.

2.4.2 3rd order Intermodulation Due to TX Leakage and OOB Blocking

As specified in [21], LTE-Advanced requires to tolerate a −15 dBm out-of-band CW blocker $P_{CW,OOB}$ at a certain offset frequency from the desired band. When the $P_{CW,OOB}$ is located at two times the duplex frequency from the RX band (see Fig. 2.6), and a modulated TX leakage P_{TX} (up to +23 dBm [21]) is present at the duplex frequency, IM3 falls on top of the RX band. The 3rd order intermodulation P_{IIM3} will then directly interfere with the

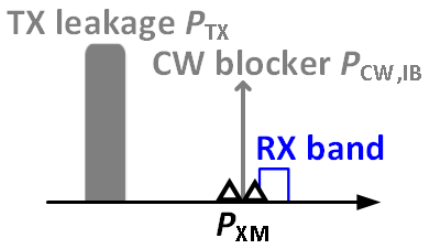

Fig. 2.7: Cross modulation due to TX leakage and in-band blocking.

RX signal. Using Eqn. (2.4) and considering $P_2 = P_{\text{TX}}$, $P_1 = P_{\text{CW,OOB}}$, the required IIP3 to satisfy a given P_{IIM3} can be written as:

$$\text{IIP3}_{\text{req,IM}} = \frac{P_{\text{cw,OOB}} + 2P_{\text{TX}} - P_{\text{IIM3}}}{2} \tag{2.8}$$

If we assume for simplicity that P_{IIM3} is roughly equal to the total thermal noise in the band of interest (i.e. P_{IIM3} =–174+$10log(\text{BW})$) when channel bandwidth BW=20 MHz, the $P_{\text{cw,OOB}}$ and P_{TX} are at maximum, we find $\text{IIP3}_{\text{req,IM}} = (-15 + 2 * 23 - (-101))/2 = +66$ dBm. Without the up-front SAW filter or another very linear passive filter, it seems unlikely that a receiver can achieve such high IIP3 (the best published IIP3 results for CMOS receivers was about +30 dBm at the start of the project).

2.4.3 Cross Modulation Due to TX Leakage and In-Band Blocking

Considering input V_{in} is a combination of an in-band CW blocker (or jammer) $A_{\text{j}} \cdot \cos(\omega_{\text{j}} t)$ and a TX leakage $A_{\text{TX}} \cdot \cos(\omega_{\text{TX}} t)$. When V_{in} is present at the input of a RX having 3rd order non-linearity and using Eqn. (2.3), the output signal at ω_{j} is $[a_1 \cdot A_{\text{j}} + \frac{3}{4} a_3 \cdot A_{\text{j}}^3 + \frac{3}{2} a_3 \cdot A_{\text{j}} A_{\text{TX}}^2] \cdot \cos(\omega_{\text{j}} t)$ [8]. As the amplitude of TX leakage is modulated (i.e. A_{TX} is a function of time not constant), a part of modulated TX is transferred and located close to

CW blocker frequency ω_j as shown in Fig. 2.7. The resulting cross modulation product P_{XM} may fall in the desired frequency to contaminate the RX band. It can be related to an IIP3 [28, 29] as:

$$\text{IIP3}_{\text{req,XM}} = \frac{P_{\text{CW,IB}} + 2P_{\text{TX}} - P_{\text{XM}} - 5}{2} \tag{2.9}$$

Where $P_{\text{CW,IB}}$ is the power of the in-band CW blocker, and the in-band blocker is −56 to −44 dBm in LTE-Advanced [21]. P_{TX} is the TX leakage (up to +23 dBm [21]) while the last term (=5 dB) is added to account for the modulated nature of the TX [28].

Assuming the P_{XM} is as low as the total thermal noise in the band of interest (i.e. $P_{\text{XM}} = -174 + 10log(\text{BW})$) when channel bandwidth BW=20 MHz, the $P_{\text{cw,IB}}$ and P_{TX} are at maximum, we find $\text{IIP3}_{\text{req,XM}} = (-44 + 2 * 23 - (-101))/2 = +52$ dBm.

2.4.4 2nd order Intermodulation Due to "Self-Mixing" of Modulated TX Leakage

In general, the 2nd non-linearity of a differential receiver is due to mismatch in both paths. When a modulated TX leakage P_{TX} is present at the input of a practical RX, the RX band will be contaminated by 2nd order intermodulation P_{IIM2} due to self-mixing of modulated TX [30].

For better understanding of 2nd order non-linearity due to "self-mixing", we first consider the two-tone case. As shown in Fig. 2.8(a), the strong OOB RF signals $A \cdot \cos(\omega_1 t)$ and $A \cdot \cos(\omega_2 t)$ may couple to the LO port, resulting RF to LO leakage: $\alpha A \cdot \cos(\omega_1 t)$ and $\alpha A \cdot \cos(\omega_2 t)$ where α<1. The self-mixing components located BB frequencies $f_1 - f_2$, $f_2 - f_1$ are induced and proportional to A^2. When there is no mismatch, these self-mixing components are common mode signals and cancelled at the differential output. In reality, mismatch exists and the 2nd order non-linearity is generated at BB to degrade the performance of a mixer circuit.

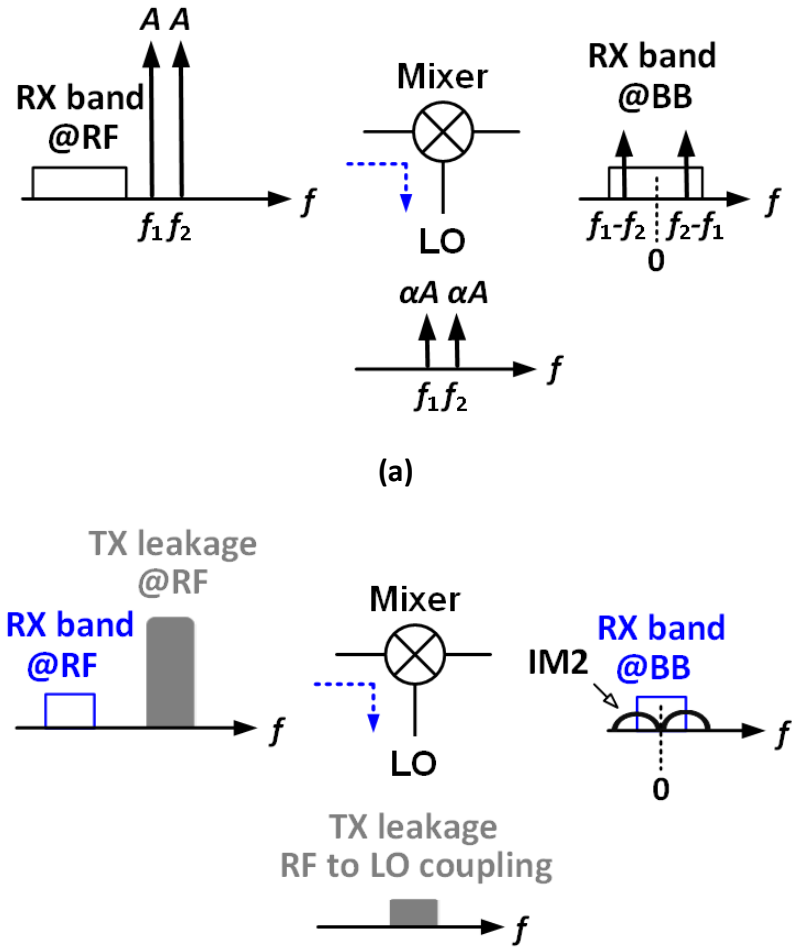

Fig. 2.8: 2nd order intermodulation due to "self-mixing" of (a) CW tones and (b) a modulated TX signal [30].

When TX is a modulated signal as shown in Fig. 2.8(b), the requirement for out-of-band IIP2 to keep the P_{IIM2} below a certain level can be determined by using the following equation [30, 31]:

$$\mathrm{IIP2}_{\mathrm{req,IM}} = 2P_{\mathrm{TX}} - P_{\mathrm{IIM2}} + C(N) \tag{2.10}$$

Where correction factor $C(N)$ depends on the number of data channels N in TX signal [30, 31]. For 1 data channel case, the correction factor is about −11 dB [31] and used for calculation. More detailed discussion for $C(N)$ could be found in [30, 31].

Assuming the P_{IIM2} is as low as the total thermal noise in the band of interest (i.e. P_{IIM2} =−174+10log(BW)) when channel bandwidth BW =20 MHz and the P_{TX} is at maximum (+23 dBm [21]), we find $\mathrm{IIP2}_{\mathrm{req,IM}} = 2 * 23 - (-101) - 11 = +136$ dBm, which is extremely challenging.

2.5 Conclusions

The development of LTE-Advanced results in an evolution of wireless communication towards higher data rate and lower latency. FDD and TDD duplexing techniques are both applied in today's mobile communication systems. Compared to TDD, the RX for FDD suffers from stronger TX blocker signals because the RX and TX work at the same time. The strong TX signal is up to +23 dBm in current LTE-Advanced. We derived linearity requirements assuming we want to keep the intermodulation product lower than the total thermal noise in the band of interest. For a SAW-less receiver, we find the following required intercept points for the main antenna path: IIP3 > +66 dBm and IIP2 > +136 dBm, which are extremely challenging.

There is an inherent ≈15 dB isolation between the main transceiver and the diversity receiver, resulting in relaxed IIP3 (> +44 dBm) and IIP2 (> +106 dBm) requirements for a SAW-less diversity receiver design.

The noise figure of a receiver must be kept low enough to achieve the required sensitivity. A SAW filter has 2-3 dB loss [24], causing 2-3 dB noise figure degradation. A SAW-less receiver design can avoid this loss, but the required linearity is challenging.

As a SAW filter attenuates blockers, it not only greatly relaxes the receiver linearity but also the LO phase noise requirement. A SAW-less solution hence may ask for very strict phase noise requirements of the local oscillator.

SAW or BAW filters occupy a large area in a mobile phone (see Fig. 1.3). Integrating these filters in CMOS technology is attractive but also very challenging. In the next chapter, a comprehensive survey of related research from the past years will be given, to see what will be possible solutions that we can explore further.

CHAPTER 3

Survey of Existing Techniques for Integrated Blocker Tolerant Front End

In wireless receivers, sensitivity is the minimum power at the input to guarantee the specified signal to noise ratio (SNR). As discussed in Chapter 2, the strong modulated TX leakage, as well as OOB and in-band CW blockers, may introduce intermodulation and/or cross modulation that fall in the RX band, all deteriorating the sensitivity. Aiming for removing (off-chip) SAW or BAW filters, various techniques have been proposed to deal with OOB blockers in past years. Integrated hybrid transformer-based duplexer designs [32-34] provide high TX-RX isolation to greatly relax RX linearity requirement. Cancellation-based front-end architectures [35] tap a portion of the TX-signal to perform subtraction at the RX, relaxing the requirements of front-end filters. Integrated tunable N-path filters [36-39] and mixer-first receivers [40-42] suppress OOB signals with passive switched-RC mixing circuits, showing some promising results. In the following sections, these existing blocker tolerant RF front-end design techniques will be discussed. The key focus will be on techniques that allow for realizing high IIP3, IIP2 and gain compression point in order to retain satisfactory sensitivity on CMOS technology.

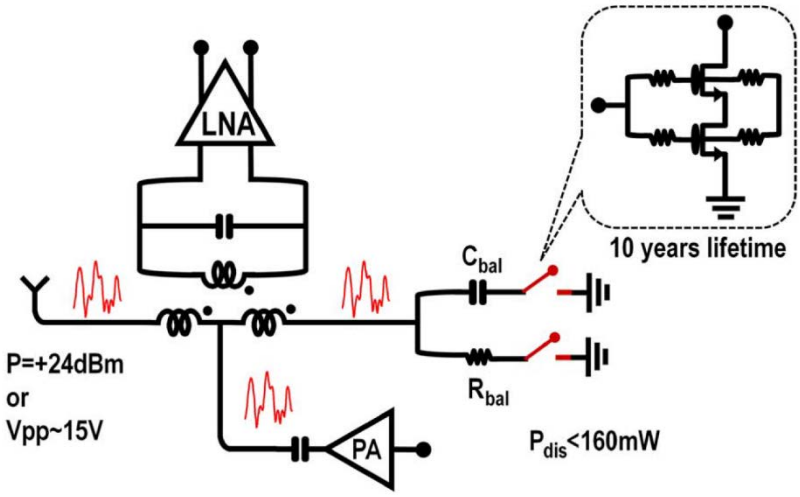

Fig. 3.1: Schematic of a transformer-based duplexer integrated in CMOS [33, 43].

3.1 Hybrid Transformer-Based Duplexer

The hybrid transformer has been used in traditional wireline systems for telephony [44, 45]. The concept offers isolation between the earpiece and microphone in a telephone handset to allow for simultaneous talking and listening, i.e. 2-directional or "duplex" communication. In recent years, it gained interest for on-chip duplexer design to provide TX-RX isolation at RF for mobile communications [32, 34, 43, 46].

The idea of using a hybrid transformer to serve as an RF duplexer had been demonstrated in [47] where off-chip discrete components are adopted. Targeting for integration in silicon, a duplexer based on an on-chip transformer was proposed in [33, 43]. The implementation in [33, 43] uses a differential LNA at the RX port which is shown in Fig. 3.1. Ideally the LNA did not see the "differential" TX-signal because the TX signal is presented as a common-mode signal at the input of LNA. However, if the PA operates at full power, compression of the LNA may still occur due to the presence of large common-mode signal.

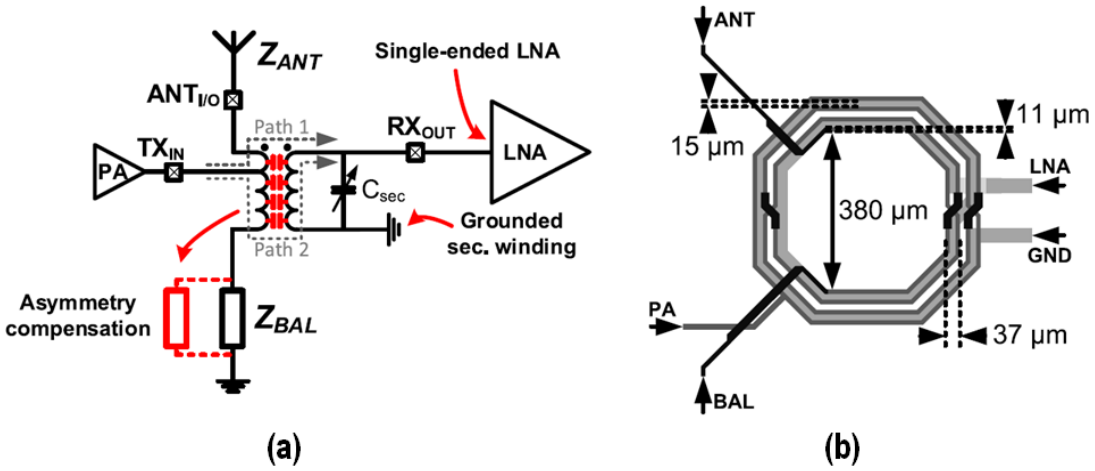

Fig. 3.2: (a) Schematic of the single-ended transformer-based duplexer, and (b) the transformer layout [34].

To reduce the large common-mode issue, a single-ended hybrid transformer topology is proposed in [34] and one side of the secondary winding is connected to ground. As shown in Fig. 3.2, the TX signal leaks to the RX port through ”Path 1” at the antenna side. The TX signal is also inverted in the current domain as indicated in ”Path 2”. By adjusting the balance network Z_{BAL}, the TX leakage in these two paths are cancelled out due to destructive interference at the RX port. The single-ended hybrid transformer duplexer [32, 34] achieved very promising performance of >50dB TX-RX isolation, >+70 dBm IIP3 and moderate insertion loss of about 4 dB (for both RX and TX). However, it has a limited operating frequency range of a few hundred MHz. Moreover, the antenna impedance varies with user interaction in practical scenarios. It is very critical to compensate for this variation and further investigations are required [48].

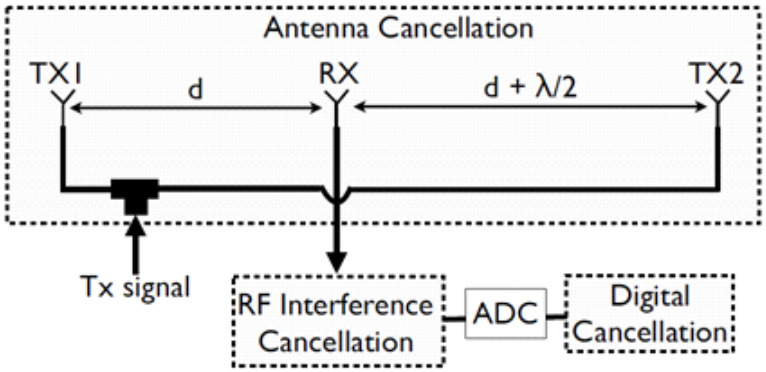

Fig. 3.3: Antenna cancellation [49].

3.2 TX Leakage Cancellation

3.2.1 Antenna Cancellation

As shown in Fig. 3.3 [49], antenna cancellation can also be applied to realize in-band full-duplex, where two TX antennas and one RX antenna are involved. For each wave length λ, a null position exists where the signals of both TX-antennas cancel. However, this involves change of the position of antennas for different frequency of operation. Moreover, multiple antennas are required and the achievable cancellation is sensitive to the EM environment.

3.2.2 Passive TX Leakage Cancellation

A block diagram of a passive TX leakage cancellation system is shown in Fig. 3.4 [50]. The passive circuitry may be applied to suppress the TX leakage. However, both LC-based and transmission-line-based [51] cancellation paths are not very attractive for integration in silicon due to their large size compared to other components.

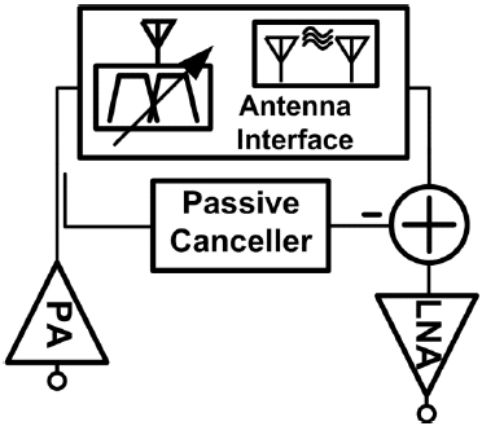

Fig. 3.4: Passive TX leakage cancellation [50].

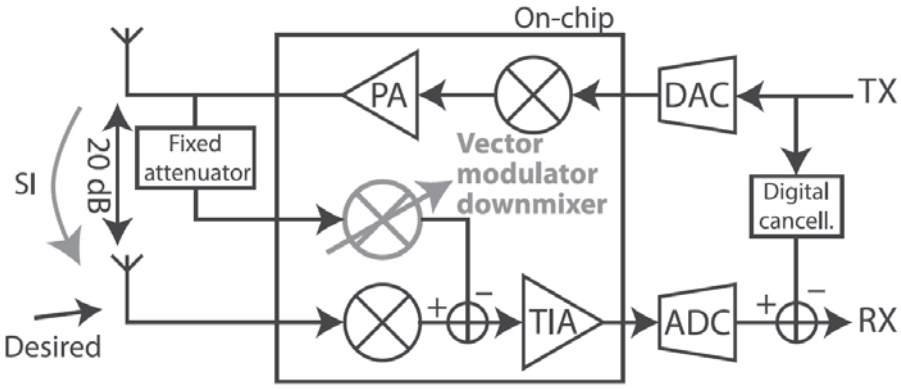

Fig. 3.5: an integrated Passive TX leakage cancellation for in-band full duplex wireless communication [52].

Targeting for a highly linear on-chip passive TX leakage canceller in CMOS, an integrated self-interference (SI) cancelling receiver for in-band full duplex (FD) wireless communication is proposed (see Fig. 3.5) in [52]. A copy of attenuated TX signal with tunable phase shift is down-converted and the TX leakage cancellation is performed at

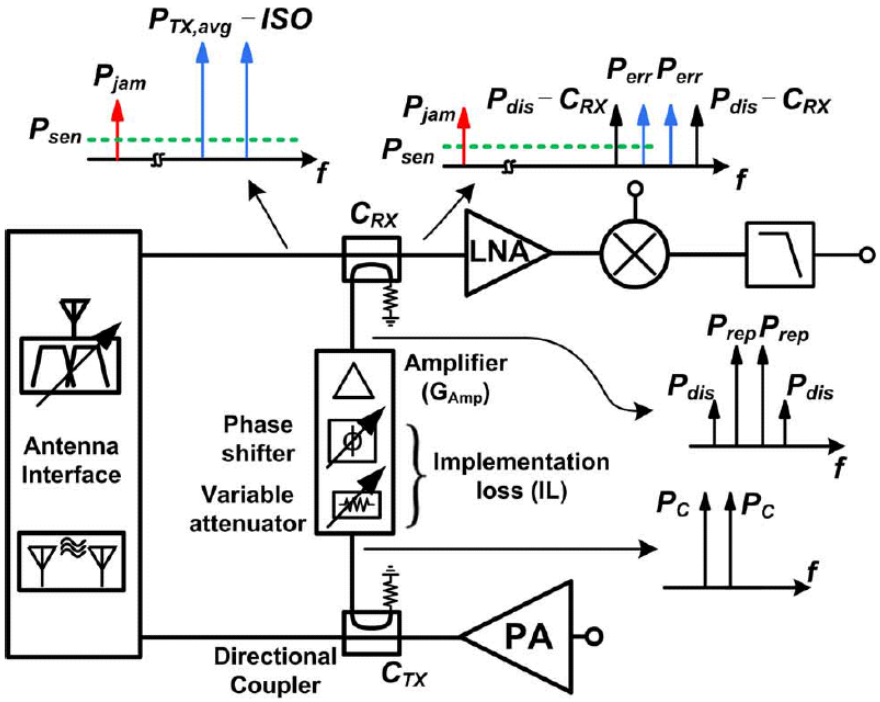

Fig. 3.6: An example of active TX leakage cancellation [35].

analog baseband, prior to the signal amplification. The in-band SI cancelling RX design in [52] is based on switched-resistor mixing architecture, resulting considerable noise injection to BB (i.e. the achieved NF is about 10 dB).

3.2.3 Active TX Leakage Cancellation

An example of an active TX leakage canceller is shown in Fig. 3.6. Such cancellers can be reconfigurable and can be integrated in CMOS technology [35, 53-55]. A portion of the TX signal is coupled from the power amplifier (PA) output by using a directional coupler. The phase and amplitude of a replica of the TX signal are tuned, and the subtraction is conducted at the RX input. A key challenge of active TX leakage cancellation designs is the performance degradation due to non-linearity and noise caused by the active cancellation circuits. Also, the supply voltage is around 1 V in current CMOS technologies,

which is normally not enough to handle the very large TX leakage voltage swings associated with commonly used maximum power levels in excess of +20 dBm.

3.3 Q-enhanced LC BPF

Integrated LC filters possess significant insertion loss, because the quality factor of on-chip inductors is poor due to metal resistances and other loss mechanisms [56, 57]. To compensate for this loss, Q-enhancement techniques exploiting a negative resistance have been proposed [56, 57]. Such LC filters have several drawbacks such as large area occupation, limited tuning range and most notably poor dynamic range due to the nonlinearity and noise added by the negative resistance circuits. A more detailed discussion can be found in [58].

3.4 g_m-C BPF

The basic building block of a g_m-C filter is an integrator composed of a transconductance g_m and a load capacitor C. The g_m-C filter can operate at RF frequencies [59, 60], but the achievable dynamic range is limited due to active g_m cells introducing noise and distortion.

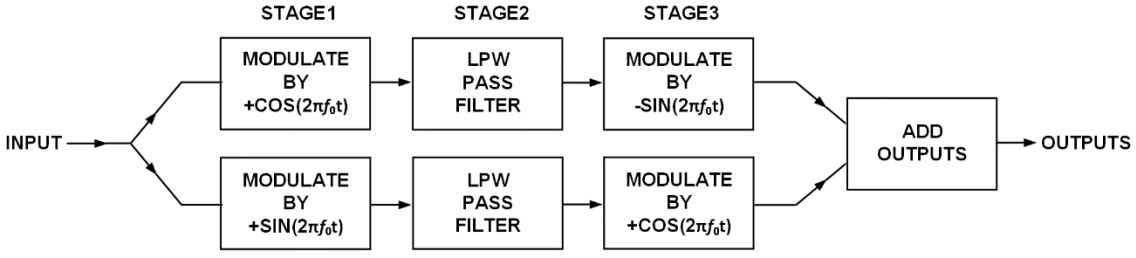

Fig. 3.7: a narrow bandpass filter using modulation [61].

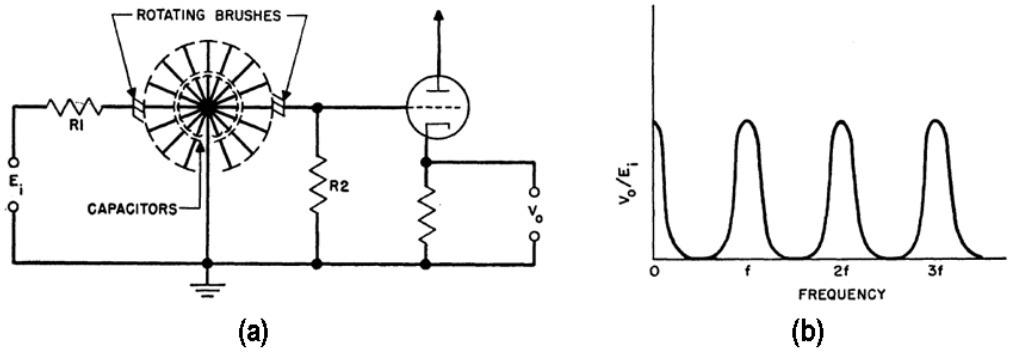

Fig. 3.8: (a) The electromechanical circuit and its (b) "comb filter" frequency response [62].

3.5 N-Path Filter and Mixer-First Receiver

3.5.1 General Introduction

N-path filters and mixer-first receivers exploit time-variant circuits. This allows for realizing a frequency-shifted transfer function, and idea can be traced back to a paper as early as 1947 [61]. N. F. Barber proposed the concept of a narrow bandpass filter using modulation [61] as shown in Fig. 3.7. In later year, Busignies and Dishal proposed an electromechanical circuit [62] (see Fig. 3.8) that produces a "comb passband filter" (i.e. bandpass filter) type of frequency response. A capacitor array rotates mechanically at a frequency that determines the passband center-frequency. The input is down-converted on each capacitor, then it is up-converted after half a cycle later.

In literature, this concept is sometimes also called ''Commutated Network'' [63], Sampled-Data filter [64], Frequency-Translated Filter [64] or N-path filter [65], the term that we will use here. Fig. 3.9(a) shows the general model of an N-path filter, as proposed by Franks and Sandberg in 1960 [65]. The frequency translation circuit can shift a specified impedance to a well-defined center frequency. An N-path BPF can be obtained by conducting frequency translation of a LPF (see Fig. 3.9(b)), while the N-path notch can be obtained by conducting frequency translation of a HPF (see Fig. 3.9(c)).

In the discussion so far, two switches are required for up- and down-conversions respectively in a single frequency translation path. This can be simplified to one switch if the frequency of the p(t) and q(t) clocks is the same. When the clocks p[t] and q[t] are identical, the output is available between the source resistor R and a shared switch which was presented by Smith in 1953 [63] (see Fig. 3.10). Moreover, the −3 dB bandwidth of the filter is predicted as $1/\pi NRC$ [63], where NC is the total commuted capacitors.

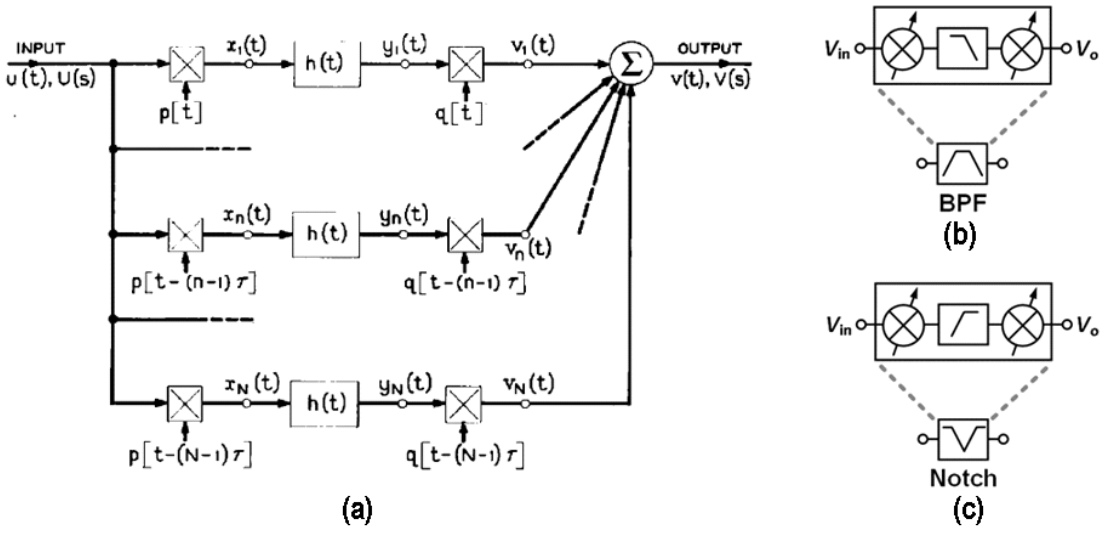

Fig. 3.9: (a) The N-path filter configuration [65], (b) N-path BPF and (c) notch filter [66].

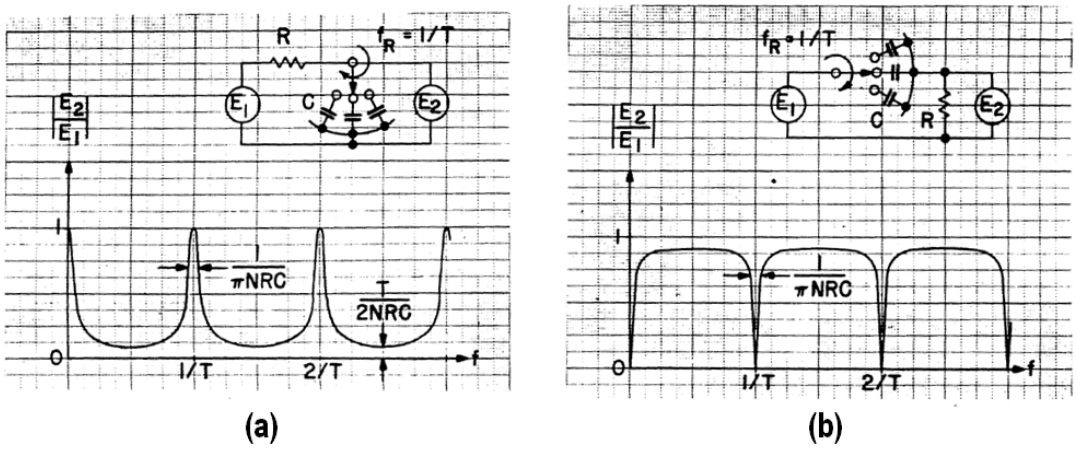

Fig. 3.10: (a) Commutated bandpass filter, and (b) band-stop [63].

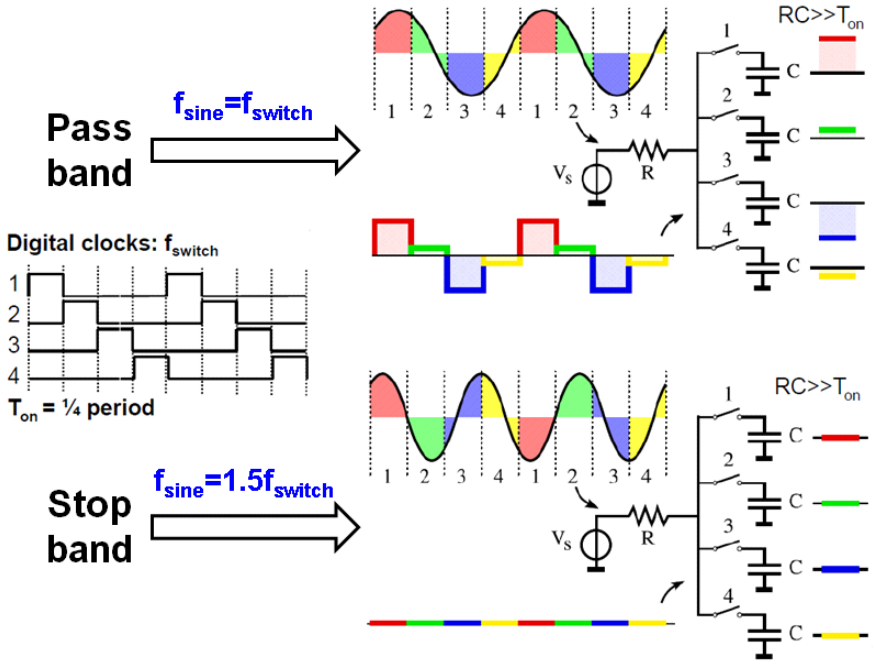

Fig. 3.11: Time domain waveform of a 4-path bandpass filter for pass band $f_{\text{sine}} = f_{\text{switch}}$ and stop band $f_{\text{sine}} = 1.5 f_{\text{switch}}$ [67].

3.5.2 Basics of the N-Path Filter

To intuitively understand the N-path filter concept, Fig. 3.11 shows the time domain waveform for pass band and stop band respectively. Consider a 4-path filter driven by 25% duty-cycle non-overlapping clocks and $RC >> T_{on}$, where T_{on} is on-time of the switch. After many clock periods of settling and assuming that the RF input frequency f_{sine} equals the switching frequency f_{switch}, a staircase approximation of the RF input results at the RF-side of the switches, while the (approximate) staircase values are stored on the capacitors. The signal source now "sees" a relative high impedance which passes the filter. If the RF input frequency is OOB, e.g. at $f_{\text{sine}} = 1.5 f_{\text{switch}}$, the average of the input signal down-converted on each of the capacitors is almost zero. The signal source now sees a very low impedance and the source signal will largely be shortened to ground. Note that more clock phases (higher N) can result in a smoother waveform and higher input impedance for the passband signal. In contrast to a SAW filter, that lacks programmability, the passband frequency of the N-path filter is exactly the same as the switching frequency f_{switch}, which can be programmed flexibly.

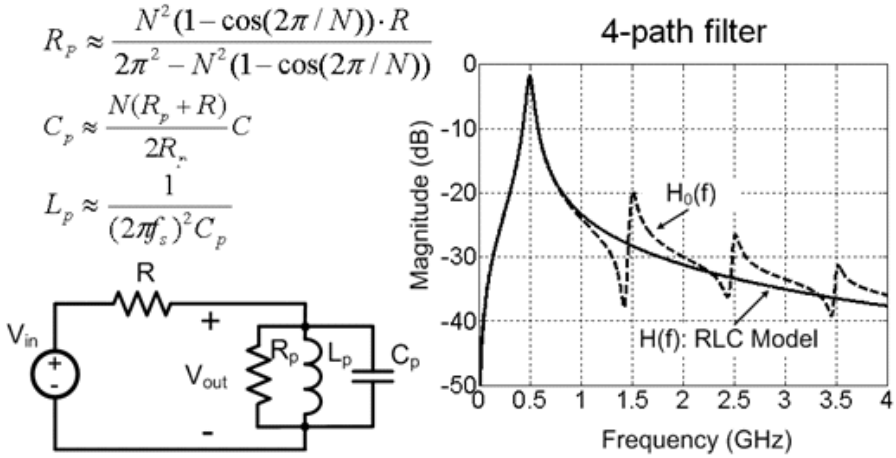

Fig. 3.12: Simulated transfer function of a 4-path filter (dash line) and it RLC approximation model (solid line) [36].

In [36], it is shown that the transfer function of an N-path filter resembles that of a high-Q LC tank around f_{switch} (see Fig. 3.12). The equations for equivalent R_{p}, L_{p} and C_{p} are also derived to quantify this similarity and shown in the figure.

Moore's law predicts the evolution of the complexity per area for CMOS integrated circuit (IC) technology. Downscaling brings lower parasitic capacitance, faster digital clocking circuits with the same power consumption budget and lower on-resistance of the MOS transistors because of their shorter channel length. Due to the smaller feature sizes, a higher capacitance density for high-linearity metal-oxide-metal (MOM) capacitors is also available. These developments make N-path filter implementations more attractive. An early N-path filter had been integrated in CMOS technology in 1978 [68]. It is 4-path implementation with BPF center frequency of 10 kHz. Recent N-path filters operate at higher center frequencies beyond 1 GHz [36] that shows the potential in radio applications.

3.5.3 Basics of the Mixer-First Receiver and the Comparison with N-Path Filter

In recent years, RF front-ends deploying passive switched-RC N-path filtering techniques for blocker signal rejection showed promising results. These circuits are integrated in CMOS technology, their passband is widely tunable and well-defined. Moreover, high compression point (>+10 dBm) [69, 70], and good linearity of 20-30 dBm OOB IIP3 [38, 71] have been demonstrated.

As illustrated in Fig. 3.13(a), the passive switched RC mixing circuit can be an N-path filter when the RF voltage V_{RF} serves as output. In wideband receiver designs, the N-path filter is often placed before a high bandwidth RF low-noise amplifier (LNA) [38, 72]. In case the down-converted BB signal V_{BB} is used as the output of the passive switched-RC mixing circuit and connected to the BB amplifier, this becomes a mixer-first receiver as shown in Fig. 3.13(b).

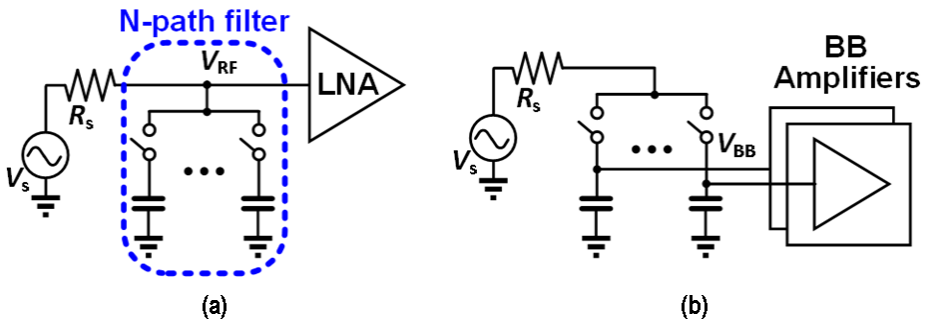

Fig. 3.13: (a) a RX with an N-path filter at RF input, and (b) a mixer-first RX.

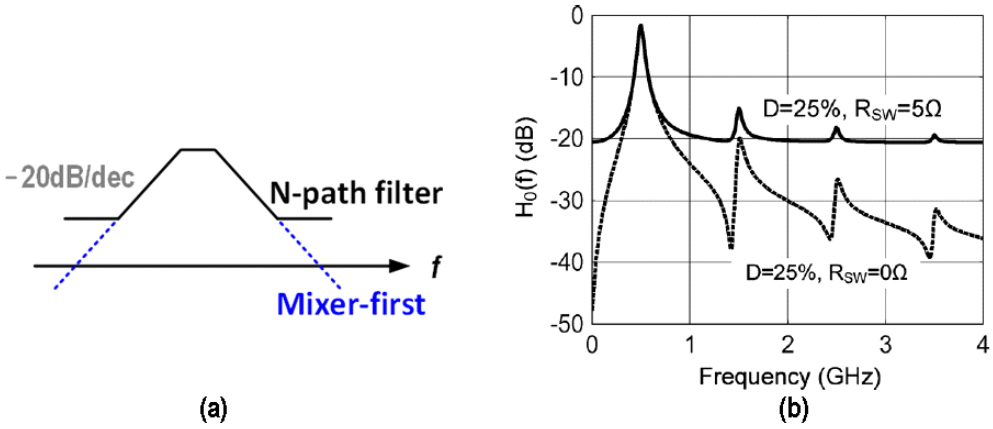

Fig. 3.14: (a) RF filtering profile before the active amplifier for the conventional N-path filter and mixer-first receiver, and (b) the reduction of OOB rejection due to mixer switch resistance in the conventional N-path filter [36].

One of the early development of mixer-first receiver removes RF LNA to reduce power consumption [40]. To achieve the same noise performance, the low frequency BB amplifier possibly consumes less power than RF LNA. The input-referred noise of an amplifier can be decreased by increasing its transconductance g_m. Compared to the RF

LNA, the BB amplifier requires much lower (e.g. 10-100 times lower) bandwidth. To achieve the same noise performance (i.e. roughly the same g_m) with lower power consumption, the size (i.e. the W/L ratio) of the BB amplifier can be much larger than RF LNA due to its low bandwidth requirement. However 1/f noise now becomes a problem.

Fig. 3.14(a) shows the related RF filtering profile before the active amplifier. For far OOB frequencies, the on-resistance R_{sw} of mixer switch limits OOB rejection to $R_{\mathrm{sw}}/(R_{\mathrm{s}} + R_{\mathrm{sw}})$, where R_{s} is the antenna source resistance. Non-ideal clock duty cycle causes the reduction of the maximum OOB rejection as well [36]. A detailed analysis of the effects of on-resistance and non-ideal clock duty cycle in an N-path filter is presented in [36], Fig. 3.14(b) shows the reduced maximum OOB rejection by transfer function simulation [36]. In the mixer-first receiver, the down converted BB voltage V_{BB} sees the capacitor (as shown in Fig. 3.13(b)) that has almost zero far OOB impedance, so that the OOB rejection is not limited by R_{sw} and non-ideal clock duty cycle.

Another notable technique which is enabled by zero-IF mixing that produces I/Q baseband voltages deploys “complex frequency translated feedback” as proposed by Andrews and Molnar [71, 73]. This technique provides input matching to a practical antenna with a complex impedance, while the noise figure penalty is minor.

3.5.4 Selectivity Enhancement of a N-Path Filter

A SAW filter can offer very high selectivity, see e.g. the 8$^{\mathrm{th}}$-order RF-BPF in [74]. However, a typical N-path filter or mixer-first receiver up-converts only a first-order BB LPF to second order BPF with one pair of complex poles (i.e. 2$^{\mathrm{nd}}$-order BPF) for OOB rejection.

Nowadays, the spectrum had been already occupied by many applications (see Fig. 1.4). The spectrum will be more crowded in the future, because more bandwidth is demanded for higher data rate and new applications such as 5G. A typical N-path filter has

selectivity of only 2nd-order BPF roll-off is not sufficient to substitute the role of a SAW filter.

In 1968, an N-path filter topology with two complex pole pairs was proposed by Langer [75] as shown in Fig. 3.15. Similar to other well-known biquad active-RC filters (such as multiple feedback [76] or Sallen and Key [77] filters), it incorporates multiple passive-RC low-pass filters with an active amplifier to synthesize a complex pole pair for 2nd order LPF realization. When the switches are cyclically turned-on to operate as the N-path filter, the impedances of C_1 and C_2 are up-converted and a BPF having two complex pole pairs is implemented. Unfortunately, R_1 and R_2 have the same order of noise contribution as source resistance R_g, so that the noise performance may degrade a lot.

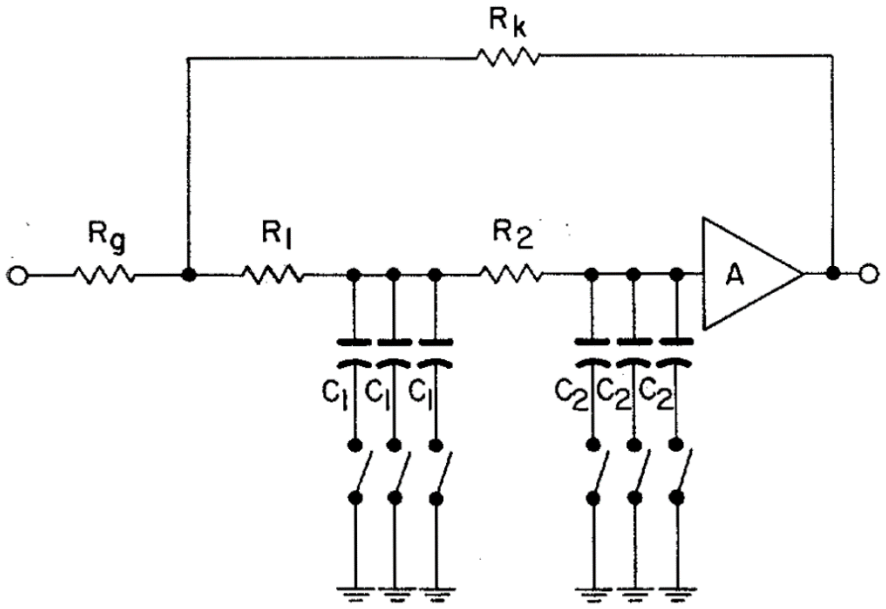

Fig. 3.15: Bandpass filter with two complex pairs of poles.

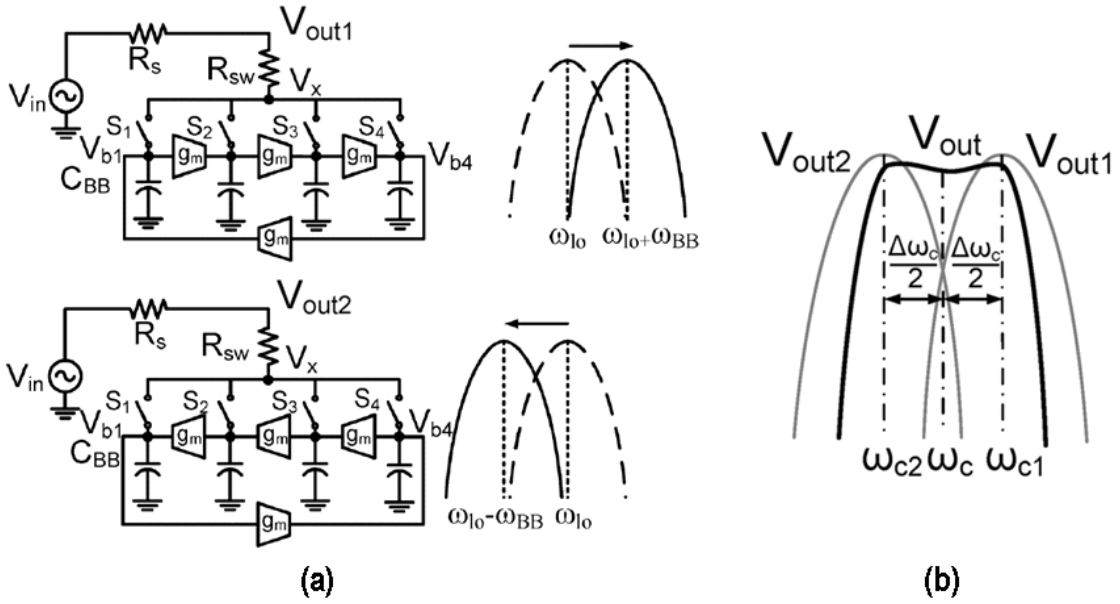

Fig. 3.16: (a) g_{m} cells are coupled between BB nodes with 90° phase difference in an N-path filter to produce the center-frequency shifted V_{out}, (b) higher order bandpass N-path filter by subtraction of output signals of two N-path filters [37].

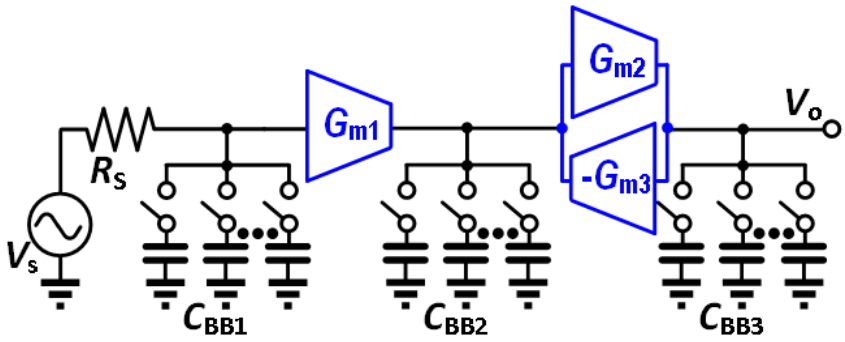

Fig. 3.17: A 6th order N-path filter is realized by coupling N-path filters with gyrators that are implemented as g_{m} cells.

As shown Fig. 3.16, transconductance cells g_{m} are connected between BB nodes with 90° phase difference in an N-path filter to produce a center-frequency shifted V_{out}. By subtracting the V_{out} of two 2nd order bandpass N-path filters with equal but opposite frequency shifts, a 4th order BPF is obtained [37]. However, the flicker noise of active g_{m} cells is up-converted and greatly degrades the noise performance.

As shown in Fig. 3.17, higher order N-path filtering can be realized by coupling N-path filters with gyrators that are implemented as g_{m} cells [38]. Compared to [37], the g_{m} cells operate at RF frequency [38] and there is no up-converted flicker noise from g_{m} cells at BB. Therefore, significant lower NF (i.e. <3 dB at 1GHz) than [37] is obtained.

3.5.5 Impairments of N-Path Filters and Mixer-First Receivers

Based on the discussions so far, the N-path filter or mixer first receiver shows promising linearity, tunable passband and improved performance as process scaling, resulting a potential solution on CMOS technology to replace off-chip SAW filters. However, it has some weaknesses as follows:

LO Leakage

For an N-path filter in CMOS technology, N clock pulses switch twice every period $1/f_{\mathrm{LO}}$ to drive the gate of MOS switches. This induces a coupled signal to the RF input port at N times f_{LO} via gate-drain (or gate-source) overlap capacitance or layout coupling capacitance. As there is unwanted CMOS switch transistor mismatch in reality, LO leakage at f_{LO} and its harmonics may be induced. This may also deteriorate the RX dynamic range. Besides, in the mixer-first receivers, the offset voltage of BB amplifiers following the mixer switches can be up-converted to become LO leakage at f_{LO} as well. Suppressing LO leakage at f_{LO} to lower than −70 dBm is required in many receivers [78].

Noise and Interference Folding

Unwanted noise at $|m\mathrm{N}-1|f_{\mathrm{LO}}$ of N-path filters can be folded back to f_{LO} where $m \in \mathbb{Z}$ and $m \neq 0$ causing NF degradation. It becomes a severe problem when frequency bands f_{LO} and $|m\mathrm{N}-1|f_{\mathrm{LO}}$ are occupied by different applications. For example, in a receiver for the LTE band 5 (824-849 MHz) application, an interferer at 2.4-2.5 GHz (such as Bluetooth) can also be down-converted to the BB when N=4. Therefore, harmonic rejection techniques [79, 80] may be demanded in practical receiver designs.

Reciprocal Mixing

SAW filters attenuate blockers to relax both RX linearity and LO phase noise requirements. In contrast, N-path filters provide low OOB impedance for blocker bypassing at the receiver input, but passive mixing operation is performed as well. The presence of a strong blocker causes reciprocal mixing which is proportional to both the blocker power and phase noise of the LO (see Eqn. (2.2)). To deal with the NF degradation due to reciprocal mixing constitutes a key challenge of N-path filter design.

3.6 Conclusion

Table 3.1 summarizes the pros and cons of existing techniques for blocker tolerant RF front-end designs. Hybrid transformer-based duplexers can achieve very high TX-RX isolation and linearity, but their performance is sensitive to antenna impedance, tuning range is limited and a large chip area is required [48]. Active TX leakage cancellation techniques can cover a wide tuning range of several GHz, however the active canceller limits the achievable linearity [35].

N-path filters and mixer-first receivers perform passive mixing and offers OOB rejection with high-linearity. They support a wide center frequency tuning range, can

achieve high Q [36, 38] and <3 dB NF [38]. Hybrid architectures can be further explored to improve the performance of N-path filters. For example, combing the N-path filter with g_m-C techniques [38] can enhance the selectivity.

The passive switched-RC N-path filter and mixer-first techniques will be deployed and further explored for the SAW-less receiver designs in this thesis.

Architecture	Pros	Cons
SAW filter	▪ >50dB out-of-band rejection ▪ very high linearity (>70dBm IIP3)	▪ passband frequency is not tunable ▪ bulky (a few mm^2 per filter)
Hybrid transformer-based duplexer	▪ >50dB TX-RX isolation ▪ >70dBm IIP3	▪ >4dB loss ▪ sensitive to antenna impedance variation ▪ limited tuning range (a few hundred MHz) ▪ large area occupation
Active TX leakage cancellation	▪ compact and reconfigurable	▪ limited tolerable blocker power (up to ≈0dBm) ▪ active canceller at RF input limits achievable linearity.
Q-enhanced LC BPF	▪ high Q	▪ limited tuning range ▪ large area occupation ▪ poor dynamic range
g_m-C BPF	▪ high operating frequency	▪ linearity is limited by active g_m cells
N-path filter and mixer-first receiver	▪ wide tuning range (> GHz) ▪ low loss ▪ high Q ▪ high linearity >10dBm B1dB 20-30dBm IIP3	▪ LO leakage ▪ noise and interference folding ▪ reciprocal mixing

TABLE 3.1: Pros and cons of existing techniques for blocker tolerant front-end designs.

CHAPTER 4

High Linearity Bottom-Plate Mixing Technique with Switch Sharing for N-path Filters/Mixers

4.1 Introduction

LTE-advanced wireless receivers require high-linearity up-front filtering to prevent corruption of the in-band signals by strong out-of-band (OOB) signals and self-interference from the transmitter in case of FDD. Surface acoustic wave (SAW)-duplexer-filters are generally used for this purpose (see Fig. 4.1), but supporting the plethora of existing and new bands becomes troublesome with separate filters for each band.

As discussed in Chapter 3, the N-path filter supports a wide center frequency tuning range, high Q [36] and promising linearity [36, 38]. However, the N-path filter performs OOB bypassing by offering a low OOB impedance [36]. If the RX input and TX output are directly connected to a shared antenna, the TX output would see a low RX-impedance, seriously degrading TX-performance. On the other hand, the OOB rejection of a 2nd order N-path filter is limited to ≈20 dB due to switch on-resistance and non-ideal clock duty cycle [36]. When the TX operates at full power, e.g. ≈+23 dBm (i.e. 9 V peak-to-peak in

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This chapter is a verbatim copy of the first journal paper in the list of publications except for the following changes:

1. The reason of using an external wide-band circulator is given in 4.1.
2. The measured B1dB as a function of blocker frequency offset and LO frequency are added in 4.5.2.
3. Together with the RX design presented in Chapter 5, the performance comparison with state-of-the-art designs is given in Chapter 5.

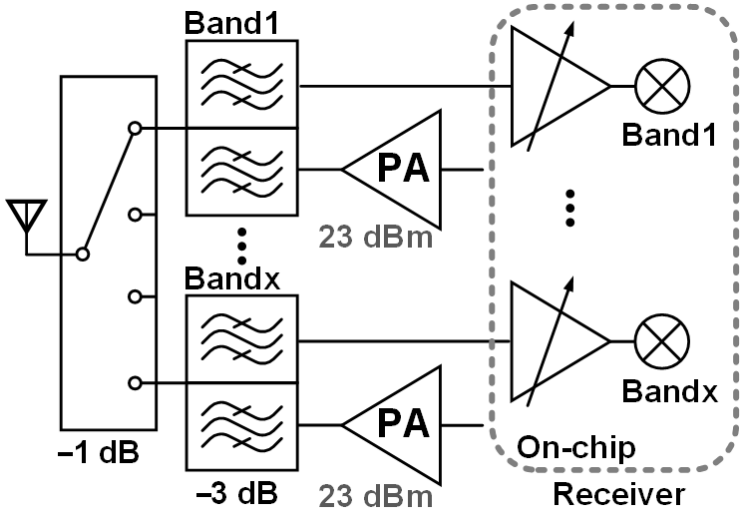


Fig. 4.1: Conventional LTE receiver with external SAW duplexing filters.

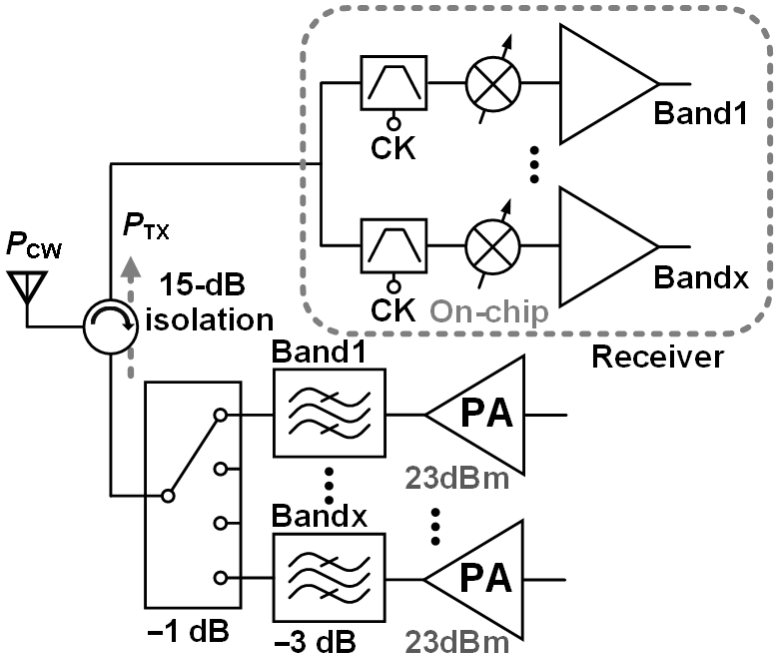


Fig. 4.2: Proposed LTE receiver with on-chip reconfigurable N-Path BPF.

50 ohm), there would still be 0.9 V peak-to-peak across the switches. Because the maximum supply voltage of current CMOS technologies is about 1 V, it seems not feasible to keep the intermodulation products low enough to maintain satisfactory RX sensitivity under these circumstances. Hence a TX-RX isolation to preliminarily attenuate the TX before entering the RX input seems needed.

A circulator [81] is a passive non-reciprocal microwave device with three ports. A radio frequency signal enters any port of a circulator and couples to the next port in the (circular) rotation direction, while isolating in the reverse direction. Wide-band circulators can provide about 10-15 dB isolation from TX to RX. In this chapter we explore the possibility of combining an off-chip circulator with high-linearity on-chip N-path filtering and mixing.

As an N-path band-pass filter has a programmable RF-center frequency, one circulator and a programmable chip can replace a set of SAW-filters, as shown in Fig. 4.1. However, even with 15 dB isolation from the circulator, the on-chip filter needs to deal with up to +4 dBm TX leakage P_{TX} (see Fig. 4.2), with a −15 dBm OOB continuous-wave (CW) blocker P_{cw} also present. Intermodulation P_{IIM3} will in this case deteriorate the RX sensitivity. For LTE applications, the integrated thermal noise is −101 dBm for a 20-MHz channel BW. If we assume P_{IIM3} is roughly the same as −101 dBm, the resulting required IIP3 is about 45-50 dBm, which is an extremely tough requirement. Inductor-less tunable N-path filters [36, 38] and mixer-first receivers in [42, 71, 82, 83] achieved >+10 dBm compression point and an IIP3 of 20-30 dBm, i.e. about 20 dB worse than required. Moreover, improved filtering is desired. A 2$^{\mathrm{nd}}$ order bandpass filter (BPF) is obtained with a simple switch-RC N-path filter and this high-linearity passive filtering relaxes the linearity requirement of the subsequent active amplifiers, which are much less linear. To sufficiently relax amplifier linearity, while dealing with strong blockers and TX leakage that is close to the desired RX frequency, more than 2$^{\mathrm{nd}}$ order filter roll-off may be required. Higher order N-path filtering can be realized by incorporating g_{m} cells [37, 38], but the

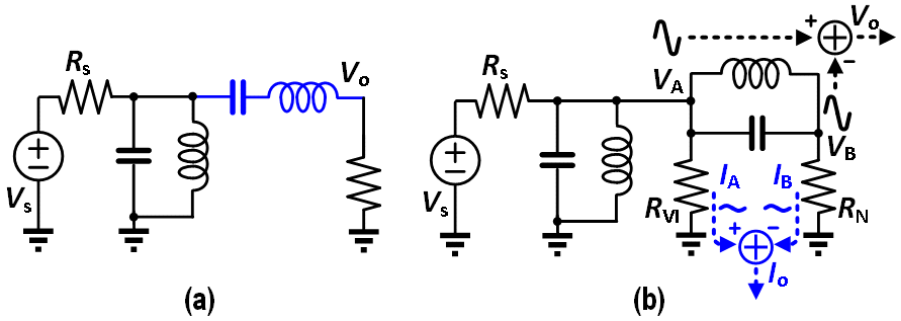


Fig. 4.3: (a) Conventional 4th order BPF realization by cascading a series LC tank. (b) Proposed 4th order BPF using V-I conversion and current subtraction.

active g_m circuits limit the achievable linearity. In this thesis we increase filter roll-off by cascading an N-path Voltage in-Voltage out (V-V) and Voltage in-Current out (V-I) BPF, while a bottom-plate mixing technique with switch sharing is proposed to enhance the linearity. This chapter is organized as follows: section 4.2 introduces the RF bandpass filtering receiver architecture, while section 4.3 describes the receiver circuit implementation. Section 4.4 proposes an LTI RLC model, to roughly estimate transfer function. Section 4.5 provides the measurement results, and the conclusion is presented in Section 4.6.

4.2 Receiver Architecture

We will now describe how we conceived the RX architecture. An N-path filter can emulate a parallel LC tank, modelled by a parallel R, L and C [36], and perform bandpass filtering. A 4th order BPF response could be obtained by adding a series LC tank (see Fig. 4.3(a) in case of ideal LC tanks). A series LC tank can be synthesized from a parallel LC tank via gyrator circuits [38], but these circuits limit achievable linearity. A quarter-wavelength transmission line could also be exploited [84], but this limits tuning range (0.6-0.85 GHz)

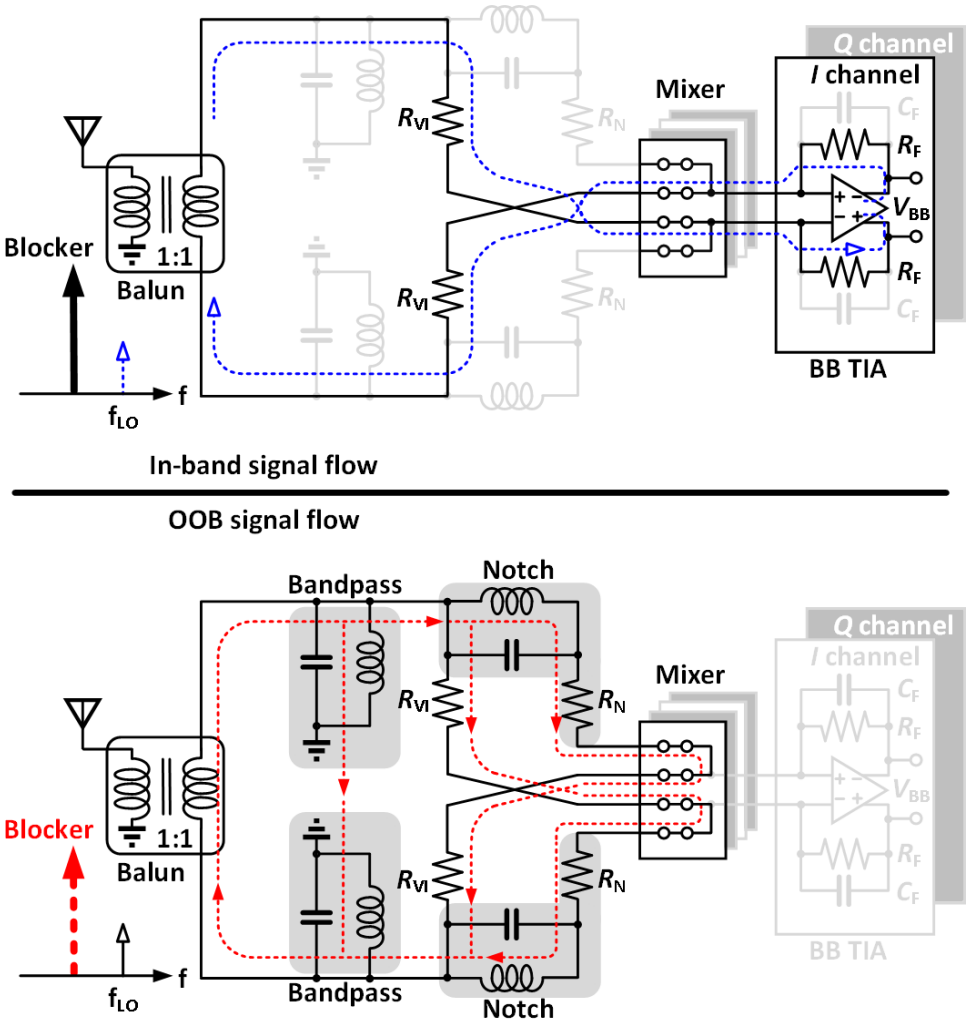


Fig. 4.4: (a) In-band and (b) OOB signal flow in the proposed receiver.

while the achieved IIP3 was not sufficient (18 dBm). Fig. 4.3(b) shows an alternative 4th order BPF realization by using two parallel LC tanks. As the tanks become high-ohmic in-band and low-ohmic OOB, the 1st tank attenuates OOB voltage swing bypassing OOB current, while the 2nd LC bypasses OOB current to the termination resistance R_N. If we take the output voltage across the 2nd tank, i.e. $V_o = V_A - V_B$ as in Fig. 4.3(b), the OOB

signals become largely common mode and are attenuated. Nevertheless, a high-linearity differential amplifier that can handle large common-mode voltage swings due to blockers is hard to implement. Instead, we propose V-I conversion by high-linearity passive resistors R_{VI} and R_{N} combined with current subtraction (see Fig. 4.3(b), output I_{o}). Current subtraction will be implemented by simple wire cross-coupling in the differential implementation.

Note that the BPF in Fig. 4.3(b) has an extra V-I conversion resistor that degrades filter-Q compared to Fig. 4.3(a) (i.e. Assuming R_{s}=R_{VI} for matching, R_{s}=R_{VI} simply halves the resistance seen by the input and hence halves Q.). Although not optimal for filter selectivity, this does allow for a high-linearity implementation and this is our key target here.

Fig. 4.4 shows the conceptual diagram of the proposed blocker rejection receiver. The parallel LC tanks are emulated by N- path filters. The differential structure offers the possibility of high-linearity current subtraction by wire-crossing. Input voltage signals are converted to current by resistor R_{VI}, which also allows for RF-impedance matching, and this current is down-converted by the mixer switches. For in-band signals, the LC tanks are high-ohmic, and the baseband (BB) current is converted to BB voltage V_{BB} by the Trans-Impedance-Amplifiers (TIA), as shown in Fig. 4.4(a). For OOB signals, the LC tanks become low ohmic and bypass the current as shown in Fig. 4.4(b). OOB signals are first attenuated by a voltage bandpass filter and then converted to current by resistors R_{VI}. The 2$^{\mathrm{nd}}$ tank acts now as a notch filter, blocking in-band signals (Fig. 4.4(a)), but passing OOB blockers (Fig. 4.4(b)) which are converted to current by R_{N}. Due to the differential symmetry and low switch resistance, OOB blocker current will mainly circulate in the RF domain (see Fig. 4.4(b)), ideally without entering the BB TIA. In summary, the 1$^{\mathrm{st}}$ stage gives RF blocker voltage reduction and the 2$^{\mathrm{nd}}$ stage V-I conversion with RF blocker current bypassing to improve selectivity.

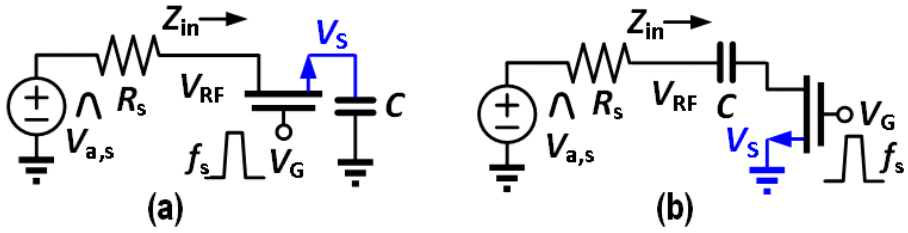


Fig. 4.5: Switched RC mixer with (a) top-plate and (b) bottom-plate mixing.

4.3 Circuit Implementation

4.3.1 Non-linearity Considerations

N-path filters and mixer-first receivers are switch-RC circuits that exploit the low-noise "mixer-region" [85, 86] or "passive mixer mode" [87], where the RC time constant is much larger than the on-time of the switch. In conventional (top-plate switched) mixers as shown in Fig. 4.5(a), the MOS switch suffers from largely varying $V_{\rm GS}$ and $V_{\rm DS}$, which modulates MOSFET channel resistance and limits linearity. To obtain some intuitive insight in the non-linearity mechanism, we will qualitatively describe the variations in channel resistance assuming the gate-voltage is switched on to a constant value (e.g. =VDD).

For simplicity, suppose the RF-voltage is a sinewave at frequency $f_{\rm RF}$ in its positive signal-half with amplitude $\hat{V}_{\rm RF}$ and average=0 (DC value=0), so that the RF-side of the MOSFET is the drain terminal. We choose $\rho = R_{\rm sw}/R_{\rm s} << 1$ (e.g. $\rho = 0.1$) to achieve high OOB linearity. For in-band signals $Z_{\rm in}$ is significantly higher than source resistance R_s (e.g. $4.3R_s$ for a 4-path mixer with 25% duty-cycle clocks[73]). As the switch resistance is assumed to be much smaller than R_s (e.g. $\rho = 0.1$), the BB-voltage $\hat{V}_S$ will almost reach $\hat{V}_{RF} = \hat{V}_{a,s}\, Z_{\rm in}/(R_s + Z_{\rm in})$ where $\hat{V}_{a,s}$ is the amplitude of the antenna signal. As a result, $V_{\rm GS}$ of the mixer switch is strongly modulated while the switch is closed, whereas the modulation of $V_{\rm DS}$ is much smaller and the non-linearity is mainly due to $V_{\rm GS}$ modulation. For OOB signals, $Z_{\rm in}$ decreases with offset frequency, reducing the $V_{\rm GS}$ modulation, while

the V_{DS} modulation becomes slightly higher due to the increasing current. The distortion overall reduces due to the OOB filtering at V_{S}. When OOB signals are very far away from the LO frequency, the BB-voltage $\hat{V}_S$ becomes almost zero resulting in negligible V_{GS} modulation. Assuming $\hat{V}_{DS} \approx \rho \hat{V}_{a,s}$, OOB IIP3 can then be estimated as [88]:

$$V_{\mathrm{IIP3}} = \sqrt{\frac{4}{3}\frac{(1+\rho)^4}{\rho^3(2g_2^2 - g_3(1+\rho))}} \tag{4.1}$$

Where g_2 and g_3 are related to the 2nd and 3rd derivation of $I_D\,(V_{DS})$, which can be estimated as g_2 is $-(2V_{\mathrm{OD}})^{-1}$ and $g_3 = -(2V_{\mathrm{SAT}}^2)^{-1}$, where V_{OD} is overdrive voltage $V_{\mathrm{GS}} - V_{\mathrm{th}}$ and V_{SAT} is a velocity saturation parameter respectively [88].

4.3.2 High Linearity Bottom-Plate Mixing Technique

We will now introduce the bottom-plate mixing technique. Instead of using a switch between the RF-node and the "top-plate" of a grounded capacitor (Fig. 4.5(a)), we propose to connect the RF-node to the top-plate and instead switch the bottom-plate to ground as shown Fig. 4.5(b). Although the name may suggest a relation with bottom-plate sampling, it is clearly different as it doesn't use two switches, while it also doesn't produce a sampled time-discrete output, but rather a continuous mixer output (for a further discussion of the difference between mixing and sampling, see also [89]). The main target for bottom-plate mixing is switch-resistance induced distortion improvement. In contrast, the deployment of bottom-plate sampling is for reducing the signal dependent charge injection and clock feedthrough.

For LTE applications, the duplex frequency is <200 MHz for most of the frequency bands, while a BPF with channel BW up to 10 or 20 MHz is required. Hence not only far-OOB IIP3 matters, but also the non-linearity for OOB signals that are still rather close to the LO-frequency. To reduce the V_{GS} modulation and improve linearity, we proposed a

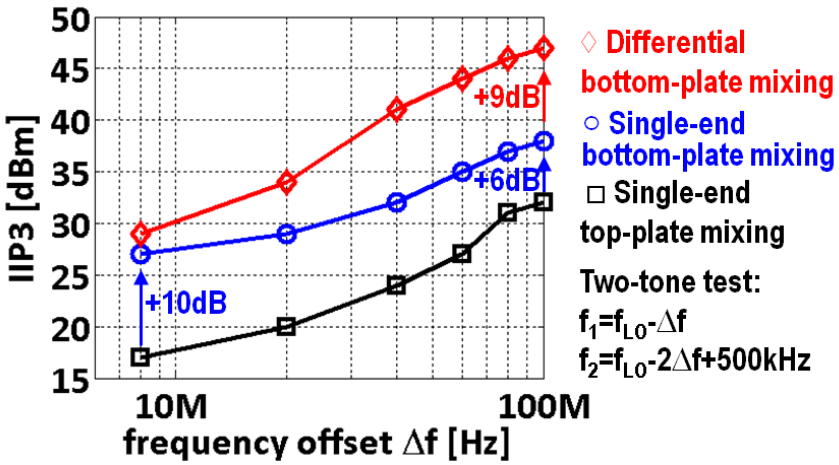


Fig. 4.6: Simulated IIP3 for 4-path single-ended top-plate, single-ended bottom-plate and differential bottom-plate mixing filters.

bottom-plate mixing technique [90] as shown in Fig. 4.5(b). When the switch is turned on, the drain terminal voltage V_D of the NMOS switch will be pulled to ground, instead of being connected to a variable voltage V_S as in Fig. 4.5(a). Now V_{GS} is kept constant, i.e. the in-band V_{GS} modulation problem is avoided. In-band voltage signals are down-converted and mixed to capacitor C, while the signal source still sees a high impedance, i.e. very small V_{DS} modulation occurs. In conclusion, the bottom-plate mixing keeps V_{GS} constant to obtain better linearity.

Applying 1-GHz 25-% duty cycle 4-phase clocks with rising/falling time of 10 ps and common mode voltage of half supply, simulations reported in Fig. 4.6 indeed confirm benefits (we will discuss them in more detail below). We tried to quantify the benefits analytically, but unfortunately accurate MOSFET models are complex. Experiments also indicate that several effects can play a role, e.g. subthreshold conduction, body effect and charge injection. Splitting and quantifying these factors proved complicated, and hence we resort to simulations combined with qualitative reasoning and rough calculations. Bottom-

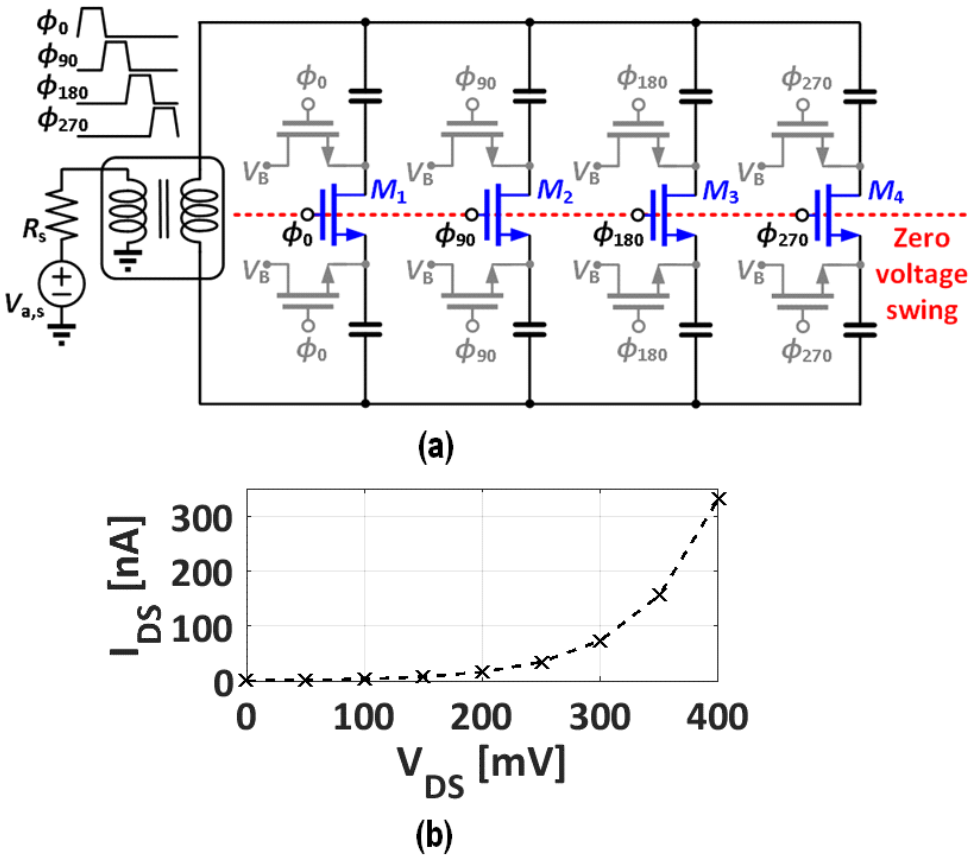


Fig. 4.7: (a) Circuit schematic of a 4-phase differential bottom-plate mixing bandpass N-path filter. *W*/*L*=180 um/30 nm for M_1-M_4 and *W*/*L*=18 um/30 nm for other NMOS transistors, (b) simulated non-linear sub-threshold current I_{DS} of M_1 when it is off.

plate mixing proofs to have clear linearity benefits, and reasoning supports this: apart from avoiding V_{GS} modulation, source-bulk voltage modulation is also avoided in Fig. 4.5(b), reducing threshold voltage variation due to the body effect. Moreover, as in bottom-plate mixing circuits, signal dependent charge injection from MOS switches is reduced as there is a low-ohmic path to ground.

Fig. 4.7(a) shows the circuit schematic of a 4-phase differential bottom-plate mixing N-path filter. M_1-M_4 are NMOS switches with large W/L ratio for the N-path filter function, while the other NMOS switches are chosen 10x smaller to periodically reset the DC bias to the common-mode level. Larger switch size for the DC bias setting can offer faster settling (i.e. less clock cycles) to the desired common-mode level, but more LO power is required. Note that one *shared NMOS switch* can be used for both circuit halves, instead of two switches to ground in the conventional pseudo differential architecture of Fig. 4.5(b). Therefore, ρ is reduced to half of its single ended value thanks to switch sharing in the differential circuit. For $\rho << 1$, Eqn. (4.1) can approximate to:

$$V_{\text{IIP3}} \approx \sqrt{\frac{4}{3}\frac{1}{\boldsymbol{\rho^3}(2g_2^2-g_3)}} \tag{4.2}$$

Eqn. (4.2) predicts OOB IIP3 is improved by 9 dB if ρ is halved. Fig. 4.6 shows the simulated IIP3 for a single-ended top-plate, single-ended bottom-plate and differential bottom-plate mixing N-path filter, driven by 4-phase clocks and switch size of 180 um/30 nm. The BPF BW $f_{-3\text{dB,BPF}}$ is 30 MHz and f_{LO} is 1 GHz. TSMC 28 nm technology simulation with a PSP MOS-model were used. Comparing to the conventional topology, bottom-plate mixing improves IIP3 by 10 dB and 6 dB for in-band and OOB respectively. Note that the switch sharing offers an additional 9 dB OOB IIP3 improvement, as predicted by Eqn. (4.2).

An experiment was devised to find out whether weak inversion conduction in M_1-M_4 limits in-band linearity for the mixer in Fig. 4.7(a). Ideal switches were added in series to both sides of M_1-M_4, to block current during their off-state. This improves linearity, indicating that subthreshold current likely limits the achievable linearity. As shown in Fig. 4.7(a), Z_{in} is high ohmic for in-band signals, resulting in significant input signal swing which is AC-coupled via the N-path filter capacitors to the drain or source terminals of the transistors that are supposed to be off, but apparently modulate their current. Fig. 4.7(b)

shows the simulated I_{DS} of M_1 in Fig. 4.7(a) as a function of V_{DS} (common mode of V_D and V_S is 0.2 V) when M_1 is off (gate terminal is connected to the ground). The un-constant slope indicates the sub-threshold current is non-linear.

In summary, the in-band IIP3 of conventional top-plate mixers is dominated by V_{GS} modulation, while far-OOB IIP3 is limited mainly by V_{DS} modulation. Bottom-plate mixing keeps V_{GS} constant to achieve high linearity for all frequencies. Moreover, OOB linearity is improved by 9 dB due to switch sharing. Subthreshold current likely limits the achievable in-band IIP3.

4.3.3 Cascading Passive RF BPF Stages

The circuit schematic of the entire proposed receiver is shown in Fig. 4.8(a). C_A and the corresponding switches implements the bandpass in Fig. 4.4(b). C_B, R_{VI}, R_N and the corresponding switches implements the OOB current subtraction circuit in Fig. 4.4(b). Because the proposed receiver is self-biased, two external RF DC blockers with low loss (<0.5 dB up to 8 GHz) are applied. A differential external clock with 4 times the LO frequency f_{LO} is applied to generate 4-phase 25-% duty-cycle clocks via a divide-by-4 ring counter. By exploiting only one clock-edge, the pulse width of 25-% duty-cycle clocks is determined by the period and not sensitive to the duty-cycle of the external clock. As a result, the timing error can be smaller than for a divide-by-2 flip-flop with extra logic circuits to realize 25-% duty cycle. Note that most power is consumed in the output buffers that drive large mixer switches (not in divider itself), so that the power penalty of using a divide-by-4 compared to a divided-by-2 4-phase clock generator is not so significant. Both N-path filter stages are driven by the same clocks and hence have the same center frequency. Zero-IF frequency conversion is also implemented in the second V-I stage. The common-mode bias-voltage V_B for the mixer switches in the first V-V BPF is set to ≈0.2 V. There is a trade-off regarding the choice of V_B. Lower V_B reduces on-resistance of switches, but increases subthreshold current when switches are off. The W/L of all mixer

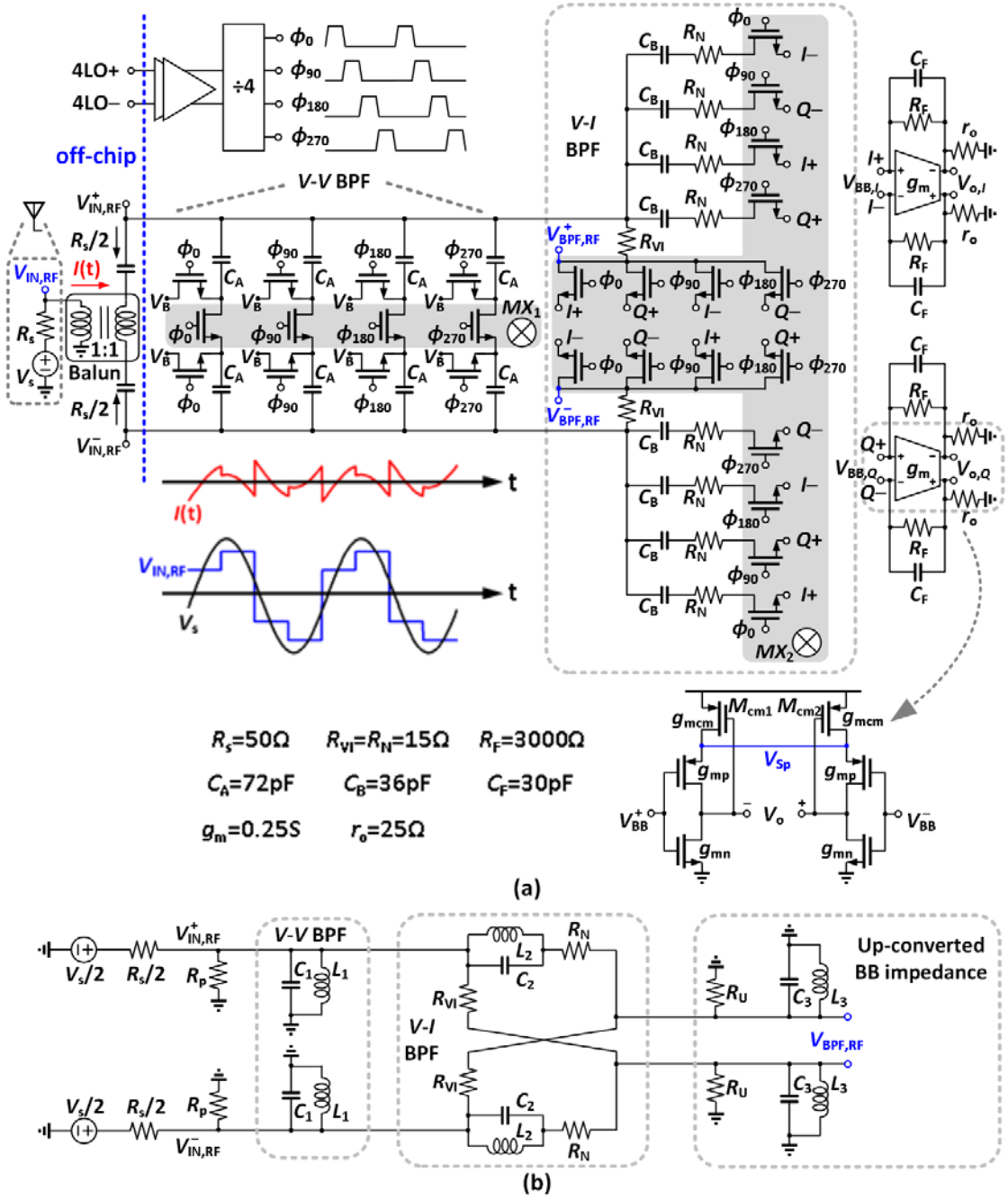


Fig. 4.8: (a) Circuit schematic of the proposed receiver, and (b) the corresponding RLC model (equivalent LTI model for the RF part)[1].

[1]One single set of mixer switches MX_2 is now implementing L_2C_2 and also L_3C_3.

switches is 180 um/30 nm and the differential on-resistance is as low as ≈2 Ω. The resistance of R_{VI} and R_N for V-I conversion is 15 Ω, which is implemented in top-metal with high current density tolerance, low parasitic capacitance and very high linearity. R_{VI} and R_N also reduce the voltage swing across mixer switches to improve the linearity. Mismatch between R_{VI} and R_N causes intermodulation tones at f_{LO}+f_b and f_{LO}-f_b, where f_b is blocker frequency. These intermodulation tones will be down-converted to a BB frequency of f_b, which is not in-band, and hence not of primary importance.

Much like the band-pass filter, a conventional top-plate switch notch N-path filter [91] also suffers from strong V_{GS} modulation that causes non-linearity. The bottom-plate mixing technique can also be applied in the notch filter that is composed of C_B, R_N and the corresponding mixer switches in Fig. 4.8(a) to gain similar benefits. 4xR_N are used instead of one (in Fig. 4.4) and the switch to ground to reduce V_{GS} modulation is possible now. Also, the down-converted BB output current signals are available for OOB blocker bypassing. Switch sharing between circuits halves seems not possible.

In this receiver, the down-converted BB signal is used as output, so that the OOB rejection limitation due to switch resistance in a bandpass N-path filter [36] is avoided.

The second V-I BPF stage in Fig. 4.8(a), composed of R_{VI} and a notch N-path filter, enhances the selectivity, but the OOB impedance at the V-I BPF input is $(R_{VI}+R_{sw})||(R_N+R_{sw})$ while it is R_{sw} in a conventional V-V N-path filter [36]. For mixer switches in the V-I BPF that are off, still a large OOB voltage signal is directly coupled to the MOSFET-switch via capacitor C_B, again potentially resulting in non-linear subthreshold current limiting IIP3. Fortunately, the first stage V-V BPF already greatly reduces the OOB voltage signal swing, alleviating this problem.

For implementing more number of paths, a more elaborate BB I/Q re-combination circuit is required, see e.g. the 8-path receiver by [73].

4.3.4 Baseband Amplifier

A CMOS inverter is one of the best transconductors in terms of dynamic range per power [92], and it can serve to make a low-noise quite-linear BB transimpedance amplifier. Stability concerns for closed loop operation are avoided in a single-stage amplifier. Because it is pseudo differential, extra circuitry is needed to reduce the common mode gain, while maximizing differential mode gain, which often leads to extra power consumption and noise [60, 93]. We avoid this by implementing a low common-mode output impedance using M_{cm1} and M_{cm2} which are put above the core g_{mn} and g_{mp} devices for current re-use, as shown in the right-bottom corner of Fig. 4.8(a). Feedback resistor R_{F} provides self-biasing. Each BB amplifier consumes about 15 mW from a 1-V supply. The W/L values are 1700 um/40 nm and 1200 um/40 nm for the PMOS and NMOS of the inverter respectively, while $g_{\mathrm{mn}} + g_{\mathrm{mp}}$=250 mS and $r_{\mathrm{on}} \| r_{\mathrm{op}}$=25 Ω. By using a higher threshold voltage for M_{cm1} and M_{cm2} and small overdrive voltage of about 60 mV for the PMOS of the inverter, all transistors can operate in saturation. M_{cm1} and M_{cm2} only generate common mode noise, which will be cancelled at the differential output. Operating M_{cm1} and M_{cm2} in saturation also provides isolation between the supply voltage and the outputs of the amplifier, which is good for supply noise rejection. For differential input signals, voltage V_{Sp} ideally shows very low impedance and small voltage swing due to differential symmetry and a gain of $\approx (g_{\mathrm{mn}} + g_{\mathrm{mp}})(\mathrm{r_{on}} \| \mathrm{r_{op}})$=16 dB is achieved. For a common mode input signal, V_{Sp} follows input signal and g_{mp} is degenerated. The BB amplifier output is diode-connected with output impedance of $1/g_{\mathrm{mcm}}$ giving a low common-mode gain of $g_{\mathrm{mp}}/g_{\mathrm{mcm}}$≈3 dB. Note that a traditional CM-feedback circuit with triode devices would lead to much smaller g_{mcm}, i.e. more common mode gain.

4.4 Circuit Analysis

In this section we will analyze different properties of the mixer-first receiver, like transfer function, noise and input impedance.

The equivalent RLC circuit in Fig. 4.8(b) models the frequency response of the multiple-stage N-path filter in magnitude. The intuition behind this semi-empirical model comes from the observation that the capacitors C_{A} in the first capacitor bank are not directly in parallel to the capacitors C_{B} in the second bank, but are coupled via resistor R_{N}, introducing an extra filter order.

4.4.1 RLC BPF Model

The filter shape of an N-path filter around its LO-frequency can be modelled by a parallel RLC circuit [36, 91]. The corresponding model parameter can be found as [91]:

$$R_{\mathrm{p}} = \frac{N^2 sin^2\left(\frac{\pi}{N}\right)}{\pi^2 - N^2 sin^2\left(\frac{\pi}{N}\right)} (R_{\mathrm{s}} + R_{\mathrm{L}}) \tag{4.3}$$

$$\boldsymbol{C_p = \frac{\pi^2}{mNsin^2(\pi/N)} C} \tag{4.4}$$

$$\boldsymbol{L_p = \frac{1}{(2\pi f_{LO})^2 C_p}} \tag{4.5}$$

Where m=2 for single-ended circuit and m=8 for differential case. N is the number of clock-phases. Note that the LC tank modelled the N-path filter only in its magnitude but not in its phase as noted in [87] in the paragraph before Eqn. (43).

Assuming mixer switches in Fig. 4.8(a) are ideal. The RLC tank equivalent circuit for the RF part of the proposed receiver is shown in Fig. 4.8(b). The V-V BPF is modelled by the L_1C_1 tank while the V-I BPF is modelled by R_{VI}, R_{N} and the L_2C_2 tank. The Miller approximation is applied to the BB amplifier, resulting in capacitor $(1 + A)C_{\mathrm{F}}$, where $A = g_m(r_0||R_{\mathrm{F}})$ is the gain of the BB amplifier. The effect of switching before this Miller

capacitor is modelled with the L_3C_3 tank, which offers extra OOB rejection. In contrast to a single balanced mixer, we use a balun-driven double-balanced mixer. Now each of the baseband components is connected twice per period to the RF source, doubling the conduction time, compared to the single-end case. Therefore, the BB resistance $R_{\mathrm{BB}} \approx R_{\mathrm{F}}/(1+A)$ is up-converted and becomes $R_{\mathrm{U}} = 2\gamma R_{\mathrm{BB}}$, where $\gamma = 2/\pi^2$ for 4-path case [73]. Note that C_{p} and L_{p} in Eqn. (4.4-4.5) only depends on the number of phases, the BB capacitance in a single path and the LO frequency. The mixer switches up-convert the BB low-pass impedance to an RF band-pass impedance. To be more precise, the switched-RC passive mixer in Fig. 4.8(a) performs frequency-conversion and mixing. For a narrowband in-band signal close to the LO-frequency, the capacitors contain a (quasi-) constant baseband voltage. Hence a sinewave RF-excitation results in a stair-case waveform response at $V_{\mathrm{IN,RF}}$ [36], as shown in the lower left corner of Fig. 4.8(a). The voltage difference between the sine and stair-case renders a "spiky" current with harmonic content (Fig. 4.8(a)), which is dissipated in signal-source-resistance $0.5R_s$. This dissipation can be modelled as an "harmonic shunt impedance" $R_{\mathrm{p}} \approx 4.3(0.5R_s)$ for the 4-phase case [73]. Note that the capacitance of C_{A} *does not* affect this in-band R_{p}. Moreover, as C_{B} contains almost the same voltage as C_{A}, there is hardly any difference in the voltage across $0.5R_s$ with or without C_{B}. Hence only one R_{p} suffices to model the in-band loss of both the switched C_{A} and C_{B} in this receiver. Using the RLC model for the RX shown in Fig. 4.8(b) and solving the node equations at $V_{\mathrm{IN,RF}}$ and $V_{\mathrm{BPF,RF}}$, we derived $H_{\mathrm{o,RF}}(s) = V_{\mathrm{BPF,RF}}(s)/(V_{\mathrm{s}}/2)$ as:

$$H_{\mathrm{o,RF}}(s) = \frac{2R_{\mathrm{p}}(0.5R_{\mathrm{s}}+R_{\mathrm{p}})^{-1}(C_1C_2C_3R^2R_{\mathrm{A}})^{-1}s^3}{s^6+D_{\mathrm{x}}s^5+D_{\mathrm{y}}s^4+D_{\mathrm{z}}s^3+D_{\mathrm{y}}\,\omega_{\mathrm{LO}}^2s^2+D_{\mathrm{x}}\,\omega_{\mathrm{LO}}^4s+\,\omega_{\mathrm{LO}}^6} \tag{4.6}$$

$$D_{\mathrm{x}} = \frac{2}{C_1R} + \frac{1}{C_2R} + \frac{2}{C_3R} + \frac{1}{C_3R_{\mathrm{U}}} + \frac{1}{C_1R_{\mathrm{A}}}$$

$$D_{\mathrm{y}} = 3\,\omega_{\mathrm{LO}}^{2} + \frac{L_2 L_3 (R+R_{\mathrm{U}})}{\omega_{\mathrm{LO}}^{-4} R^2 R_{\mathrm{U}}} + \frac{L_1 L_2 (R+R_{\mathrm{A}})}{\omega_{\mathrm{LO}}^{-4} R^2 R_{\mathrm{A}}} + \frac{L_1 L_3 (R+2R_{\mathrm{U}})(R+2R_{\mathrm{A}})}{\omega_{\mathrm{LO}}^{-4} R^2 R_{\mathrm{U}} R_{\mathrm{A}}}$$

$$D_{\mathrm{z}} = \frac{2(L_2 R_{\mathrm{U}} + L_3 (R+2R_{\mathrm{U}}))}{\omega_{\mathrm{LO}}^{-4} R R_{\mathrm{U}}} + \frac{L_1 L_2 L_3 (R+R_{\mathrm{U}}+R_{\mathrm{A}})}{\omega_{\mathrm{LO}}^{-6} R^2 R_{\mathrm{U}} R_{\mathrm{A}}} + \frac{2L_1 (R+2R_{\mathrm{A}})}{\omega_{\mathrm{LO}}^{-4} R R_{\mathrm{A}}}$$

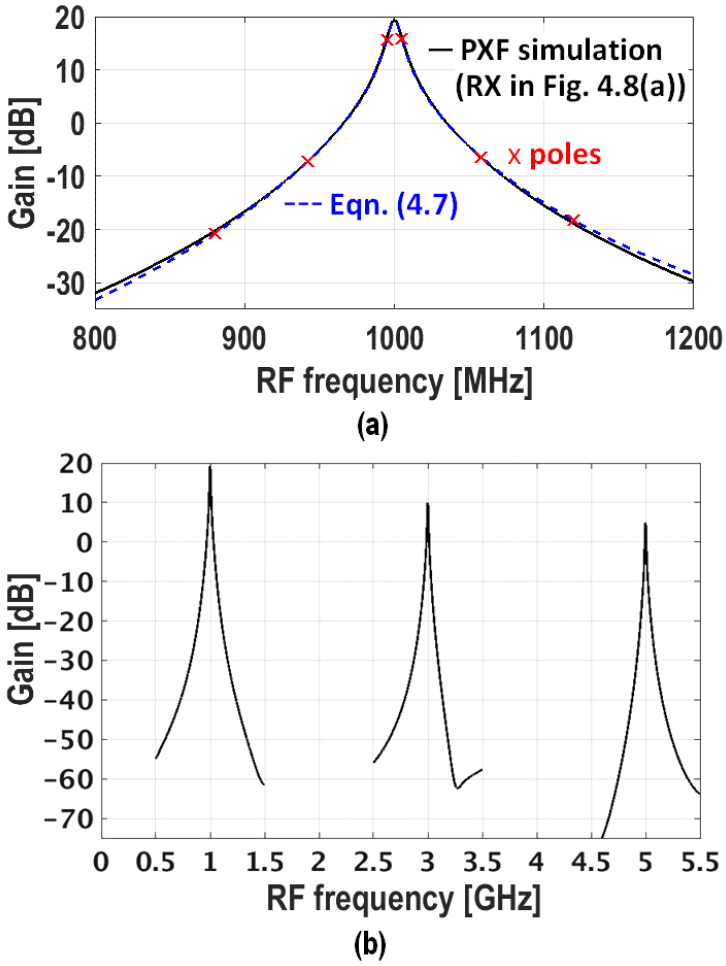


Fig. 4.9: PXF simulation (sideband: -1, LO=1 GHz) of the proposed receiver with ideal components and the calculated gain $|V_{\mathrm{o}}/V_{\mathrm{s}}/2|$ in Eqn. (4.7), (b) broadband filter response up to 5th harmonic (sideband: -1, -2, -3, LO=1 GHz).

Where $\omega_{\mathrm{LO}}^{-2} = L_1C_1 = L_2C_2 = L_3C_3$, $R_{\mathrm{A}} = (0.5R_{\mathrm{s}})||R_{\mathrm{p}}$ and $R = R_{\mathrm{VI}} = R_{\mathrm{N}}$. Assuming the R_{s} is given, R_{VI} and R_{F} are designed to provide in-band matching to it. Channel Bandwidth tuning can be realized by simultaneously changing all the capacitors with the same ratio. Substituting the component values (see Fig. 4.8(a), bottom left corner) in Eqn. (4.6), and obtaining the corresponding RLC values, we can find the poles are located at $j\omega_{\mathrm{LO}} \pm 2\pi(5\mathrm{M})$ rad/s, $j\omega_{\mathrm{LO}} \pm 2\pi(58\mathrm{M})$ rad/s and $j\omega_{\mathrm{LO}} \pm 2\pi(120\mathrm{M})$ rad/s. Assuming $R_{\mathrm{F}}C_{\mathrm{F}} \gg \omega_{\mathrm{LO}}^{-1}$, $\mathrm{V_{BB}}$ at the BB amplifier input is a down converted version of $V_{\mathrm{BPF,RF}}$, and the voltage gain from V_{RF} to V_{BB} can be derived by dividing Eqn. 4 in [73] by Eqn. 6, resulting $1/\sqrt{4\gamma}$ (=0.9 dB) where γ is $2/\pi^2$ for 4-phase case. Hence, the gain of this receiver can be written as:

$$\left|\frac{V_{\mathrm{o}}}{V_{\mathrm{s}}/2}\right| \approx \left|H_{\mathrm{o,RF}}(s)(\sqrt{4\gamma})^{-1}g_{\mathrm{m}}(r_{\mathrm{o}}||R_{\mathrm{F}})\right| \tag{4.7}$$

To verify analysis, Fig. 4.9(a) shows a Spectre PSS/PXF simulation result for the receiver circuit in Fig. 4.8(a) and the estimate of the receiver gain of Eqn. (4.7). As $f_{\mathrm{RX}} - f_{\mathrm{TX}}$<200 MHz for most LTE frequency bands, we focus on f_{LO} ±200 MHz, and the fit is satisfactory.

Fig. 4.9(b) shows the filter response up to the 5th harmonics and the 1st order roll-off in magnitude can be observed. The second order harmonic response is rejected due to differential architecture, while odd harmonic rejection is not implemented in this RX design, as in many other 4-path I-Q receivers. In principle harmonic rejection can be achieved, as shown for instance in the 8-path receiver in [73].

4.4.2 OOB Rejection of the Receiver

In the proposed receiver, the first V-V N-path BPF attenuates blockers but the OOB rejection is limited by the resistance of the mixer switches [36]. Instead of using capacitors to ground, the feedback capacitor across the BB amplifier is used to save area and provide higher feedback factor for better OOB linearity [20]. Here the OOB rejection is ultimately

limited due to the finite transconductance g_{m} of the BB-amplifier. Thanks to the differential circuit symmetry, the BB output nodes $I+$, $Q+$, $I-$ and $Q-$ of the second V-I BPF stage show very low voltage swing, resulting in effective OOB-current bypassing (see Fig. 4.8(a)).

4.4.3 Noise Performance

The noise factor F of the receiver can be calculated as the total output noise divided by the noise contribution due to the thermal noise from the antenna or signal source, modelled as $\overline{v_{n,s}^2} = 4kTR_s$. All the mixer switches are equal in Fig. 4.8(a).The resulting F of this RX can be derived as:

$$F = 1 + \frac{(R_{VI}+R_{sw})}{R_s} + \frac{(R_{VI}+R_s+R_{sw})}{4.3R_s} + \frac{(R_{VI}+R_s+R_{sw})^2}{\gamma(2R_F)R_s}$$

$$+ \frac{\overline{v_{n,in,A}^2}(4(R_s+R_{VI}+R_{sw})+2R_{BB})^2}{4kTR_s(4\gamma)(2R_{BB})^2} \tag{4.8}$$

An explanation is given below: The thermal noise of R_{N} and the corresponding mixer switch is suppressed by the switched capacitor C_{B} in Fig. 4.8(a) due to its notch function. The direct noise contribution from thermal noise of R_{VI} and the mixer switch in series is $(R_{\mathrm{VI}} + R_{\mathrm{sw}})/R_{\mathrm{s}}$. Moreover, noise degradation due to noise folding from odd harmonics of the mixing frequency occurs. Thermal noise of R_s, R_{VI} and R_{sw} are hence down converted and sampled [73], leading to a summation of $4kT(R_s + R_{VI} + R_{sw})/n^2$ terms, where $n = 3, 5, 7, \ldots$ for a 4-path mixer. This sums up to $\approx 4kT(R_s + R_{VI} + R_{sw})/4.3$. The up-converted noise current induced by the BB feedback resistor R_F renders the term proportional to $1/(2\gamma R_F)$. Note that R_F is much higher than R_s primarily due to the negative feedback. Therefore the noise contribution of R_F is minor. The input-referred noise of the BB amplifiers is $v_{n,in,A}^2 = \overline{v_{n,out,A}^2}/A^2$, where $\overline{v_{n,out,A}^2}$ is noise at the BB amplifier output and $\sqrt{(\overline{v_{n,out,A}^2})} = 1.6$ nV/$\sqrt{\text{Hz}}$ from simulation. The noise voltage due to

source resistance at the BB amplifier input undergoes a voltage division with gain of $\sqrt{4\gamma}$ and it is $\overline{v_{n,s,BB}^2} = 4kTR_s(4\gamma)(2R_{BB}/(4(R_s + R_{VI} + R_{sw}) + 2R_{BB}))^2$, where R_{BB} is $R_F/(1 + A)$. Filling the design values in Eqn. (4.8), NF of 3.9 dB at very low frequency is obtained.

4.4.4 Influence of Parasitic Capacitance at the RF Input Port

Bottom-plate mixing can offer blocker rejection with significantly higher linearity than a conventional top-plate mixing N-path filter. However, it also brings some limitations. There is no isolation by the mixer switch between the RF input and filter-capacitors when a switch is in its off-state, complicating the read-out of the baseband signal across the capacitors. The floating filter capacitors will have a parasitic capacitance to substrate, which is directly connected to the RF input introducing signal loss[2]. In this design, MOM capacitors were used, and the lowest layer was metal 3 instead of 1 to reduce parasitic capacitance. QRC extractions indicate that the parasitic capacitance is about 1.1 % of MOM capacitance. As shown in Fig. 4.8(a), the total MOM capacitance seen by RF input is $4C_\mathrm{A} + 4C_\mathrm{B}$. Since one of the bottom plates of C_A is connected to the symmetry point when the switch is on, the total MOM parasitic capacitance is $0.011(4C_\mathrm{A} \times 7/8 + 4C_\mathrm{B})$≈4.4 pF. As large mixer switches were applied for high linearity, substantial extra parasitic MOSFET junction and overlap capacitances are introduced at other nodes. The total unwanted parasitic capacitance C_s that is from RF input $V_{\mathrm{IN,RF}}^{+}$ ($V_{\mathrm{IN,RF}}^{-}$) coupled to ground in Fig. 4.8(a) is about 5.2 pF. It decreases the harmonic shunt impedance $R_\mathrm{p}(\omega_\mathrm{LO})$ and increases the folded noise [88]. For a 4-path mixer-first receiver, $R_\mathrm{p}(\omega_\mathrm{LO})$ can be approximated as [88]:

$$\boldsymbol{R_p(\omega_{LO}) \approx 4.3R_{sw}(1 + (4R_{sw}C_s\omega_{LO} + R_{sw}/R_s)^{-1})} \tag{4.9}$$

[2]The paracistic capacitance can be put only at bottom plate of the MOM capacitor on the switch side, but this has even larger disadvantage.

The reduction of $\boldsymbol{R_p(\omega_{LO})}$ at higher $\boldsymbol{\omega_{LO}}$ causes gain, S_{11} and NF degradation. Taking the parasitic capacitance $\boldsymbol{C_s}$ into account, the RX gain as a function of $\boldsymbol{\omega_{LO}}$ can be written as:

$$\left|\frac{2(R_{\mathrm{in}}(\omega_{\mathrm{LO}})||(j\omega_{LO}C_s)^{-1})R_{\mathrm{U}}}{(0.5R_{\mathrm{S}}+R_{\mathrm{in}}(\omega_{\mathrm{LO}})||(j\omega_{LO}C_s)^{-1})(R_{\mathrm{VI}}+R_{\mathrm{U}})}(\sqrt{4\gamma})^{-1}g_{\mathrm{m}}(r_{\mathrm{o}}||R_{\mathrm{F}})\right| \tag{4.10}$$

Where $R_{\mathrm{in}}(\omega_{\mathrm{LO}})$ is $\mathrm{R_p}(\omega_{\mathrm{LO}})||(R_{\mathrm{VI}}+R_{\mathrm{U}})$, $R_{\mathrm{U}}=2\gamma R_{\mathrm{F}}/(1+A)$, $\gamma=2/\pi^2$, $A=g_m(r_0||R_{\mathrm{F}})$. (see Fig. 4.8(b))

The parasitic capacitance causes direct input attenuation and more harmonic folding noise [88]. Considering these mechanisms, the noise factor as a function of the LO frequency can be written as:

$$F \approx 1+\frac{(R_{VI}+R_{sw})}{\mathrm{Re}(Z_s)}+\frac{(\mathrm{Re}(R_{VI}+R_s+R_{sw}))^2}{\mathrm{Re}(Z_s)\,\mathrm{R_p}(\omega_{\mathrm{LO}})} \tag{4.11}$$

Where $Z_s=R_{\mathrm{s}}||(j\omega_{\mathrm{LO}}\mathrm{C_s})^{-1}$ and $\mathrm{R_p}(\omega_{\mathrm{LO}})$ can be obtained from (4.9). Since the BB noise is a minor contribution as discussed in (4.8), it is neglected in (4.11).

Note that the center frequency of an N-path filter is controlled by LO, therefore the parasitic capacitance does not influence the tuning range.

4.5 Measurement Results

A test chip was fabricated in 1P7M TSMC 28 nm technology and packaged in a 3x3 QFN package. The total chip area including pads and decoupling capacitors is 1 mm^2 while the active area is 0.8 mm^2. Fig. 4.10 shows the chip micrograph. The external differential clock is applied from the top side, while the RF input-signal is applied from the bottom to reduce

coupling. An off-chip 10-8000 MHz 1:1 transformer (Mini-Circuits TCM1-83X+) serves as balun for single-to-differential conversion, while also providing impedance matching to the 50-Ω differential chip input. Both the balun and cable losses were de-embedded for all measurements except the S_{11} measurement.

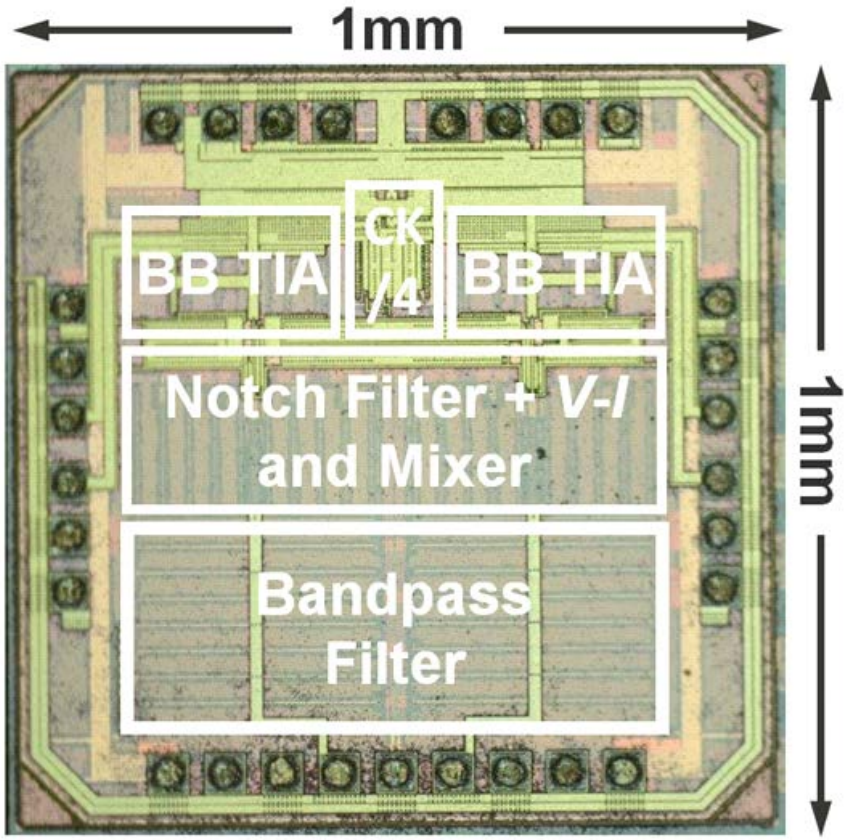


Fig. 4.10: Chip microphotograph.

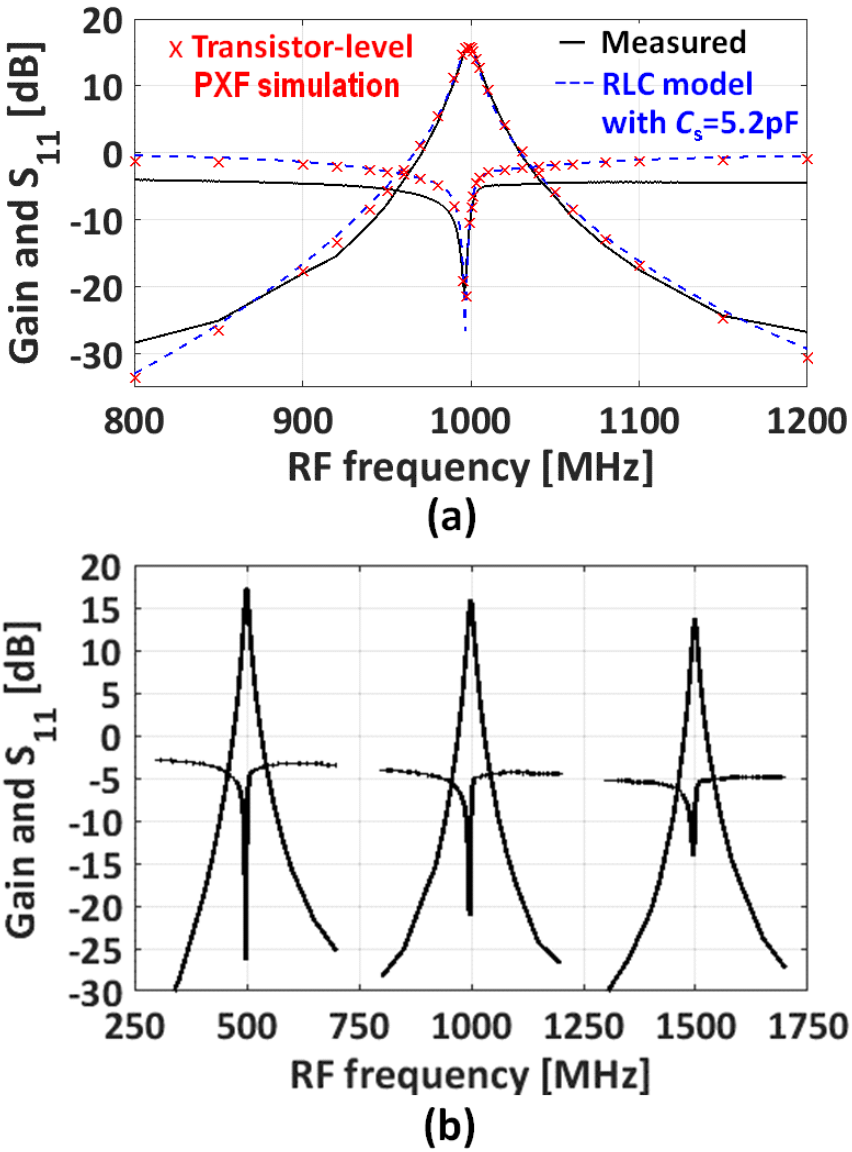


Fig. 4.11: Measured and simulated gain and S_{11} vs. RF frequency (f_{LO} = 1 GHz), (b) Measured gain and S_{11} for three LO frequencies.

4.5.1 Gain and S_{11}

Because the BB amplifier is not able to directly drive a 50-Ω load, a low noise external measurement buffer (TELEDYNE LECROY AP033 Active Differential Probe) with differential high-impedance input and single-ended 50-Ω output impedance was added. A weak tone of −50 dBm is applied to the RF input and the BB output is observed to obtain the conversion gain. Fig. 4.11(a) shows the measured voltage gain and S_{11} as a function of the RF input frequency for a 1-GHz LO. To compare measurement to theory, the RLC model in Fig. 4.8(b) was used and a shunt C_s of 5.2 pF is added to the RF input. Applying Eqn. (4.9), $R_p(\omega_{LO})$ becomes 30 Ω. The single ended input impedance of this receiver $R_{in}(\omega_{LO})$ is $R_p(\omega_{LO})||(R_{VI} + R_{sw} + 2\gamma R_{BB})$, it becomes ≈50 Ω differentially. The receiver conversion gain obtained from the RLC model can be computed by using (4.6) and (4.7), while R_p of (4.6) becomes $R_p(\omega_{LO})||(j\omega C_s)^{-1}$ now. It is observed that both the gain and optimum S_{11} dip are shifted towards lower frequencies due to the presence of C_s, in agreement with the analysis in [73, 94]. This issue can be addressed by introducing complex feedback with resistors [71] or adding a series inductor [94]. The measured gain is about 16 dB and the $f_{-3dB,BPF}$ is about 13 MHz ($f_{-3dB,BB}$=6.5 MHz), while the filter roll-off from 20 to 200-MHz offset is about −32 dB (−34 dB from (4.6)) for the upper sideband, and −33 dB (−38 dB from (4.6)) for the lower sideband.

Note that the deviation between the measured S_{11} and the theoretical prediction is likely due to balun non-idealities (simulations were done with an ideal balun model). Fig. 4.11(b) shows gain and S_{11} plots over three LO different frequencies to illustrate the filter tuning capability of the receiver.

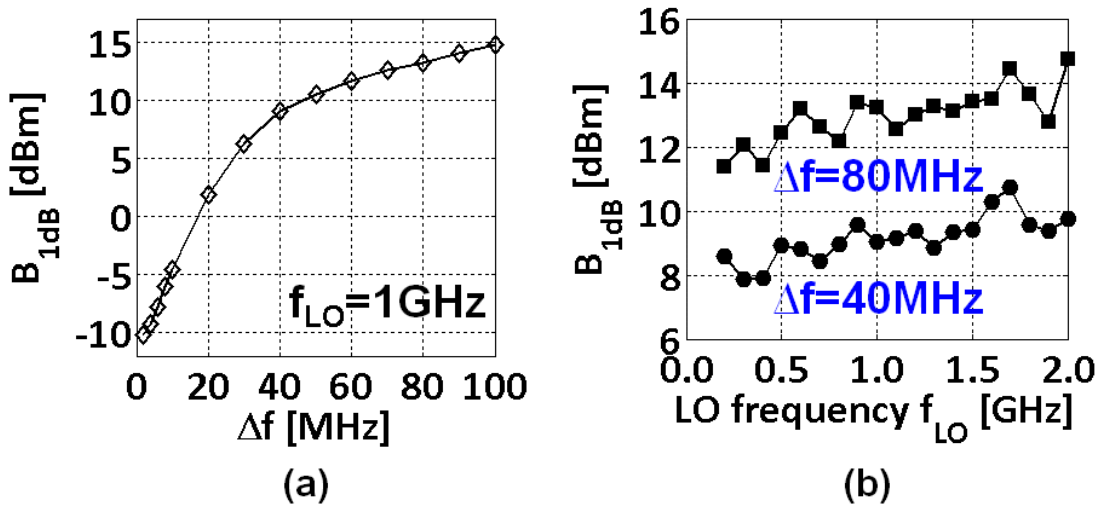


Fig. 4.12: (a) Measured B1dB versus blocker frequency offset Δf at f_{LO}=1GHz and (b) B1dB versus f_{LO} for Δf=40MHz and Δf=80MHz.

4.5.2 B1dB, IIP2 and IIP3

Fig. 4.12 shows the measured blocker 1-dB gain compression point (B1dB) as a function of frequency offset Δf from the carrier and B1dB as a function of f_{LO}. The proposed receiver achieves a high B1dB of 13 dBm for Δf =80 MHz when f_{LO} is 1 GHz.

IIP3 and IIP2 measurements are performed by two-tone tests. Circulators that offer higher than 20 dB isolation are applied between the two blocker signal generators to prevent intermodulation in the test setup, so that over +55-dBm IIP3 was achieved in the test setup itself. For LTE radio applications, the transmitter signal frequency is lower than the receiver frequency for most of the bands. Therefore, the test tones were chosen at $f_1 = f_{\mathrm{LO}} - \Delta f$ and $f_2 = f_{\mathrm{LO}} - 2\Delta f + 500$ kHz for IIP3 measurements, and at $f_1 = f_{\mathrm{LO}} - \Delta f$ and $f_2 = f_{\mathrm{LO}} - \Delta f + 500$ kHz for IIP2 measurements. This choice keeps the resulting IM3 or IM2 product at a constant BB frequency of 500 kHz. In a practical wireless communication system such as LTE, the frequency offset between TX and RX in FDD

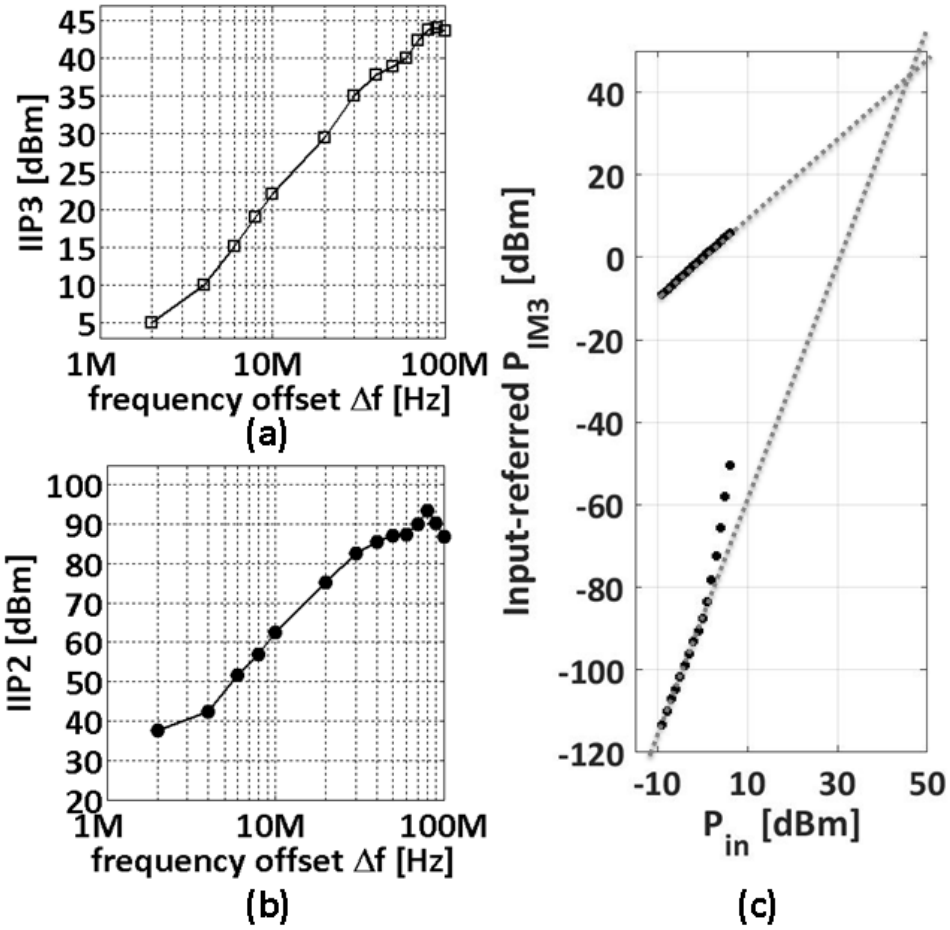


Fig. 4.13: Measured (a) IIP3, (b) IIP2 versus blocker frequency offset Δf at f_{LO}=1 GHz and (c) measured P_{IIM3} versus P_{in} for Δf=80 MHz.

mode is specified in the standard. The very high IIP3 and IIP2 is only required at this specified frequency offset Δf. Measured IIP3 and IIP2 as a function of Δf for a 1-GHz LO are shown in Fig. 4.13. At Δf=80 MHz, very high IIP3 of +44 dBm and IIP2 of +90 dBm are achieved. Fig. 4.13(c) shows the input referred IM3 as a function of the blocker power

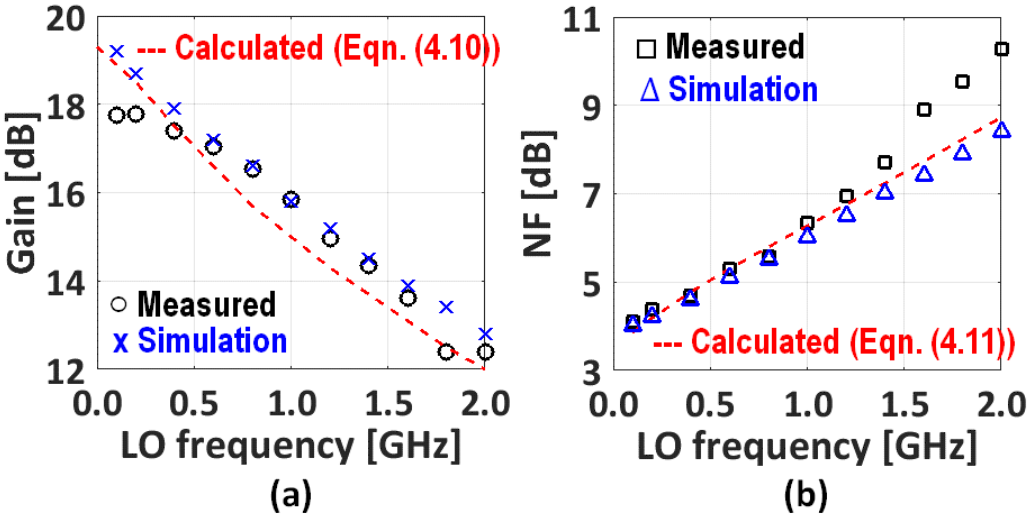


Fig. 4.14: (a) Gain and (b) DSB NF versus LO frequency.

for a 1-GHz LO and Δf=80 MHz. The measured P_{IIM3} follows the extrapolation line up to an input power as high as 0 dBm. Basically $R_{sw} << R_s$ is required to achieve such high linearity, causing large switch gate capacitance. As the required power consumption of the clocking circuit to drive switches is proportional to the clock frequency and switch gate capacitance, there is a trade-off between linearity and LO power.

In this receiver design, phase shifts in the LO between the bandpass and notch mixers will contribute to charge sharing between baseband capacitors. To investigate how it influences the linearity, we deliberately add a delay on the LO clock that drives notch filter. Simulation shows that the IIP3 variation of this receiver is kept less than 0.5 dB when the clock delay between bandpass and notch is within 5 ps. The possible charge sharing has a minor impact on the linearity.

4.5.3 NF and Gain vs LO Frequency

Fig. 4.14(a) shows the measured and transistor-level (with QRC layout extraction) simulated gain as a function of LO frequency. The gain loss at higher f_{LO} is due to input

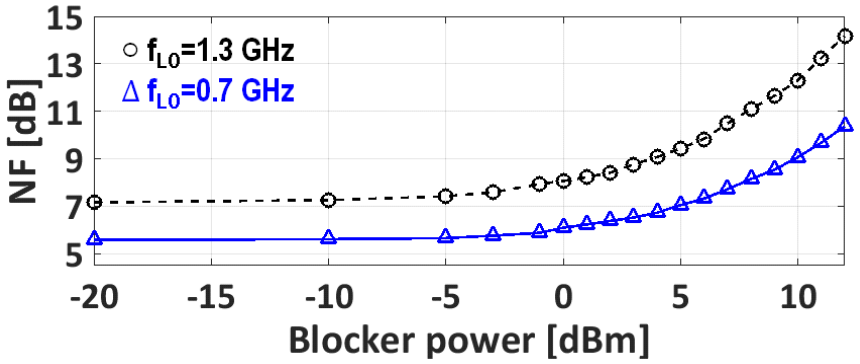


Fig. 4.15: Measured blocker NF (blocker frequency offset Δf=80 MHz) for f_{LO}=0.7 GHz and f_{LO}=1.3 GHz.

impedance reduction as a result of parasitic capacitance C_s as discussed in section 4.4.4. The measured conversion gain at a low LO frequency of 100 MHz is about 18 dB while the simulated gain is about 19 dB. This deviation is due to variation as a function of frequency in the output impedance of the on-board balun (35 Ω, instead of 50 Ω). As a result, the harmonic shunt impedance and the RF input impedance will be smaller, and the conversion gain at the RF input becomes lower.

NF measurements were performed using the Y-factor method with an external noise source. As shown in Fig. 4.14(b), at low LO frequency of 100 MHz, NF is 4.2 dB. The parasitic capacitance C_s at RF input is not taken into account in Eqn. (4.8) derived in section 4.4.3. In the practical circuit, this lowers the impedance seen by the source voltage at higher RF frequencies. Therefore, the source resistance contributes a lower percentage of the total output noise at higher frequencies and NF increases.

4.5.4 Blocker NF

Fig. 4.15 shows the measured NF as a function of blocker power for 0.7-GHz and 1.3-GHz LO-frequency, while the blocker offset was 80 MHz. The measured desensitization is only

0.6 dB for a 0-dBm blocker, and 3.5 dB for a 10-dBm blocker at 0.7 GHz LO. Overall, the presence of strong blockers degrades NF due to reciprocal mixing and gain compression. Since the measured B1dB is as high as +13 dBm, the blocker NF degradation is most likely due to reciprocal mixing which is proportional to blocker power and phase noise of LO. To obtain satisfactory measured blocker NF, two external tunable narrow-band BPFs in cascade were applied to the output of the signal generators used to supply 4xLO for ensuring low phase noise. The clocking circuit consumes about 33 mW/GHz from 1.2-V supply to achieve a simulated phase noise of −170 dBc/Hz for 1-GHz LO at 80-MHz offset frequency. As also discussed in [95], generating an LO with such strict requirements is one of the biggest challenges of passive mixing SAW-less receiver designs.

4.5.5 Performance Comparison

The performance comparison with another proposed receiver design and other blocker-tolerant RF front ends will be presented in the next chapter (Chapter 5).

4.6 Conclusion

In this thesis, a high linearity receiver combining 2-stage N-path filtering with passive mixing is proposed, analyzed, implemented and evaluated. The N-path filter is a cascade of a passive V-V and a V-I bandpass filter, enhancing selectivity. Very high linearity is achieved exploiting a bottom-plate mixing technique that improves both in-band and OOB linearity. Switch sharing further improves linearity and can offer an additional 9 dB IIP3 enhancement. Implemented in 28 nm CMOS, a High-linearity RX achieving +44-dBm IIP3, +90-dBm IIP2, +13-dBm B1dB with moderate NF of 6.3 dB at 1-GHz LO frequency is demonstrated, offering robustness to strong TX leakage.

CHAPTER 5

Enhanced-Selectivity High-Linearity Low-Noise Mixer-First Receiver with Complex Pole Pair due to Capacitive Positive Feedback

5.1 Introduction

To improve data rate and capacity, cellular phones based on the long-term evolution (LTE) standard have to support an ever increasing number of bands. For 5G, a receiver (RX) covering much of the spectrum up to 6 GHz is likely required. The mobile receivers need to deal with large out-of-band (OOB) blockers, while Frequency Division Duplex (FDD) also introduces strong self-interference from the transmitter (TX). To prevent degradation in sensitivity, off-chip high-linearity SAW filters are often adopted. However, these filters are not tunable, increase size and cost, and introduce 2-3 dB in-band loss, making multi-band 1-6 GHz support troublesome. SAW-less solutions compatible with CMOS integration are highly desired.

Antenna diversity with two antennas is widely applied in modern cellular phones to improve the quality and reliability of wireless links. Moreover, two or even more receive antennas are wanted for MIMO. In this thesis we focus on a diversity antenna receiver for a conventional FDD cellular system as shown in Fig. 5.1(a).

This chapter is a verbatim copy of the journal paper [96] except for the following changes:

1. The LTE band 5 diversity antenna path experiment of journal will now be described in detail in Chapter 6 and more analysis is given.

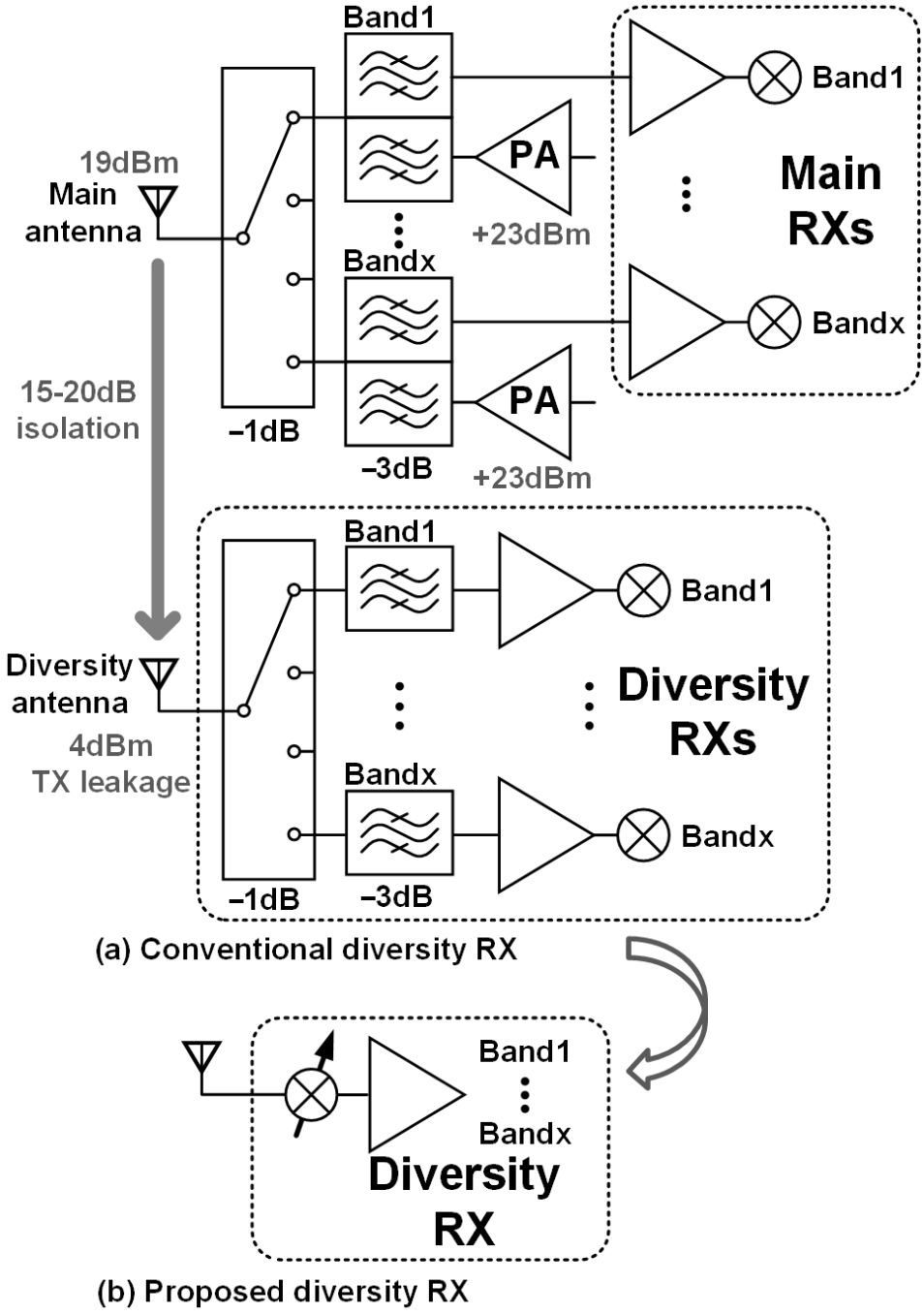


Fig. 5.1: (a) Conventional LTE receiver with external SAW filters, and (b) proposed single tunable diversity receiver without external SAW filters.

The typical TX-power is as strong as +23 dBm and there is about 15-20 dB (i.e. it is measured by using a realistic mobile phone) isolation from the main antenna to the diversity antenna. Including TX-filter and switch losses, about +19 dBm and +4 dBm TX-leakage are present at the RF input ports of the main and diversity receivers respectively. Usually SAW RX-filters (see Fig. 5.1(a)) provide TX-RX isolation to relax the RX-linearity requirements to a feasible level. Targeting more integration, recent work shows that passive switch-capacitor N-path filtering with tunable center frequency in mixer-first receivers can achieve >10 dBm blocker 1-dB compression point (B1dB) and good IIP3 of 20-30 dBm [71, 82, 83]. This shows promise to remove the off-chip SAW filters in the diversity receiver and also reduce the number of diversity receivers to a single one, as shown in Fig. 5.1(b). This paper explores the feasibility of such a receiver in CMOS.

In a FDD system, cross-modulation due to TX leakage and an in-band continuous-wave (CW) blocker deteriorates RX sensitivity, which can be related to an IIP3 requirement discussed in 2.4.3: Considering Eqn. (2.9), $P_{\mathrm{cw,IB}}$ is the power of the CW blocker (typically ≈–40 dBm), P_{TX} that of the TX leakage (4 dBm), P_{XM} the power of the cross-modulation product, while the last term (=5 dB) is added to account for the modulated nature of the TX [28]. For example, the integrated thermal noise is −101 dBm for 20-MHz channel BW in an LTE receiver. If we assume the cross-modulation product is equal to the noise power, i.e. $P_{\mathrm{XM}} = -101$ dBm, the resulting required IIP3 is ≈+35 dBm, which is a challenging specification that we will try to meet.

Table 2.1 shows some examples of LTE frequency bands. A single switch-R-C N-path filter [36] or mixer-first receiver [71] performs "only" 1st order Low Pass Filtering (LPF), which is up-converted to a 2nd order Band-Pass Filter (BPF) around the switching frequency. However, this is not sufficient to deal with strong TX-leakage in case of a very small "duplex spacing" (e.g. band 5 and 8 in Table 2.1).

To enhance the selectivity and extend the linearity, a 6th order BPF was realized by cascading passive N-path filters, coupling them by transconductors g_{m} [38]. These

transconductors work at RF in open loop and have a rather limited achievable linearity of around 10-15 dBm [97]. Even with a first passive stage [38], overall linearity was limited to +25 dBm, which is >10 dB worse than the +36 dBm requirement. Also, other $g_m - C$ filter techniques, e.g. [98] achieve good selectivity but insufficient linearity. An IIP3=36 dBm was demonstrated by [29], however at boosted switch-driver supply voltage of 2 V, raising power dissipation, and introducing device reliability concerns. Recently, we proposed higher order RF filtering by cascading two passive BPF stages [90], while a "Bottom-plate mixing" technique with switch sharing pushes IIP3 to +44 dBm. Unfortunately, large parasitic capacitance from MOM capacitors at the RF input introduce signal loss, and sub-3 dB noise figure (NF) was not obtained.

In this thesis we propose a different approach to enhance selectivity in a mixer-first receiver: we will exploit capacitive positive feedback to obtain a steeper filter roll-off [99], increased frequency range and enhanced linearity, while achieving a noise figure below 3 dB. Note that this is different from [82], where positive resistive (not capacitive) feedback is added to aid input impedance matching and realize sub 3-dB NF, whereas our key target is selectivity enhancement at high linearity.

5.2 Receiver Architecture

To enhance IIP3 and compression point of the entire receiver, strong OOB signals should be rejected as early as possible by steep filtering. This is what a SAW filter does, immediately at the RF-input, but as motivated in the introduction we would like a more CMOS compatible solution exploiting N-path filtering.

Fig. 5.2(a) shows a mixer-first receiver, in which capacitor C_1 is put across negative feedback amplifier $-A_0$ and interacts with source impedance R_s via a passive mixer to obtain N-path filtering [42, 67, 71, 82, 83, 99]. The resulting first order low-pass filter is frequency shifted to a 2nd order RF bandpass filter around f_{LO}. By putting C_1 across the

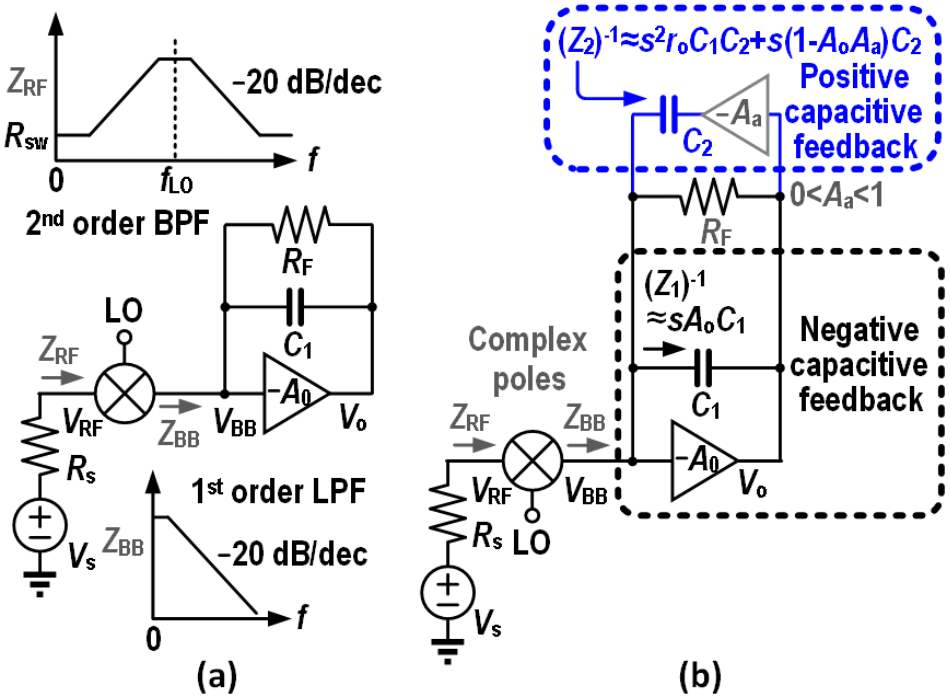


Fig. 5.2: (a) Mixer-first receiver with the BB Miller capacitor C_1; (b) The proposed receiver with extra positive capacitive feedback.

amplifier instead of to ground, the baseband (BB) capacitance "seen" by the mixer is increased due to the Miller effect by $(1 + A_0)$, saving chip area. Moreover, this Miller effect allows for low-noise impedance matching using a high R_F value [71]. A single-stage amplifier will be used, modelled as a voltage controlled current source g_m with output resistance r_o, where $A_0 = g_m r_o$. Assuming $r_o \ll R_F$, an OOB blocker is down-converted and sees a baseband conductance $(Z_{BB})^{-1} \approx (Z_1)^{-1} + (1 + A_0)/R_F$, with $(Z_1)^{-1} \approx s(1 + A_o)C_1/(1 + sr_oC_1)$. For frequencies $\ll (r_oC_1)^{-1}$ and $A_o \gg 1$, conductance $(Z_1)^{-1} \approx sA_oC_1$ offers OOB current by-passing and first order filtering.

Higher order filtering can be obtained by creating a higher order input conductance as shown in Fig. 5.2(b). A capacitive positive feedback path is added in the form of capacitor C_2, driven by the attenuated inverted BB signal, rendering:

$$(Z_2)^{-1} \approx \frac{[s^2 r_o C_1 C_2 + s(1 - A_0 A_a) C_2]}{1 + s r_o C_1} \tag{5.1}$$

where A_0 and A_a are positive numbers. The combination of negative feedback via C_1 and positive feedback via C_2 produces a 2-zero, 1-pole conductance, which can be approximated as:

$$(Z_2)^{-1} + (Z_1)^{-1} \approx \frac{[s^2 r_o C_1 C_2 + s(1 - A_0 A_a) C_2 + s A_0 C_1]}{1 + s r_o C_1} \tag{5.2}$$

By choosing a proper A_a and C_1/C_2 ratio, both zeros in Eqn. (5.2) can be located at a frequency lower than $(r_o C_1)^{-1}$, and the conductance for a blocker offset frequency $< (r_o C_1)^{-1}$ can be approximated as $s^2 r_o C_1 C_2 + s(1 - A_0 A_a) C_2 + s A_0 C_1$. This gives the approximations $(Z_2)^{-1} \approx s^2 r_o C_1 C_2 + s(1 - A_0 A_a) C_2$ and $(Z_1)^{-1} \approx s A_0 C_1$ as shown in Fig. 5.2(b).

To get more detailed insights into the proposed mixer-first RX, we assume that 4 BB-slices of the circuit of Fig. 5.2(b) are driven by 4 mixers and non-overlapping 4-phase clocks with 25% duty-cycle. The 4-phase example of proposed RX is shown in Fig. 5.3(a). We still assume that A_a is an ideal attenuator with infinite input impedance and zero output impedance. Adopting a derivation as in [88], we derived an equivalent Linear Time Invariant (LTI) model of the time variant circuit and voltage transfer functions from the RF signal V_s to the BB. The resulting LTI model for a sinewave RF-excitation is shown in Fig. 5.3(b) (note that the left part of the circuit operates at RF, and the right part at $\omega_{BB} = \omega_{RF} - \omega_{LO}$ as in [88]). The harmonic shunt impedance R_{sh} of the passive mixer is

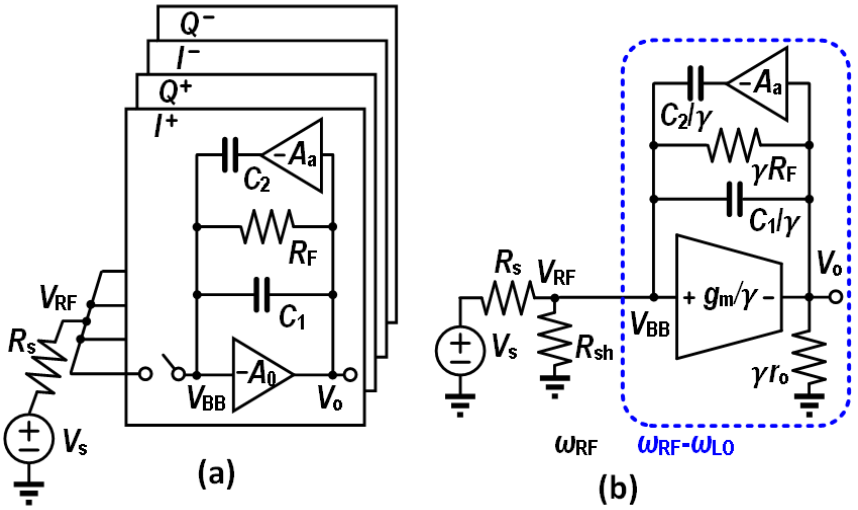


Fig. 5.3: (a) A 4-phase case of the proposed receiver and (b) the corresponding LTI model.

$4\gamma R_s/(1-4\gamma)$ [73]. Assuming ideal mixer switches, the voltage gain from V_{RF} to V_{BB} can be derived by dividing Eqn. 4 in [73] by Eqn. 6, resulting $1/\sqrt{4\gamma}$ (=0.9 dB) where γ is $2/\pi^2$ for 4-phase case. In our RX design, r_o is small because a large g_m is required for low noise. R_F is much higher than R_s, because $R_F \approx R_s(1+A_0)/(8\gamma-1)$ is needed for input matching. We first show the single-ended to single-ended voltage transfer function $H_{BB,S}(s) = V_{BB}(s)/(V_s/2)$, and its natural frequency $\omega_{0,S}$ and quality factor Q_S:

$$H_{BB,S}(s) = \frac{V_{BB}(s)}{V_s/2} \approx \frac{2\sqrt{4\gamma}((1+A_a)C_2 4R_s)^{-1}(s+1/(r_o C_1))}{s^2+\frac{\omega_{0,S}}{Q_S}s+\omega_{0,S}^2} \tag{5.3}$$

$$\omega_{0,S} \approx \sqrt{\frac{1+4g_m r_o R_s R_F^{-1}}{4(1+A_a)C_1 C_2 r_o R_s}} \tag{5.4}$$

$$Q_S \approx \frac{2\sqrt{(1+A_a)C_1 C_2 r_o R_s(1+4g_m r_o R_s R_F^{-1})}}{4C_2(1-A_a g_m r_o)R_s+C_1(r_o+4R_s+4g_m r_o R_s)} \tag{5.5}$$

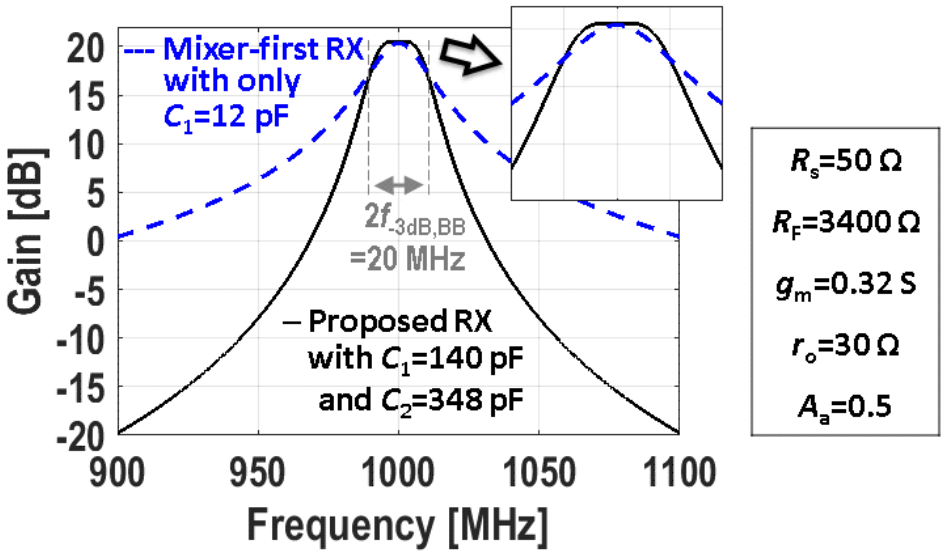


Fig. 5.4: Simulated (PXF) $V_o(s)/(V_s/2)$ for the mixer-first RX with only C_1 (dashed line) and the proposed mixer-first RX with C_1 and C_2 (solid line). C_1 and C_2 are tuned to have the same channel BW for fair comparison.

When $\omega_{BB}<1/(r_oC_1)$, $V_{BB}(s)/(V_s/2)$ is a LPF with 2-pole roll-off. As ω_{BB} increases to $1/(r_oC_1)$, this unwanted zero is introduced because Miller capacitor C_1 is no longer valid.

Next, we derive the $H_{o,S}(s) = V_o(s)/(V_s/2)$, and it can be written as:

$$H_{o,S}(s) = \frac{V_o(s)}{V_s/2} \approx \frac{2\sqrt{4\gamma}((1+A_a)C_2 4R_s)^{-1}(s-g_m/C_1)}{s^2+\frac{\omega_{0,S}}{Q_S}s+\omega_{0,S}^2} \tag{5.6}$$

The frequency of unwanted zero in $H_{o,S}(s)$ that is located at g_m/C_1 can be as high as 1 GHz if g_m is large enough. Then $H_{o,S}(s)$ effectively shows a 2-pole roll-off below g_m/C_1. Fig. 5.4 compares the filter shape of a 4-phase mixer-first receiver with a BB Miller capacitor C_1 in Fig. 5.2(a) and that of the new one with C_1 and C_2 in Fig. 5.2((b), designed

as Butterworth filter. Clearly, a more brick-wall like and also steeper RF BPF-shape and BB LPF-shape is achieved for blocker frequencies close to the RX band compared to the "round shape" when cascading real poles.

We see that the combination of the new positive feedback path via C_2 combined with the negative feedback path via C_1 can establish a complex pole-pair allowing to improve selectivity.

The quality factor Q is adjustable by changing the ratio of C_1 and C_2. Note that both BB capacitive feedback paths can have *high linearity as well as low noise, in contrast to open loop* g_m *blocks*. Before we analyze the practical circuit with *non-ideal attenuator* A_a in depth, we describe the actual circuit implementation in some more detail.

5.3 Circuit Implementation

Fig. 5.5 shows a detailed schematic of the proposed zero-IF receiver. It was designed for $f_{-3\mathrm{dB,BB}}$=10 MHz to support an RF channel bandwidth of 20 MHz for LTE applications. The passive mixer MOS-switches are driven by quadrature 4-phase 25% duty-cycle clocks, provided by a divide-by-2 circuit. Parasitic capacitance at the RF input causes the frequency of optimum S_{11} to shift towards lower frequencies than f_LO, which was compensated by complex feedback via R_FIQ [71].

5.3.1 Enhanced Selectivity Receiver Circuit Realization

Due to the differential architecture, the negative gain $-A_\mathrm{a}$ for the attenuator in Fig. 5.5 can simply be implemented by wire-crossing, while low-ohmic passive resistors R_a1 and R_a2 realize a high-linearity attenuator with A_a =0.5. In section 5.4 we will see that this hardly degrades NF. As C_2 serves as OOB blocker bypassing path, low OOB impedance of the attenuator is important to maintain good blocker rejection. For this purpose capacitor

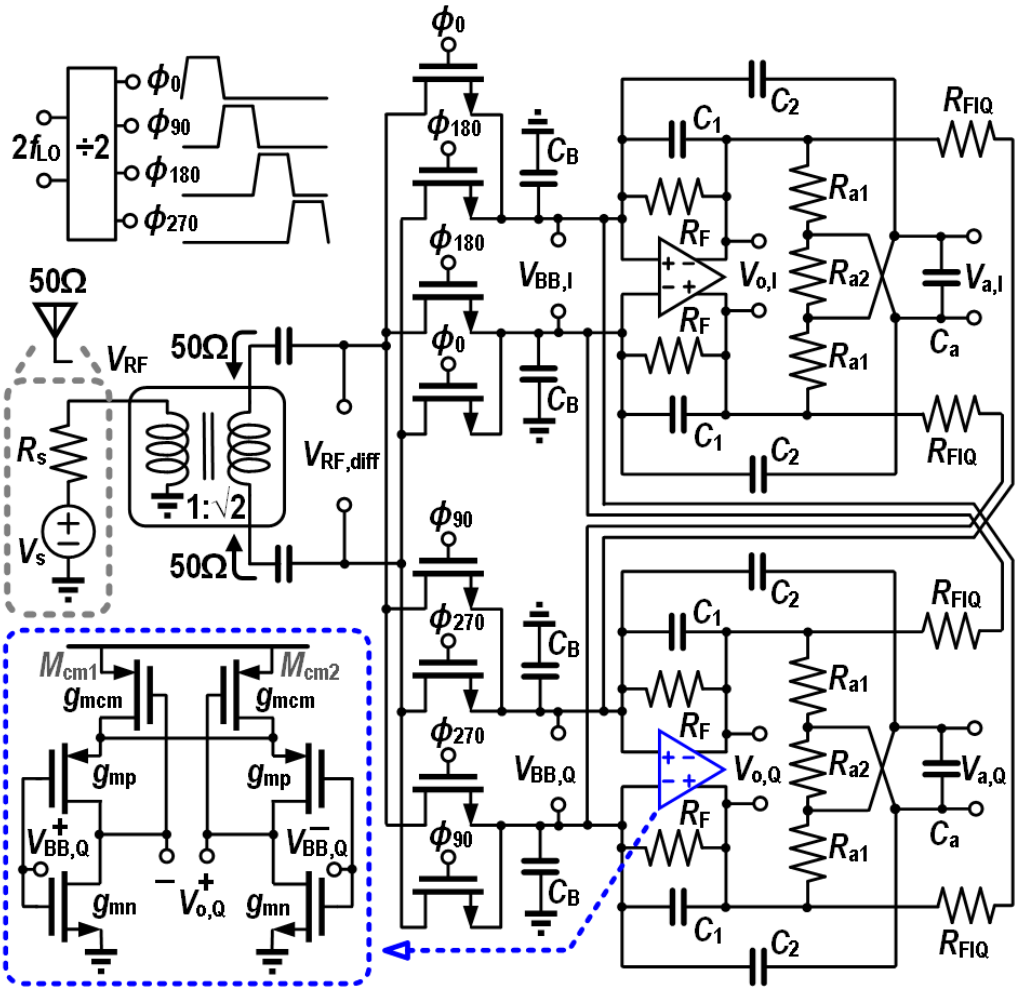


Fig. 5.5: Circuit details of the proposed receiver and low noise BB amplifier.

C_a is added, providing a high linearity purely capacitive signal path shunting the BB-input directly (see Fig. 5.5). The filter bandwidth is mainly determined by R_s, C_1 and C_2, as will be derived in section 5.4, and Q is designed about 0.7 to realize Butterworth filtering. Capacitor C_B also provides a direct blocker bypassing path to ground but plays a minor role in this design, as the TIA-input impedance is low-ohmic over a wide band due to the high g_m value used in this design (see 5.3.2).

5.3.2 Low Noise BB Amplifier

In the mixer-first receiver, low noise in the first BB amplifier stage is an important requirement to achieve sub-3 dB receiver NF. Inverter-based amplifiers [60, 93] offer large g_m with good power efficiency, while loop stability is of little concern in a single-stage amplifier. Fig. 5.5 shows the schematic of the BB amplifier also used in [90]. A higher threshold voltage V_{th} for M_{cm1} and M_{cm2}, combined with a small overdrive voltage of the PMOS input differential pair ensures all transistors operate in their saturation region. The resistive attenuator in parallel to the MOS output resistance r_{on} and r_{op} linearizes the output impedance of the BB amplifier. For a differential input signal, a high gain of $\approx (g_{mn} + g_{mp})(r_{on}\|r_{op})$≈22 dB is achieved. For a pure common mode input, the voltage-gain g_{mn}/g_{mcm} is kept low as 5 dB. To avoid the kink or history effect in partially depleted SOI-MOS transistors [100], the BB amplifiers were built by body contacted devices, while mixer switches and digital clock generator devices are implemented as floating body devices. The dimensions of PMOS and NMOS input pairs are 3600 um/0.112 um and 1600 um/0.112 um respectively, achieving a large g_m of 360 mS and an output impedance $r_o = r_{on}\|r_{op}$=36 Ω. The simulated flicker noise corner frequency is about 50 kHz, and the open loop bandwidth is about 340 MHz for a 10-pF loading capacitance.

5.4 Circuit Analysis

In this section we will analyze different properties of the mixer-first receiver, like transfer function, loop stability, linearity, noise and input impedance.

5.4.1 Transfer Function Analysis

Using a similar derivation as in [88], we derived voltage transfer functions from $V_{\rm s}$ to $V_{\rm BB,diff}$, $V_{\rm o,diff}$ and $V_{\rm a,diff}$ in Fig. 5.6. However, in contrast to a single balanced mixer, we

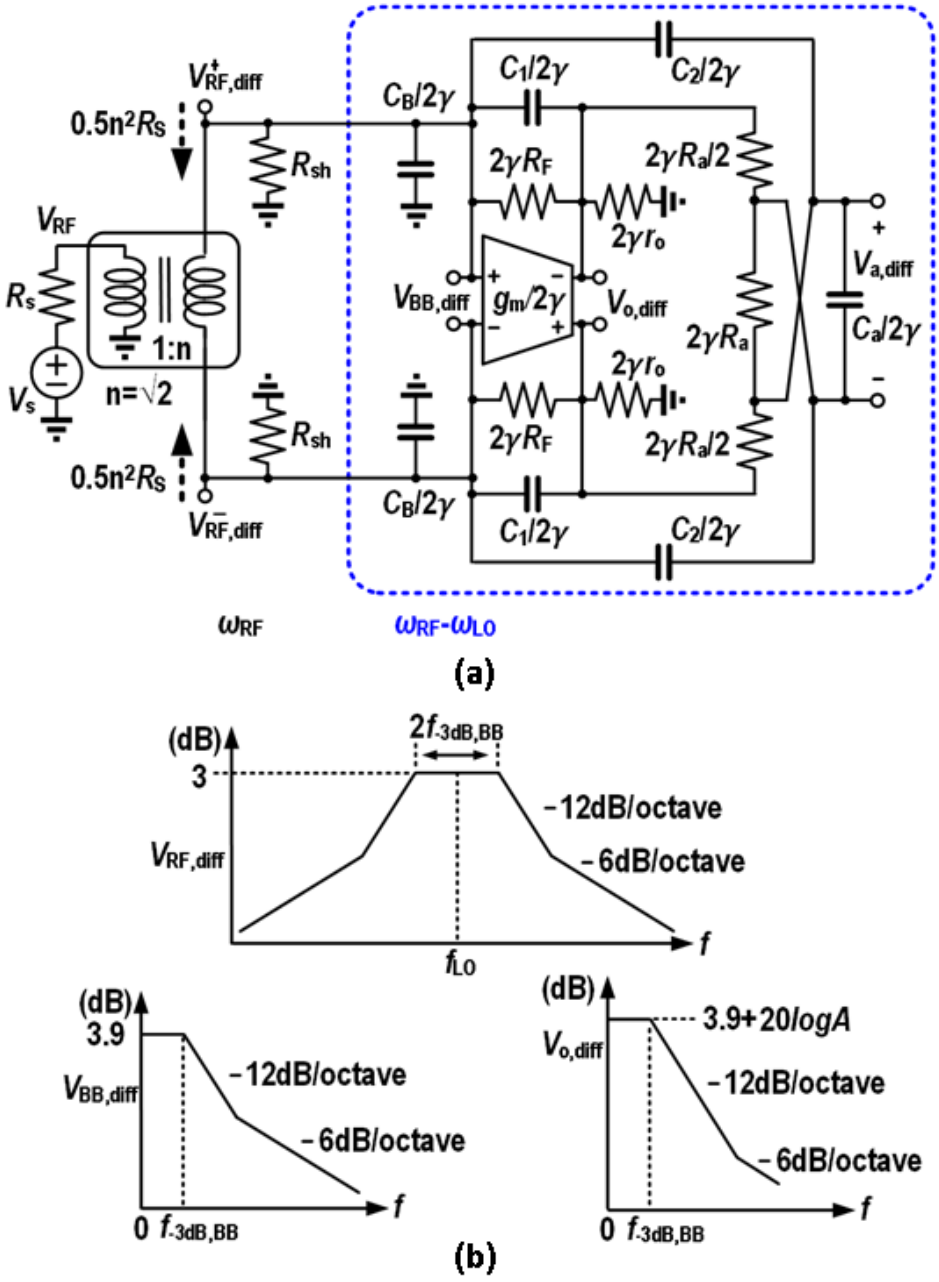


Fig. 5.6: (a) Equivalent LTI model of this receiver, (b) simplified plots for $V_{\mathrm{RF,diff}}$, $V_{\mathrm{BB,diff}}$ and $V_{\mathrm{o,diff}}$.

use a double-balanced mixer. Now each of the baseband components is connected twice per period to the RF source, doubling the conduction time, compared to the single-end case. This leads to an equivalent LTI model with extra factors 2 as given in Fig. 5.6(a). The transformer with 1:n turns ratio performs single to differential conversion. In this design, it is n=$\sqrt{2}$ and impedance ration is 1:2. To reduce equation complexity, we assume $2R_{\mathrm{a1}} = R_{\mathrm{a2}} = R_{\mathrm{a}}$ and neglect the minor effect of C_{B}. The pole and zero located at frequency higher than 500 MHz are also neglected. We derived $H_{\mathrm{o}}(s) = V_{\mathrm{o,diff}}(s)/(V_{\mathrm{s}}/2)$, its natural frequency ω_0 of the pole-pair and quality factor Q as shown in Eqn. (5.7-5.9). Since we consider now the finite gain of the BB amplifier, the equation becomes more complex than a normal biquad transfer function. The resistive attenuator A_{a} instead of the

$$H_{\mathrm{o}}(s) = \frac{V_{\mathrm{o,diff}}(s)}{V_{\mathrm{s}}/2}$$

$$\approx -2\sqrt{2}\sqrt{4\gamma}\,\frac{2R_{\mathrm{F}}/(1+g_{\mathrm{m}}(r_{\mathrm{o}}^{-1}+R_{\mathrm{a}}^{-1}+R_{\mathrm{F}}^{-1})^{-1})}{4R_{\mathrm{s}}+2R_{\mathrm{F}}/(1+g_{\mathrm{m}}(r_{\mathrm{o}}^{-1}+R_{\mathrm{a}}^{-1}+R_{\mathrm{F}}^{-1})^{-1})}\,\frac{g_{\mathrm{m}}(r_{\mathrm{o}}^{-1}+R_{\mathrm{a}}^{-1}+R_{\mathrm{F}}^{-1})^{-1}\omega_0^2(0.5R_{\mathrm{a}}C_{\mathrm{a}}s+1)}{s^2+\frac{\omega_0}{Q}s+\omega_0^2} \tag{5.7}$$

$$\omega_0^2 \approx \frac{2(r_{\mathrm{o}}(R_{\mathrm{F}}+2R_s)+R_{\mathrm{a}}(R_{\mathrm{F}}+r_{\mathrm{o}}+2R_{\mathrm{s}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}))}{R_{\mathrm{a}}(C_2C_{\mathrm{a}}(2R_{\mathrm{F}}r_{\mathrm{o}}+R_{\mathrm{a}}(R_{\mathrm{F}}+r_{\mathrm{o}}))2R_{\mathrm{s}}+C_1R_{\mathrm{F}}(6C_2r_{\mathrm{o}}R_{\mathrm{s}}+C_{\mathrm{a}}(4r_{\mathrm{o}}R_{\mathrm{s}}+R_{\mathrm{a}}(r_{\mathrm{o}}+2R_{\mathrm{s}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}))))} \tag{5.8}$$

$$Q \approx \frac{\sqrt{(r_{\mathrm{o}}R_{\mathrm{F}}+R_{\mathrm{a}}(R_{\mathrm{F}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}))2R_{\mathrm{a}}\left(C_2C_{\mathrm{a}}(2R_{\mathrm{F}}r_{\mathrm{o}}+R_{\mathrm{a}}R_{\mathrm{F}})2R_{\mathrm{s}}+C_1R_{\mathrm{F}}(6C_2r_{\mathrm{o}}R_{\mathrm{s}}+4C_{\mathrm{a}}r_{\mathrm{o}}R_{\mathrm{s}}+2C_{\mathrm{a}}R_{\mathrm{a}}g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}})\right)}}{C_2(3R_{\mathrm{a}}r_{\mathrm{o}}+2R_{\mathrm{F}}r_{\mathrm{o}}+R_{\mathrm{a}}R_{\mathrm{F}}(2-g_{\mathrm{m}}r_{\mathrm{o}}))2R_{\mathrm{s}}+2C_1R_{\mathrm{F}}(2r_{\mathrm{o}}R_{\mathrm{s}}+R_{\mathrm{a}}(r_{\mathrm{o}}+2R_{\mathrm{s}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}))+C_{\mathrm{a}}R_{\mathrm{a}}(2r_{\mathrm{o}}R_{\mathrm{F}}+R_{\mathrm{a}}(R_{\mathrm{F}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}))} \tag{5.9}$$

C_1=60 pF	C_a=120 pF	R_F=1600 Ω	r_o=36 Ω
C_2=106 pF	C_B=20 pF	R_a=90 Ω	g_m=0.36 S

TABLE 5.1: COMPONENT VALUES FOR FIG. 5.6

uni-lateral block $-A_a$ induces an unwanted left half s-plane zero located at $(0.5R_aC_a)^{-1}$. It can be moved to higher frequency by using smaller attenuator resistance or C_a.

Filling in the component values listed in Table 5.1, we find: $\omega_0/2\pi$ =9.5 MHz, and a zero at 31 MHz. At ω_0, the amplitude of $H_o(s)$ is $Q \cdot V_{o,diff}(0)/(V_s/2)$ so for a Butterworth filter $Q \approx 0.7$, $\omega_0 = \omega_{BB,-3dB}$. The simplified asymptotic plots of the transfer function to $V_{RF,diff}$, $V_{BB,diff}$ and $V_{o,diff}$ are shown in Fig. 5.6(b). The BB resistance $R_F/(1 + A)$ is up-converted and becomes $2\gamma R_F/(1 + A)$ at the RF input, where $\gamma = 2/\pi^2$ for the 4-path case [73] and A is $g_m(r_o||R_a||R_F)$. The up-converted BB resistance is in parallel with the harmonic shunt impedance $R_{sh} = (0.5n^2R_s)4\gamma/(1 - 4\gamma)$ of the passive mixer [73], where n is turns ratio of the transformer. The combined input impedance around the LO frequency is $R_{sh}||2\gamma R_F/(1 + A)$ which is designed to provide 50-ohm matching. If there is in-band matching, in-band $V_{RF}/(V_s/2)$ is 0 dB. Due to energy conservation, $V_{RF,diff}/V_{RF}$ after the 1:$\sqrt{2}$ balun (100-Ω differentially) becomes +3 dB. The in-band voltage gain $V_{BB,diff}/V_{RF}$ is $\sqrt{2}(\sqrt{4\gamma})^{-1}$ corresponding to 3.9 dB. At the output of the BB amplifier $V_{o,diff}$, it is 3.9+$20logA$ dB. For frequencies close to in-band, the roll-off is –12 dB/octave. The output RC of the attenuator introduces a zero at 31 MHz and hence the slope degrades to –6 dB/octave far out. Still, this steep roll-off part allows for better selectivity close to the desired band. Compared to the mixer-first receiver with only Miller capacitor C_1, simulations indeed show about 10 dB improvement in OOB IIP3 for the same mixer switch size, channel bandwidth and BB amplifier gain.

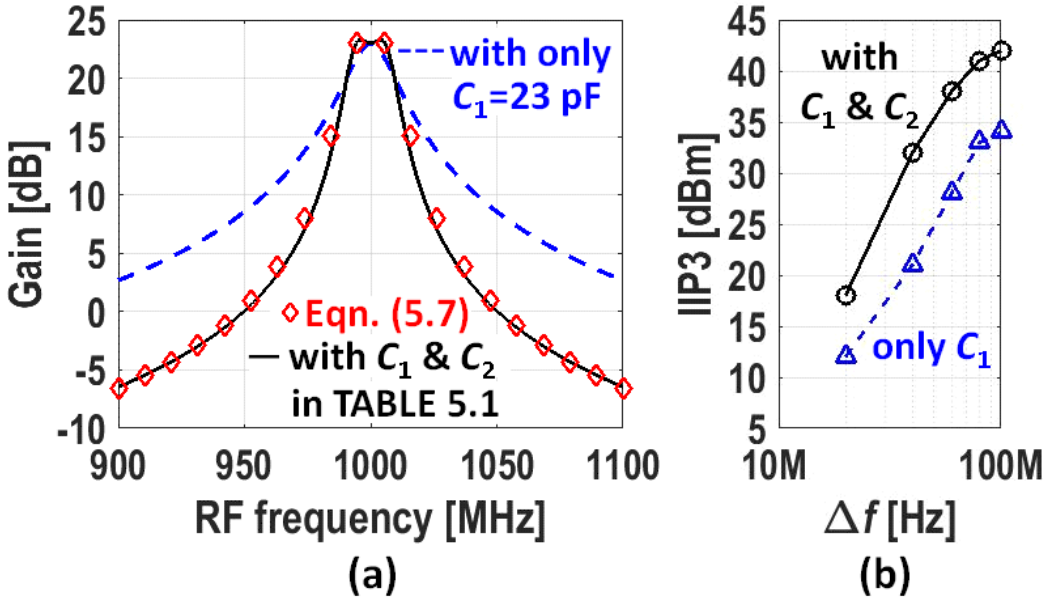


Fig. 5.7: (a) Simulated (PXF) and calculated (Eqn. (5.7)) gain ($V_{o,diff}(0)/(V_s/2)$) as a function of the RF frequency for the proposed mixer-first RX with C_1 and C_2 (solid line) and with only C_1 (dashed line). (b) IIP3 simulation result for the same two cases.

To verify analysis, Fig. 5.7(a) shows Spectre PSS PXF simulation results for the receiver circuit schematic with ideal components. About 8.0 dB more OOB rejection at 45 MHz duplex offset frequency (e.g. LTE band 5) is found. The calculated transfer function (Eqn. (5.7)) is also provided, where the BB frequency is shifted to the corresponding RF frequency and mixer conversion gain is taken into account. It shows a good fit with PSS simulations.

The IIP3 simulation results with transistor level BSIM models are provided in Fig. 5.7(b) to demonstrate that the extra filtering also results in extra overall IIP3 improvement. Since we experienced convergence issues using PSS simulations and there are effects of the discontinuity in the BSIM model, transient simulations with high accuracy settings and

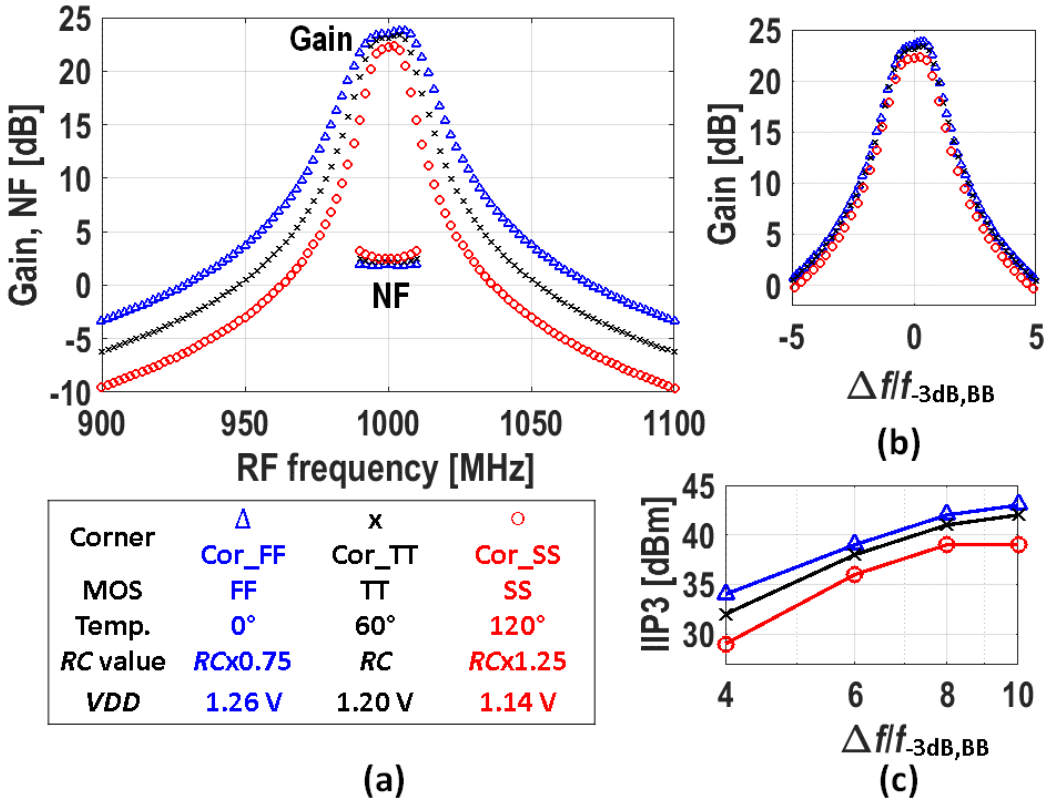


Fig. 5.8: The PVT corner simulation results for (a) transfer function $V_{o,diff}(0)/(V_s/2)$, NF, (b) redrawn transfer function as a function of normalized frequency axis and (c) IIP3.

sufficiently high input power (–10 dBm to +5 dBm) were applied to evaluate the IIP3. Intuitively this makes sense, as the part of the waveform defined by the discontinuity becomes a smaller fraction of the total waveform. Overall, we found then a reasonable match (within 2-3 dB difference) between simulation and measurement.

The process, voltage and temperature (PVT) variation simulation results for transfer function, NF and IIP3 are shown in Fig. 5.8. The BPF bandwidth or ω_0 is controlled by RC value. The ‘’filter shape’’ is determined by quality factor Q which is a function of R-to-R and C-to-C ratios, hence it is insensitive to PVT variations. The

frequency axis of Fig. 5.8(a) is shifted to BB frequency and normalized to $f_{-3\mathrm{dB,BB}}$. The RX transfer functions are redrawn and shown in Fig. 5.8(b) to confirm the robustness of RX selectivity against PVT variations. The simulated IIP3 as a function of relative frequency offset in Fig. 5.8(c) is kept within ≈3 dB variations while compared to the typical corner.

5.4.2 Receiver Loop Stability

Positive feedback may introduce stability problems, so we will now analyse the feedback system loop gain $H_{\mathrm{l,diff}}(s)$, i.e.:

$$H_{\mathrm{l,diff}}(s) = [-A(s)\,] \cdot [-A_{\mathrm{a}}(s)] \cdot \beta(s) \tag{5.10}$$

As the resistance of the attenuator is higher than r_{o}, the gain of the amplifier can be approximated as $A(s)\approx A_0/(1+sr_{\mathrm{o}}C_1)$. The frequency dependent gain of attenuator can be approximated as $A_{\mathrm{a}}(s) \approx A_{\mathrm{a}}/(1+s(R_{\mathrm{a1}}||0.5R_{\mathrm{a2}})(2C_{\mathrm{a}}+C_2))$. It is a low pass function and $A_{\mathrm{a}} = 1/2$. Applying the Miller approximation, the feedback factor from attenuator output to the BB amplifier input is $\beta(s) \approx s(C_2/C_1)/((R_{\mathrm{s}}||(A_0^{-1}R_{\mathrm{F}})C_1)^{-1} + \mathrm{s}(C_2/C_1+1+A_0))$, which is a high-pass function. The positive loop gain $H_{\mathrm{l,diff}}(s)$ should be kept well below 0 dB to guarantee loop stability. At very low frequency, C_2 provides a high impedance and $\beta(0)\approx 0$, so that $H_{\mathrm{l,diff}}(0)\approx 0$. For increasing frequency, the impedance of C_1 and C_2 becomes lower resulting in lower $A_0(s)$ and lower $A_{\mathrm{a}}(s)$ but higher $\beta(s)$. In this receiver design, $C_2\approx 2C_1$, resulting in $H_{\mathrm{l,diff}}(s) < A_0A_{\mathrm{a}}(C_2/C_1)/(C_2/C_1+1+A_0) = A_0/(3+A_0) < 1$ for all frequencies. The resistive attenuator occupies a rather large area of 20 um x 40 um to prevent linearity degradation due to the voltage coefficient of poly resistors, which also results in a good matching and an accurate resistor

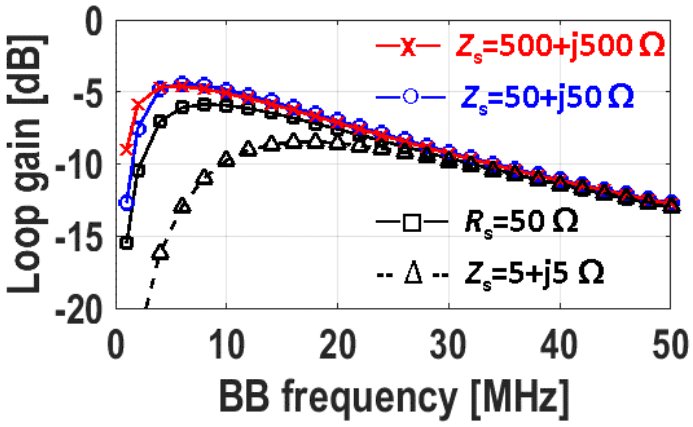


Fig. 5.9: Simulated differential loop gain for different antenna impedance Z_s.

ratio A_a. Capacitance C_1 and C_2 are large, so C_2/C_1 is also precise. The open loop gain of the BB amplifier A_0 suffers more from process variation, but largely cancels in the ratio $A_0/(3+A_0)$ and reliably gives a value below 1. Therefore loop stability is insensitive to PVT variations. Transistor-level Spectre PSS PSTB loop stability simulation shows $H_{l,diff}(s)$ is <–6 dB for different transistor, *R*, *C*, voltage and temperature corners. The antenna impedance may change with user proximity in a mobile phone and the antenna impedance Z_s may become more resistive and inductive [101]. Further analysis indicates that the proposed receiver remains stable for different passive complex values of Z_s. As shown in Fig. 5.9, the simulated differential loop gain shows a BPF profile as predicted in Eqn. (5.10), and is kept well below –4 dB (<0 dB for stable) for all frequencies even though there is 10x Z_s variation. For common mode signals, the wire-crossing no longer results in a minus sign, and it becomes positive and unity gain. As a result, Eqn. (5.10) changes to:

$$H_{l,CM}(s) \approx \frac{-A_{0,CM}}{1+sr_oC_1} \frac{sC_2/C_1}{((R_s||(A_0^{-1}R_F)C_1)^{-1}+s(C_2/C_1+1+A_0))} \quad (5.11)$$

Hence the common mode loop gain $H_{\mathrm{l,CM}}(s)$ turns out to be negative feedback, in contrast to the differential loop gain $H_{\mathrm{l,diff}}(s)$. Also the single stage BB amplifier (single pole) is designed to have a low common-mode gain resulting in $|H_{\mathrm{l,CM}}(s)| < 1$. Hence, there is no common-mode loop stability concern.

5.4.3 OOB Linearity and OOB Rejection

The NMOS mixer switches suffer from modulated V_{GS} and V_{DS} that degrade the linearity of a mixer-first receiver. Assuming $\rho = R_{\mathrm{sw}}/R_{\mathrm{s}} << 1$ (e.g. $\rho < 0.1$) to achieve high linearity, in-band matching is mainly realized by R_{F}. For in-band, the V_{GS} modulation is $\approx 0.5V_{\mathrm{A}}$ and V_{DS} modulation is $\approx 0.5V_{\mathrm{A}}R_{\mathrm{sw}}/R_{\mathrm{s}}$ where V_{A} is the amplitude of the antenna source voltage. The in-band linearity of a mixer is dominated by large V_{GS} modulation. When the blocker offset frequency from the LO increases, V_{GS} modulation is reduced due to filtering. But V_{DS} modulation is slightly increased as the OOB current is higher than in-band. When the blocker is very far away from the LO frequency, the source terminal voltage swing of the mixer switch becomes almost zero, i.e. V_{GS} modulation ≈0. The modulated V_{DS} is $\approx V_{\mathrm{A}}R_{\mathrm{sw}}/R_{\mathrm{s}}$ and dominates the OOB linearity. The far OOB IIP3 can be estimated as [88]:

$$V_{\mathrm{IIP3}} = \sqrt{\frac{4}{3}\frac{(1+\rho)^4}{\rho^3(2g_2^2 - g_3(1+\rho))}} \tag{5.12}$$

Where g_2 is $-(2V_{\mathrm{OD}})^{-1}$ and $g_3 = -(2V_{\mathrm{SAT}}^2)^{-1}$. V_{OD} is overdrive voltage and V_{SAT} is velocity saturation voltage respectively [88]. When the blockers are close to the LO frequency, the proposed mixer-first receiver with enhanced RF selectivity achieves better OOB rejection and better linearity as the simulation results in Fig. 5.7 show.

To obtain extremely high OOB IIP3 of almost +40 dBm, high OOB linearity as well as high OOB rejection for both the mixer and the low noise BB amplifiers are demanded. The

maximum OOB rejection of a mixer-first receiver with a BB Miller capacitor that is shown in Fig. 5.2(a) is limited to $\approx g_{\mathrm{m}}^{-1}/R_{\mathrm{s}}$ at the input of the BB amplifier. The OOB rejection can be extended by adding a capacitor C_{B} to ground [42, 71]. However, for the same BW a much larger capacitance area is required compared to C_1. Normally, there is a design trade-off between linearity and maximum OOB rejection. The gain of the BB amplifier as a function of frequency can be expressed as $A_{\mathrm{o}}/(1 + A_{\mathrm{o}}\beta(s))$. The Miller capacitor C_1 across the amplifier increases the feedback factor $\beta(s)$ and improves the linearity of the BB amplifier at higher frequencies [20], while a BB amplifier without Miller capacitor becomes linearity constraint in [42]. A high supply voltage of the BB amplifier can also result in better linearity [71], but consumes more power. Apart from the linearizing effect of the Miller capacitance, the output impedance of the BB amplifier is linearized by shunting it with the resistive attenuator. By adding C_{a} we also directly shunt the BB amplifier input, avoiding the limited OOB rejection due to the finite g_{m} of BB amplifier. In the proposed mixer-first receiver design, the maximum OOB rejection of the BB amplifier is improved compared to the mixer-first RX with BB Miller capacitors in Fig. 5.2(a) and the linearity of the BB amplifier is improved compared to [42, 71].

5.4.4 Noise Performance

The noise factor F of the receiver can be calculated as the total output noise divided by the noise contribution due to the thermal noise from the antenna or signal source, modelled as $\overline{v_{n,s}^2} = 4kTR_s$. The resulting F of this RX can be written as:

$$F = 1 + \frac{R_{sw}}{R_s} + \frac{(R_s+R_{sw})}{4.3R_s} + \frac{(R_s+R_{sw})^2}{\gamma(2R_F)R_s} + \frac{\overline{v_{n,in,A}^2}(4(R_s+R_{sw})+2R_{BB})^2}{4kTR_s 4\gamma(2R_{BB})^2} + \frac{(r_o||R_a)^2(4(R_s+R_{sw})+2R_{BB})^2}{A^2R_aR_s4\gamma(2R_{BB})^2} \quad (5.13)$$

The direct noise contribution from thermal noise of the mixer switch resistance which is in series with the source is R_{sw}/R_s. Moreover, noise degradation due to noise folding from odd harmonics of the mixer frequency occurs. Thermal noise of R_s and R_{sw} are hence down converted [73], leading to a summation of $4kT(R_s + R_{sw})/n^2$ terms, where $n = 3, 5, 7, \ldots$ for a 4-path mixer. This sums up to $\approx 4kT(R_s + R_{sw})/4.3$. The up-converted noise current induced by the BB feedback resistor R_F renders the term proportional to $1/(2\gamma R_F)$, where γ is the scaling factor from [73] discussed in sub-section 5.4.1. Note that R_F is designed to provide 50 ohm matching, but it is much higher than R_s primarily due to the Miller effect. Therefore the noise contribution of R_F is minor and it increases F by about only 0.08 in this design. The input-referred noise of the BB amplifiers $\overline{v_{n,in,A}^2}$ is $\overline{v_{n,out,A}^2}/A^2$, where $A = g_m(r_o||R_a||R_F)$ and $\overline{v_{n,out,A}^2}$ is noise at the BB amplifier output. The noise voltage due to source resistance at the BB amplifier input undergoes a voltage division with gain of $\sqrt{4\gamma}$ and it is $\overline{v_{n,s,BB}^2} = 4kTR_s(4\gamma)(2R_{BB}/(4(R_s + R_{sw}) + 2R_{BB}))^2$, where R_{BB} is $R_F/(1 + A)$. The BB amplifier generates $\sqrt{(\overline{v_{n,out,A}^2})} = 1400\, pV/\sqrt{Hz}$, and the $\overline{v_{n,in,A}^2}/\overline{v_{n,s,BB}^2}$ is low as 0.1 in this design. The last term in Eqn. (5.13) comes from the resistive attenuator. The noise voltage is $\overline{v_{n,att}^2} = 4kT(r_o||R_a)^2/R_a$ where r_o is the output impedance of the MOS transistors. This contribution to *F* is only 0.006.

Eqn. (5.13) indicates that this RX design can achieve a NF of 1.6 dB ($F = 1.46$) at low frequency with $R_{sw} = 1.1\ \Omega$, where the harmonic folding term is the dominant one.

5.4.5 Influence of Parasitic Capacitance at the RF Input Port

In a mixer-first receiver or N-path filter, the optimum S_{11} (dip in S_{11}) should be at ω_{LO}. However, the parasitic capacitance C_p from the mixer switches, RF input pads and tracks is in parallel with $R_{in}(\omega_{LO}) = R_{sh}(\omega_{LO})||(\gamma 2R_{BB})$, causing the frequency of optimum S_{11}

to shift towards frequencies lower than ω_{LO}. The total C_{p} is about 1 pF in this receiver design. Assuming that $R_{\mathrm{s}} \gg R_{\mathrm{sw}}$, the input impedance around ω_{LO} becomes:

$$R_{\mathrm{in}}(\omega_{\mathrm{LO}})||(j\omega_{\mathrm{LO}}C_{\mathrm{p}})^{-1}$$

$$= \frac{(R_{\mathrm{sh}}(\omega_{\mathrm{LO}})||\gamma 2R_{\mathrm{BB}})(1-j\omega_{LO}(R_{\mathrm{sh}}(\omega_{\mathrm{LO}})||\gamma 2R_{\mathrm{BB}})C_{\mathrm{p}})}{1+(\omega_{\mathrm{LO}}(R_{\mathrm{sh}}(\omega_{\mathrm{LO}})||\gamma 2R_{\mathrm{BB}})C_{\mathrm{p}})^{2}} \tag{5.14}$$

Note that this is not a purely resistive impedance, but also contains a negative imaginary part, degrading S_{11}. Apart from this (time invariant) capacitor C_{p}, the impedance of the BB capacitance is up-converted, resulting in a positive imaginary part for frequencies below ω_{LO}, but a negative inductance for frequencies above ω_{LO} [73]. This latter effect can cancel the imaginary part of Eqn. (5.14) at a frequency $\omega_{\mathrm{LO}} - \Delta\omega$ that is also roughly the frequency of optimum S_{11} due to C_{p}. To bring the dip of S_{11} back to ω_{LO}, complex feedback with resistors R_{FIQ} can be applied [71]. The BB impedance jR_{FIQ}/A [73] is now up-converted with a scaling factor to cancel the term proportional to $-j(\omega_{\mathrm{LO}}C_{\mathrm{p}})^{-1}$ in Eqn. (5.14). The required complex feedback resistance can be calculated as $R_{\mathrm{FIQ}} = A/(2\gamma\omega_{\mathrm{LO}}C_{\mathrm{p}})$ and lower resistance is demanded for the receiver operating at higher frequency. R_{FIQ} also introduces a real part making the BB admittance $Y_{\mathrm{BB}} = (R_{\mathrm{BB}})^{-1} = ((1+A)/R_{\mathrm{F}} + 1/R_{\mathrm{FIQ}})$ is slightly higher (R_{BB} is lower). The C_{p} at RF input is in parallel with $R_{\mathrm{sh}}(\omega_{\mathrm{LO}})$ that is composed of all odd harmonic shunt impedances in the 4-path case. C_{p} decreases higher order harmonic shunt impedances and increases the folded noise. The $R_{\mathrm{sh}}(\omega_{\mathrm{LO}})$ for a 4-path mixer-first receiver can be approximated as [88]:

$$R_{\mathrm{sh}}(\omega_{\mathrm{LO}}) \approx 4.3R_{\mathrm{sw}}(1 + (4R_{\mathrm{sw}}C_{\mathrm{p}}\omega_{\mathrm{LO}} + R_{\mathrm{sw}}/R_{\mathrm{s}})^{-1}) \tag{5.15}$$

At very low frequency $R_{\mathrm{sw}} \approx 1.1\ \Omega$ (*W*/*L* of a NMOS switch is 300 um/40 nm), $C_{\mathrm{p}} \approx 1$ pF yields $R_{\mathrm{sh}}(0) = 4.3(R_{\mathrm{s}} + R_{\mathrm{sw}}) \approx 220\ \Omega$. At higher frequency that is $\omega_{\mathrm{LO}} = 2$ GHz,

$R_{\mathrm{sh}}(\omega_{\mathrm{LO}})$ is reduced to 68 Ω, causing lower $R_{\mathrm{in}}(\omega_{\mathrm{LO}}) = R_{\mathrm{sh}}(\omega_{\mathrm{LO}})||(\gamma 2R_{\mathrm{BB}})$ =33 Ω and worse input matching. The RF input gain can be expressed as a voltage division of $V_{\mathrm{s}}R_{\mathrm{in}}(\omega_{\mathrm{LO}})/(R_{\mathrm{s}} + R_{\mathrm{in}}(\omega_{\mathrm{LO}}))$. The lower $R_{\mathrm{in}}(\omega_{\mathrm{LO}})$ due to C_{p} also causes gain loss and can be computed as:

$$\text{Gain loss @RF} = 20log[(\frac{R_{\mathrm{in}}(\omega_{\mathrm{LO}})}{R_{\mathrm{s}}+R_{\mathrm{in}}(\omega_{\mathrm{LO}})})/(\frac{R_{\mathrm{in}}(0)}{R_{\mathrm{s}}+R_{\mathrm{in}}(0)})] \tag{5.16}$$

For example, the RF gain loss is about 2 dB at 2-GHz LO frequency. To compensate the loss at RF, BB feedback resistance R_{F} can be adjusted to be higher to obtain higher up-converted resistance and bring the effective $R_{\mathrm{in}}(\omega_{\mathrm{LO}})$ to 50 Ω. Both S_{11} degradation and gain loss at higher LO frequency can be compensated by R_{F} tuning. Note that it can be well compensated when $R_{\mathrm{sh}}(\omega_{\mathrm{LO}}) > 50$ Ω. Unfortunately, the presence of C_{p} at the RF-input still increasing the harmonic folding noise although the gain loss and S_{11} are compensated.

5.5 Measurement Results and Comparison

This test chip has been fabricated in a Global Foundries 45 nm Partially Depleted SOI technology. A 4x4 QFN package was used. The total area including pads and decoupling capacitors is 1300 umx1100 um while the active area is 0.8 mm^2. The highest aluminum layer covers almost the whole receiver chip to provide very strong ground shielding. Fig. 5.10 shows the chip micrograph. The external differential clock is applied from the top side, while the RF input signal is applied from the bottom to minimize coupling. Wideband off-chip hybrids were used to serve as baluns to provide a differential RF signal and impedance match to the 100-Ω differential chip input. Both the hybrid and cable losses were de-embedded for all measurements except the S_{11} measurement.

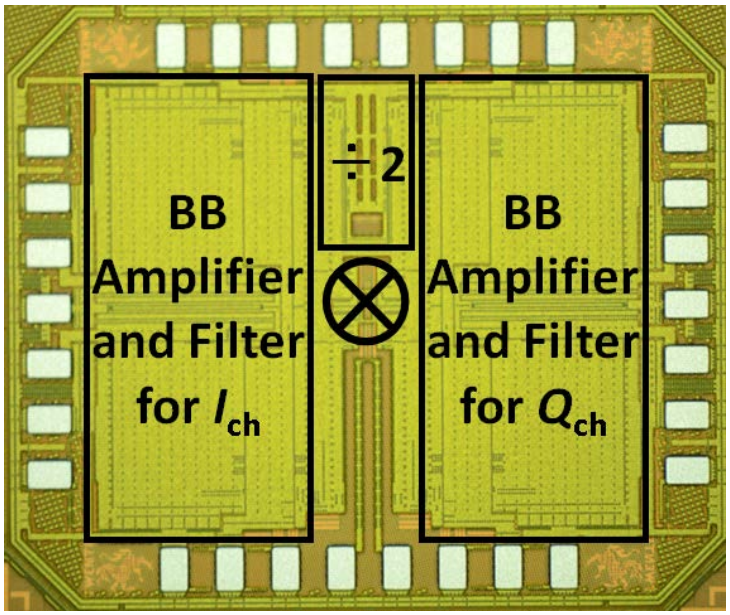


Fig. 5.10: Chip microphotograph.

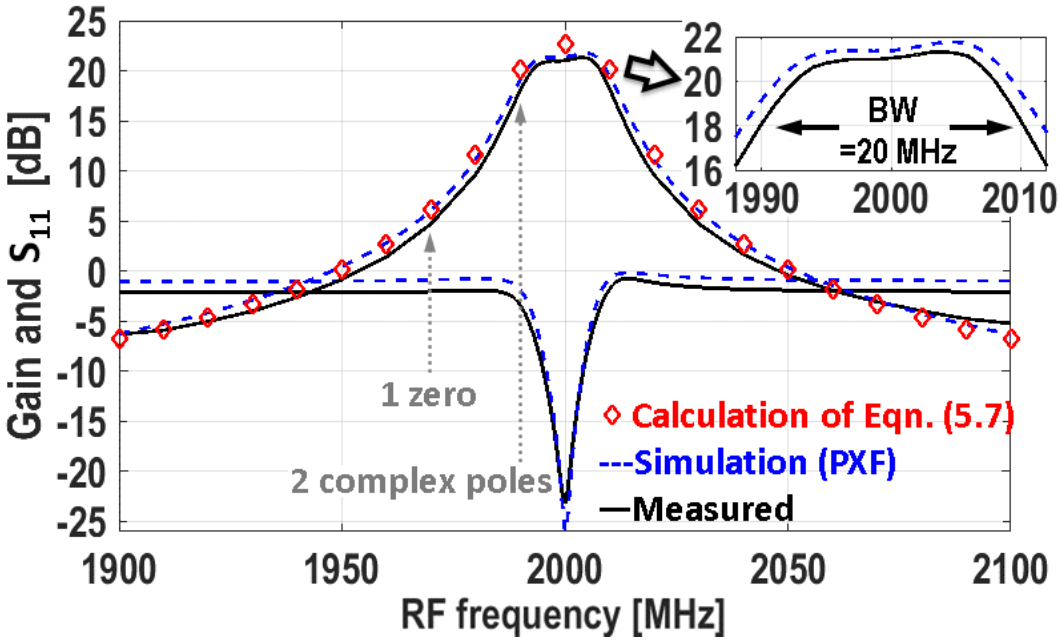
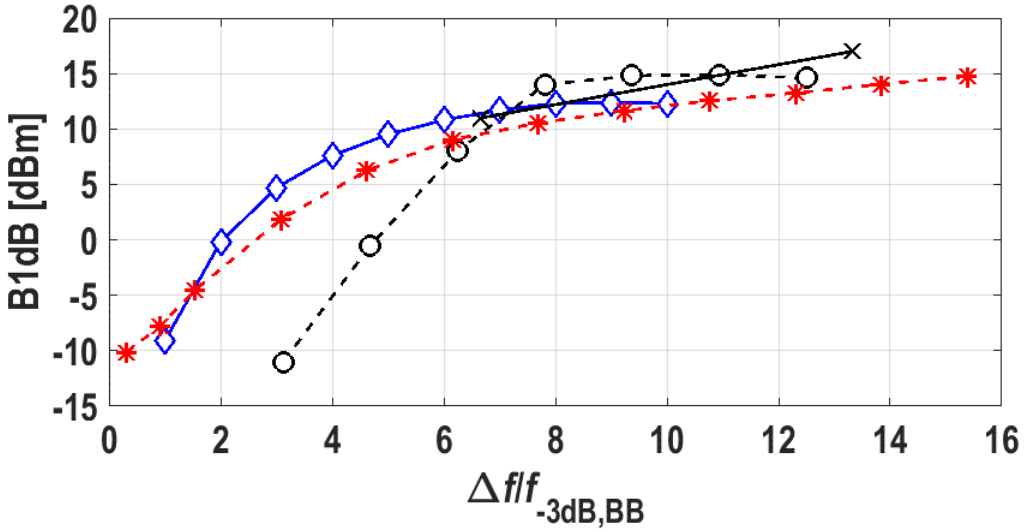


Fig. 5.11: Measured and simulated gain and S_{11} versus RF frequency (f_{LO}=2 GHz). The calculated transfer function from Eqn. (5.7) is also provided.

5.5.1 Gain and S_{11}

Because the BB amplifier is not able to directly drive a 50-Ω load, a low noise external measurement buffer with differential high-impedance input and single-ended 50-Ω output impedance was adopted. A weak tone of −50 dBm is applied to the RF input and the BB output is observed to obtain the conversion gain. Fig. 5.11 shows the measured and simulated gain and S_{11} as a function of the RF input frequency for a 2-GHz LO. The calculated transfer function from Eqn. (5.7) is also provided. Both BB negative feedback and the complex-feedback resistors are programmed to compensate RF gain loss and S_{11} shifting due to parasitic capacitance at the RF input. 21-dB gain and 20-MHz BPF channel bandwidth are obtained. As in simulation, the passband shows an asymmetrical slope induced by the complex feedback resistors. The peak of the gain roughly occurs at the middle between the center frequency and −3 dB frequency, where the magnitude of imaginary part of the input impedance is maximum. The jR_{FIQ}/A is up-converted to cancel the unwanted $-j(\omega_{\mathrm{LO}}C_{\mathrm{p}})^{-1}$ due to parasitic capacitance at the RF input, as discussed in section 5.4.5. However, the gain of the BB amplifier $A(s)$ is a function of frequency. Complete cancellation only happens at the exact center frequency. As the RF frequency changes, the residue $-j/(\omega_{\mathrm{LO}}C_{\mathrm{p}} - A/(2\gamma R_{\mathrm{FIQ}}))$ remains a negative imaginary impedance. The up-converted imaginary part of the BB impedance is positive for the low RF-side-band but negative for the upper sideband [73]. The combination of these imaginary impedances result in an asymmetrical impedance profile at the RF input port. Together with pass-band ripple, this slope in the gain can be compensated in the digital domain. The complex poles are located at BB frequency of 10 MHz. The measured filter roll-off is about 8.4 dB from 10 to 20 MHz offset frequency (It is 9.3 dB for an ideal Butterworth filter), 8.2 dB from 20 to 40 MHz offset frequency (It is 11.8 dB for an ideal Butterworth filter). The less steep filter shape is due to a zero at BB frequency of $(2\pi \cdot 0.5R_{\mathrm{a}}C_{\mathrm{a}})^{-1}$ =31 MHz that can be found in Eqn. (5.7).



—◊— **Implemented RX chip (This chapter), (f_{LO}=2 GHz)**
--*-- **Implemented RX chip (Chapter 4), (f_{LO}=1 GHz)**
--×-- **[29], LNA (f_{LO}=1 GHz)**
--○-- **[69], RX (f_{LO}=0.2 GHz)**

Fig. 5.12: Measured B1dB as a function of relative blocker frequency offset $\Delta f/f_{-3dB,BB}$ and comparison with other blocker-tolerant RF front ends.

5.5.2 B1dB, IIP2 and IIP3

To deal with a blocker that is close to the RX band is in general more difficult, as there are less octaves of filter suppression. Hence, it is preferable for fair benchmarking of linearity to consider the relative frequency offset normalized to the $f_{-3dB,BB}$. Fig. 5.12 shows the measured B1dB as a function of $\Delta f/f_{-3dB,BB}$ for f_{LO}=2 GHz and a desired signal is at 2.001 GHz (f_{BB}=1 MHz) for this work and the implemented RX chip in Chapter 4. Already at $\Delta f/f_{-3dB,BB}$>2, B1dB is >0 dBm, while for $\Delta f/f_{-3dB,BB}$>6, B1dB>+10 dBm. Note that this design only uses a 1.2-V supply (other designs like [29] artificially boost B1dB by

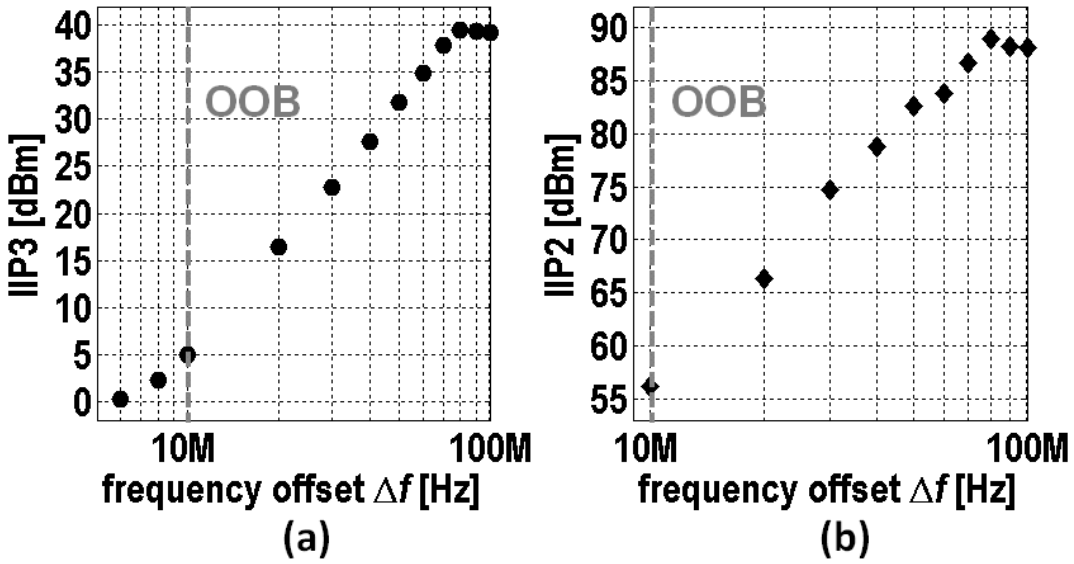


Fig. 5.13: Measured (a) IIP3 and (b) IIP2 versus blocker frequency offset Δf at f_{LO}=2 GHz.

increasing the supply voltage introducing device reliability concerns). The comparison with several blocker-tolerant receivers that achieved >+10-dBm B1dB [29, 69, 90] are also shown. A few dB improvement for maximum B1dB can be achieved by adopting complementary MOS switches [69] or using the bottom-plate mixing technique proposed in [90] to realize more constant switch resistance. It also can be extended by applying higher supply voltage [29] at the cost of higher power consumption. Interestingly, the B1dB is improved by complementary switches but not IIP3 and IIP2. The bias point of the source and drain of both the PMOS and NMOS of a complementary switch is about VDD/2 in [69]. For this complementary switch design, the overdrive voltage is smaller than the designs with only NMOS switches [42, 71, 82, 99]. As a result, the switch resistance is higher leading to worse IIP3 and IIP2 [88]. Thanks to the steeper filter roll-off due to the complex pole pair in our design, we achieve a higher B1dB at lower relative frequency offset as shown in Fig. 5.12.

IIP3 and IIP2 measurements are performed by two-tone tests. Circulators that offer higher than 20 dB isolation are applied between the two blocker signal generators to prevent intermodulation in the test setup, so that over +55-dBm IIP3 was achieved in the test setup itself. For LTE radio applications, the transmitter signal frequency is lower than the receiver frequency for most of the bands. Therefore, the test tones were chosen at $f_1 = f_{\mathrm{LO}} - \Delta f$ and $f_2 = f_{\mathrm{LO}} - 2\Delta f + 500$ kHz for IIP3 measurements, and at $f_1 = f_{\mathrm{LO}} - \Delta f$ and $f_2 = f_{\mathrm{LO}} - \Delta f + 500$ kHz for IIP2 measurements. This choice keeps the resulting IM3 or IM2 product at a constant BB frequency of 500 kHz. Measured IIP3 and IIP2 as a function of Δf for a 2-GHz LO are shown in Fig. 5.13. At Δf=80 MHz, very high IIP3 of +39 dBm and IIP2 of +88 dBm are achieved. Fig. 5.14(a) shows the input referred IM3 as a function of the blocker power for a 2-GHz LO and Δf=80 MHz. The measured P_{IIM3} follows the extrapolation line up to an input power of 0 dBm and +39-dBm IIP3 is obtained.

5.5.3 NF and Gain vs LO Frequency

Measured gain as a function of LO frequency is shown in Fig. 5.14(b) and DSB NF is shown in Fig. 5.14 (c). Measurement results show that the operating frequency can be up to 8 GHz, where an external clock $2f_{\mathrm{LO}}$=16 GHz is applied. The limitation is the achievable rising and falling time of the inverter buffers that drive the mixer switches. It is a process related parameter, where a more advanced technology achieves higher operating frequency. Measurement shows that the receiver gain is kept within 1-dB degradation up to f_{LO}=3 GHz. NF measurements were performed using the Y-factor method with an external noise source. It is below 3 dB up to f_{LO}=2 GHz. The input parasitic capacitance due to mixer switches, input tracks and pads is not taken into account in Eqn. (5.13) of section 5.4.4 noise analysis. In the practical circuit, this lowers the impedance seen by the source voltage at higher RF frequencies. Therefore, the source resistance contributes a

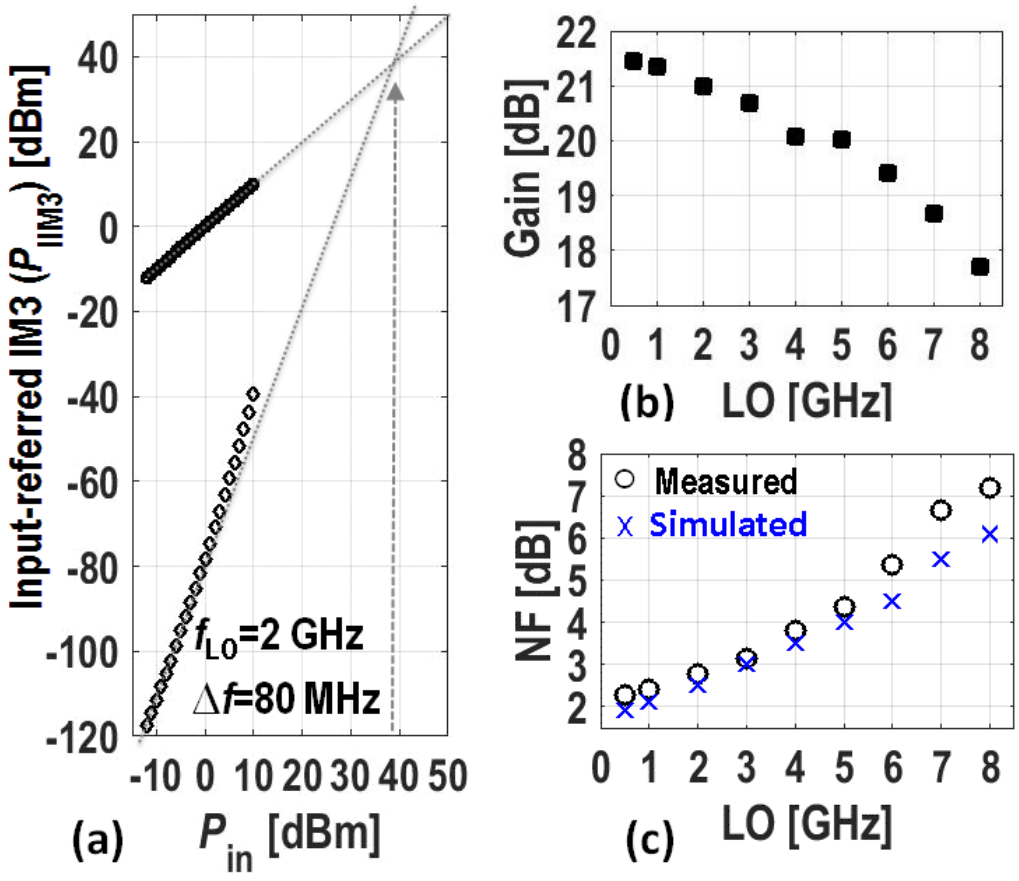


Fig. 5.14: (a) Measured P_{IIM3} versus P_{in} for Δf=80 MHz at f_{LO}=2 GHz, (b) measured gain and (c) DSB NF versus LO frequency. (PSS+PNOISE transistor-level simulated NF is also shown.)

lower percentage of the total output noise at higher frequencies and NF increases. Also, lower complex feedback resistance is required to compensate for more S_{11} shifting at higher f_{LO} leading to more NF degradation (see also 5.4.5).

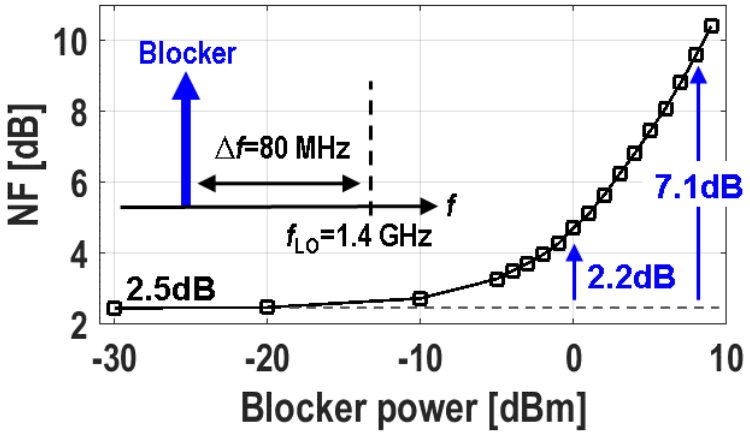
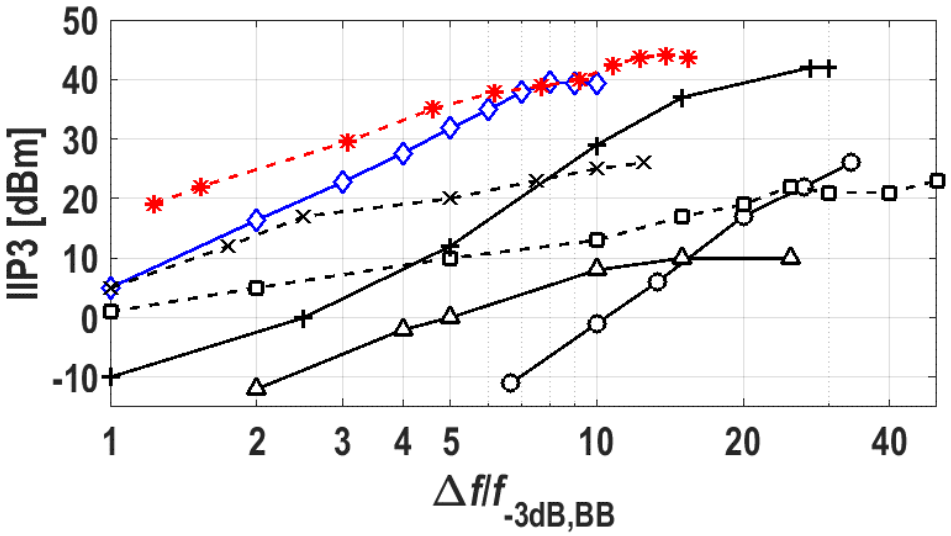


Fig. 5.15: Measured blocker NF for f_{LO}=1.4 GHz. (The highest f_{LO} for blocker NF measurement is 1.4 GHz due to the availability of external bandpass filters for blocker and clock sources.)

5.5.4 Blocker NF

A divide-by-two frequency divider is employed. The 25-% duty cycle LO pulses for quadrature mixing are obtained by combining the divider output with AND logical gates [71, 102]. In order to cover RF-frequencies >6 GHz and achieve low phase noise, the 4-phase clock generator consumes 30 mW/GHz, targeting a simulated phase noise of −171 dBc/Hz at 80-MHz offset frequency (=duplexer offset). To ensure very low in-band noise of the blocker signal generator and low phase noise of the LO clock generator, two external tunable narrow-band BPFs in cascade were applied to the output of the signal generators. This is done to ensure that the reciprocal mixing of the chip dominates performance, instead of phase noise from the measurement equipment. Fig. 5.15 shows the measured NF as a function of blocker power for 1.4-GHz LO and blocker is 80-MHz from f_{LO}. Overall, the presence of strong blockers degrades NF due to reciprocal mixing and gain compression. Since the measured B1dB is high as +12 dBm, the blocker NF degradation is most likely due to reciprocal mixing. The measured desensitization is only 2.2 dB for a 0-dBm blocker,

and 7.1 dB for a 8-dBm blocker. This design achieved a low 0-dBm blocker NF of 4.7 dB which is comparable to one of the best results published so far with a noise cancelling RX [93]. Note that, since an active g_m circuit is required at the RF input port for noise cancelling, linearity is limited in [93]. As a result, the achieved B1dB is <0 dBm which causes blocker NF to degrade rapidly with higher blocker power (>10-dB NF for +3-dBm blocker). Thanks to the steeper filter roll-off due to complex poles at the RF input that reject blockers, this design maintains a blocker NF<+10 dB up to an +8-dBm blocker.



— ◊ — **Implemented RX chip (This chapter), (NF=2.8dB@2GHz)**
-- * -- **Implemented RX chip (Chapter 4), (NF=6.3dB@1GHz)**
-- × -- **[38], BPF (NF=3 dB@1GHz)**
— ○ — **[82], RX (NF=2.9dB@1.5GHz)**
-- □ -- **[103], RX (NF=3.5dB@1GHz)**
— Δ — **[104], RX (NF=2.9dB@1.5GHz)**
— + — **[105], RX (NF=6dB@0.2GHz)**

Fig. 5.16: The IIP3 benchmark of blocker-tolerant RF front ends as a function of $\Delta f/f_{-3dB,BB}$.

5.5.5 Performance Comparison

Fig. 5.16 shows an IIP3 benchmark of blocker-tolerant RF front ends as a function of $\Delta f/f_{-3\mathrm{dB,BB}}$. Circuit type, NF, and operating frequency are also indicated. This design achieves high linearity while keeping NF <3 dB. Note that the RX design introduced in Chapter 4 achieved higher linearity but limited operating frequency and significantly higher NF. A performance summary and comparison is shown in the Table 5.2. Compared to prior art, the receiver achieves high IIP3, IIP2 and wider operating frequency f_{RF}, while maintaining comparable NF and power consumption. This confirms the effectiveness of the higher RF BPF selectivity provided by the proposed mixer-first receiver exploiting positive capacitive feedback.

5.6 Conclusion

In this thesis, a mixer-first receiver with enhanced selectivity due to capacitive positive feedback was proposed. It improves the filter shape exploiting a complex pole pair, while achieving sub-3 dB noise figure and high linearity (IIP3>36 dBm, B1dB>10 dBm) as required for LTE FDD diversity receivers. Important receiver properties were analyzed, like filter shape in terms of natural frequency ω_0, quality factor Q, bandwidth and noise figure. To evaluate stability, the loop gain as a function of frequency was related to the amplifier gain, attenuator transfer and the capacitor ratio of two feedback paths. Loop gain is reliably kept below −6 dB and the loop stability is insensitive to PVT and antenna impedance variations. This receiver design covers all sub-6 GHz cellular bands and achieves a high IIP3 of +39 dBm, IIP2 of +88 dBm and blocker 1-dB gain compression point of +12 dBm for a blocker frequency offset of 80 MHz at 2-GHz LO while achieving a NF of 2.8 dB. The measured NF ranges from 2.4 dB at f_{LO}=1 GHz to 5.4 dB at f_{LO}=6 GHz. The measured desensitization is only 2.2 dB for 0-dBm blocker, and 7.1 dB for 8-dBm blocker, demonstrating robustness to TX leakage and strong blockers.

	*JSSC*10 [71]	*JSSC*12 [93]	*RFIC*15 [82]	*RFIC*15 [29]	RX design in Chapter 4	RX design in Chapter 5
Architecture	Mixer first	Mixer first with Noise Cancelling	Mixer first with positive resistive feedback	Feedback with N-path filter	N-path filters with bottom -plate mixing	Mixer first with positive capacitive feedback
Circuit type	Receiver	Receiver	Receiver	LNA/Filter	Receiver	Receiver
Technology	65nm	40nm	65nm	32nm SOI	28nm	45nm SOI
f_{RF}[GHz]	0.1-2.4	0.08-2.7	0.7-3.8	0.4-6	0.1-2.0	0.2-8
Gain[dB]	40-70	72	40	12	16	21
BB BW [MHz]	10	2	3	7.5	6.5	10
OOB IIP3[dBm]	25 Δf/BW =10	13.5 Δf/BW =40	26 Δf/BW =33.3	36 Δf/BW =6.7	44 Δf/BW =12.3	39 Δf/BW =8
OOB IIP2[dBm]	56	55	65	NA	90	88
B1dB[dBm]	10 Δf/BW =10	−2 Δf/BW =40	3 Δf/BW =33.3	>17 Δf/BW =13.3	13 Δf/BW =12.3	12 Δf/BW =8
NF[dB]	4 ± 1	1.9 (2GHz f_{LO})	2.5-4.5	3.6-4.9	6.3 (1GHz f_{LO})	2.3-5.4 (0.5-6GHz f_{LO})
0dBm Blocker NF[dB]	NA	4.1 (f_{LO}=1.5GHz)	NA	NA	8.1 (f_{LO}=1.3GHz)	4.7 (f_{LO}=1.4GHz)
LO leakage [dBm]	−65 (f_{LO}=1GHz)	NA	<−60	<−40	NA	<−65
Supply[V]	1.2/2.5	1.2/2.5	1.2	2	1.2/1.0	1.2
Power[mW]	37-70	27-60	27-75	81-209	30mW[1]+ 33mW/GHz[2]	50mW[3]+ 30mW/GHz[4]
Area[mm^2]	2.5	1.2	0.23	0.28	0.49	0.8

Proposed RX chip design in Chapter 4:

[1]power consumption of BB amplifiers = 30mW, [2]clock generator power is 33mW/GHz.

Proposed RX chip design in Chapter 5:

[3]power consumption of BB amplifiers = 50mW, [4]clock generator power is 30mW/GHz.

TABLE 5.2: Result Summary and Comparison with Prior Arts

CHAPTER 6
System Demonstration

6.1 Introduction

In most of the literature associated with radio receiver designs, non-linearity is characterized in terms of compression point or IIP2 and IIP3 that are based on two-tone test measurements. These specifications can be defined without knowledge of the modulation technique and the associated SNR. In a practical application, the sensitivity degradation due to non-linearity is of interest. This requires knowledge of the required SNR. In a practical mobile transceiver, the strongest blocker is TX leakage, which is a modulated signal instead of a CW signal. It increases in-band noise floor due to the non-linearity of a practical circuit. To demonstrate the feasibility of deploying the proposed receiver in a real mobile handset, we build a testing setup with a dummy mobile phone to test the SNR degradation due to the presence of strong modulated TX signal.

The sensitivity of a radio receiver is related to noise figure (see Eqn. (2.1)), and this noise figure of the N-path filter or mixer-first receiver depends on source impedance [71, 73]. In the most popular Y-factor NF measurement, a noise source with wideband 50-Ω impedance is applied to the RF input port of the receiver, but the practical antenna impedance is not wideband 50-Ω. Therefore, an alternative NF measurement technique exploiting the gain method will be applied, as motivated further in this chapter. To motivate this properly, we need to review the definition of NF carefully, and especially the effect of noise from image and harmonic bands, which may affect mixer noise figure measurements.

Hence, this chapter first reviews the basics of two NF measurement techniques. Next, the sensitivity testing results for a cell phone under different blocking scenarios are presented.

6.2 NF Measurement Method

6.2.1 Noise Factor/Noise Figure Definitions

A realistic circuit such as an LNA adds extra noise to degrade the noise performance of a system. The noise factor F definition adopted by the Institute of Radio Engineers (IRE) which is an IEEE's predecessor society can be written as [106]:

$$F = \frac{N_a + kT_o BG}{kT_o BG} = \frac{T_e + T_o}{T_o} \tag{6.1}$$

Where N_a is the noise power added by the realistic circuit only, k = 1.38×10^{-23} J/K is Boltzmann constant, T_o = 290° K is the standard temperature for determining noise factor, B is the noise bandwidth and G is the available power gain of the circuit. The noise figure is simply $10log(F)$ in dB. T_e is defined as effective input noise temperature [106] and N_a can be expressed in terms of T_e, resulting $N_a = kT_e GB$.

Eqn. (6.1) can be rewritten as:

$$F = \frac{N_a + kT_o BG}{kT_o BG} = \frac{\text{total output noise}}{\text{noise from source}} = \frac{N_a + GN_i}{GN_i} = \frac{S_i/N_i}{GS_i/(N_a + GN_i)} = \frac{S_i/N_i}{S_o/N_o} \tag{6.2}$$

Hence, noise factor F is also defined as the ratio of the available signal-to-noise ratio (SNR) at the signal-generator terminals to the available signal-to-noise ratio at its output terminals [8].

6.2.2 Y-Factor NF Measurement Method

The noise figure measurement for an amplifier is straightforward. However, some confusions might be arisen when there is frequency conversion involved. In this section, the Y-factor measurement will be inspected step by step for clarifications.

Y-factor NF measurement is commonly used in commercial noise figure measurement equipment. A noise source with accurately calibrated Excess Noise Ratio (ENR) and well-defined impedance is involved. It uses a special low capacitance diode that generates a well-controlled amount of thermal noise when it is reverse biased ("hot" mode), while it produces an available noise kT when it is off ("cold" mode). The ENR that is provided by the noise source can be written as:

$$ENR = \frac{T_{\mathrm{ON}} - T_{\mathrm{OFF}}}{T_{\mathrm{o}}} = \frac{T_{\mathrm{ON}} - T_{\mathrm{OFF}}}{T_{\mathrm{OFF}}} \tag{6.3}$$

Usually it is specified in dB which is $ENR_{\mathrm{dB}} = 10logENR$. T_{ON} is the effective noise temperature when the noise source is turned on. T_{OFF} is the temperature when the noise source is turned off. It is usually assumed $T_{\mathrm{OFF}} = T_0$ =290° K, which is room temperature. The Y-factor method is sometimes also called hot-cold method, while T_{ON} and T_{OFF} are called hot and cold temperature respectively.

As shown in Fig. 6.1, a Y-factor measurement can be conducted by measuring the output power of the DUT using a spectrum analyzer, while the noise source is controlled by a spectrum analyzer to be on or off. The measured output noise powers are N_{ON} and N_{OFF} corresponding to the on and off state of the noise source. The ratio of N_{ON} and N_{OFF} is called the Y-factor that can be written as:

$$\mathrm{Y} = \frac{N_{\mathrm{ON}}}{N_{\mathrm{OFF}}} = \frac{N_{\mathrm{a}} + k\,T_{\mathrm{ON}}\,G\,B}{N_{\mathrm{a}} + k\,T_{\mathrm{OFF}} G\,B} \tag{6.4}$$

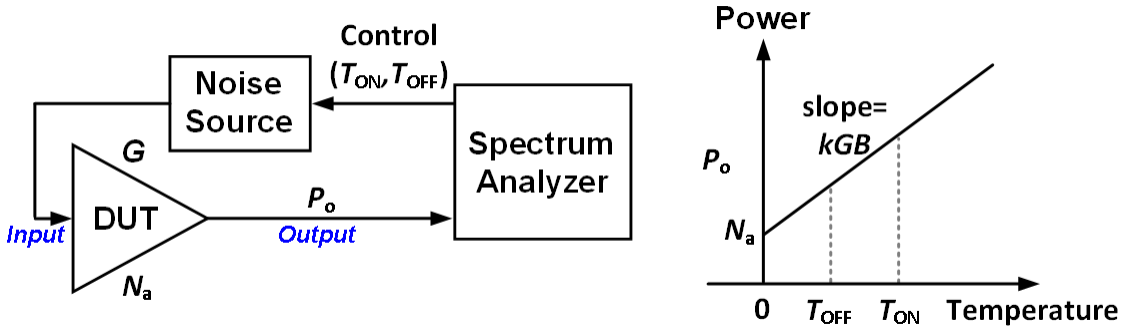


Fig. 6.1: NF measurement setup and the output noise of DUT as a function noise temperature.

Where N_a is the noise power added by the DUT and G is its gain, while B is the resolution bandwidth of the spectrum analyzer. From Eqn. (6.3) and (6.4), N_a can be written as:

$$N_a = k\,T_{OFF}GB\left(\frac{ENR}{Y-1} - 1\right) \tag{6.5}$$

from the noise factor definition in Eqn. (6.2), F can be written as:

$$F = \frac{N_a + GN_i}{GN_i} = \frac{N_a + k\,T_{OFF}GB}{k\,T_{OFF}GB} = \frac{k\,T_{OFF}GB\left(\frac{ENR}{Y-1} - 1\right) + k\,T_{OFF}GB}{k\,T_{OFF}GB} = \frac{ENR}{Y-1} \tag{6.6}$$

Note that this way of measuring system noise factor F can be accurate as it relies on measuring a power-ratio Y without changing any connections (only switching the noise souree between “hot” and “cold”), while ENR is accurately pre-calibrated. To eliminate the influence of the noise contribution from the spectrum analyzer, knowledge and subtraction of the noise contribution of the spectrum analyzer is needed, which can be done by a calibration procedure with the noise source directly coupled to the spectrum analyzer.

NF Measurement for a Direct Conversion

Assuming equal upper-side and lower-side band frequency response in the frequency conversion circuit, the measured noise of the DUT from both side bands while considering the folded back noise at harmonics can be written as:

$$N_{\mathrm{a}} = 2\beta \cdot kT_{\mathrm{OFF}}GB\left(\frac{ENR}{\mathrm{Y}-1} - 1\right) \tag{6.7}$$

Where β>1 specifies that the noise at harmonics is folded back. For example, when a 4-path passive switched RC mixer is implemented, noise at $|m\mathrm{N} - 1|f_{\mathrm{LO}}$ is folded ($m \in \mathbb{Z}$ and $m \neq 0$) [71, 73]. Hence β is 1 + $1/3^2$ + $1/5^2$ + ⋯. Note that in a practical NF measurement environment, the bandwidth of the noise source is often limited, while each next term is also smaller. Often it is sufficient to only consider the noise around the 3rd and 5th order harmonics, leading to 0.6 dB noise figure penalty (the 7th harmonic would only add another 0.1 dB error).

Using the definition of double-side band (DSB) noise factor definition (i.e. the signal and noise are from both side bands), the measured noise factor can be written as:

$$F = \frac{2\beta \cdot k\, T_{\mathrm{OFF}}GB\left(\frac{ENR}{\mathrm{Y}-1}-1\right)+2\beta \cdot k\, T_{\mathrm{OFF}}GB}{2 \cdot k\, T_{\mathrm{OFF}}GB} \tag{6.8}$$

The numerator of the above equation must contains total noise including the folded back noise, but the denominator should only involve the noise from the band of interest (i.e. the folded back noise should be excluded). Eqn. (6.8) can be simplified as:

$$F = \beta\, \frac{ENR}{\mathrm{Y}-1} \tag{6.9}$$

Without harmonic rejection, the correction factor ($\beta > 1$) that makes noise figure worse has to be added in Eqn. (6.9). If the harmonic rejection is implemented, it results in $\beta \approx 1$ so that the correction could be neglected.

6.2.3 Gain Method NF Measurement or Carrier-to-Noise Ratio Method

Assuming the input matching, $10log(N_{\mathrm{i}})$ is kT=–174 dBm/Hz. The noise figure can be related to the SNR ratio of Eqn. (6.1) in dB as follows:

$$NF = P_{\mathrm{o}}[\mathrm{dBm/Hz}] - G[\mathrm{dB}] - (-174[\mathrm{dBm/Hz}]) \tag{6.10}$$

Where $P_{\mathrm{o}} = 10log(N_{\mathrm{o}})$ is measured output noise power of N_{o} in dBm/Hz by using spectrum analyzer. Gain of DUT $G = 10log(S_{\mathrm{o}}/S_{\mathrm{i}})$ [dB] estimation is also required.

Knowledge of the gain G and P_{o} is now needed to find the NF. An in-band signal is therefore usually applied to determine the gain of the DUT for this “gain method NF measurement”. This method measures the carrier-to-noise ratio, while the Y-factor measurement measures the ratio of two noise powers for a hot and cold source.

NF Measurement for a Direct Conversion

When the gain method is deployed to measure NF of a direct conversion receiver, an in-band signal at either the upper or lower side band is applied to measure gain G. But the measured noise power P_{o} is now from both side bands. Hence, single-side band (SSB) NF is obtained. The corresponding DSB NF can be obtained by subtracting 3 dB from the SSB NF. Note that now the folding noise from around harmonics of the LO has already been taken into account implicitly whether harmonic rejection is implemented or not. Hence no further correction is needed, whereas a correction factor should be added for Y-factor measurements if harmonic rejection is not implemented.

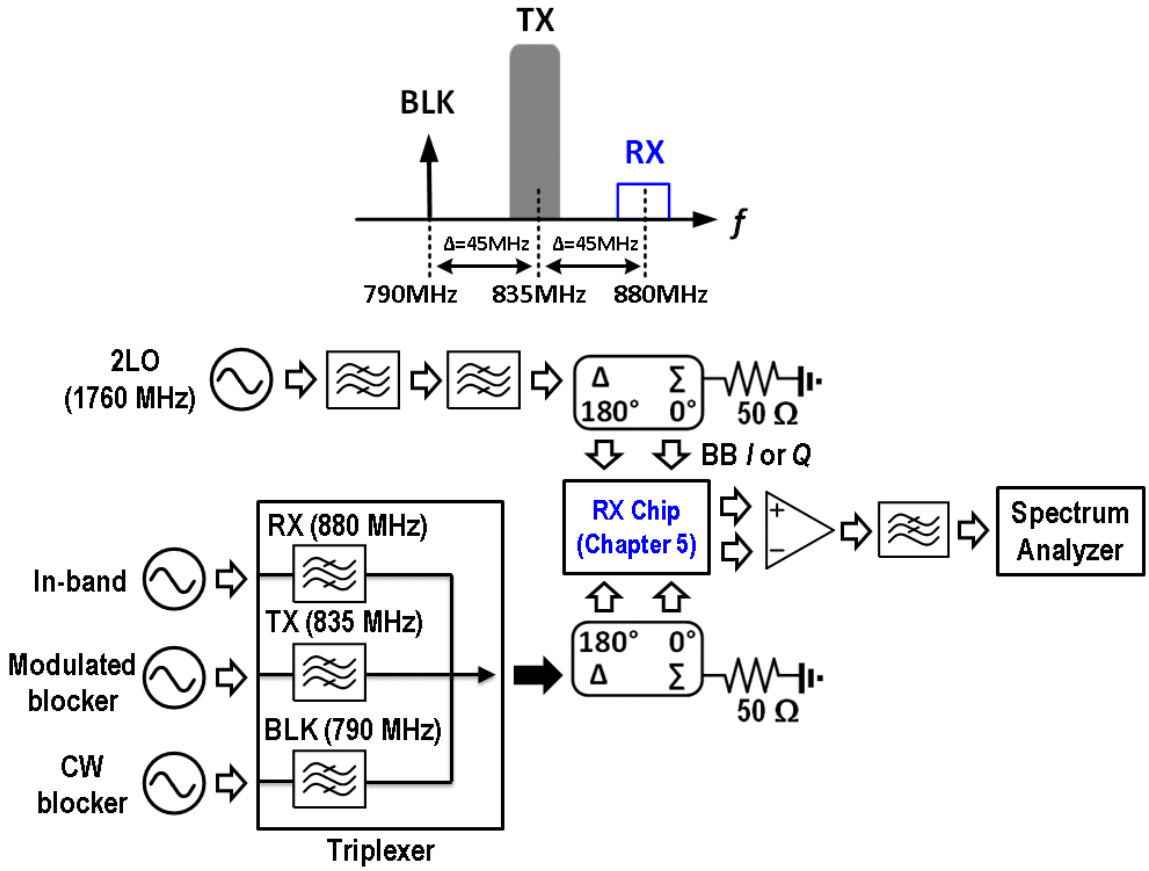


Fig. 6.2: Sensitivity measurement setup for the RX chip (in Chapter 5) applied to LTE band 5.

6.3 RX Sensitivity Test for LTE Band 5

In the most literature, the linearity of a receiver is characterized as IIP2 and IIP3 that are measured by using two-tone test. In a practical FDD mobile system, the strongest blocker is modulated TX signal but not a CW signal. As shown in section 2.4, the receiver desensitization due to modulated TX can be linked to IIP2 and IIP3 mathematically. In the following sections, the related experimental will be performed, some qualitative analysis will be given.

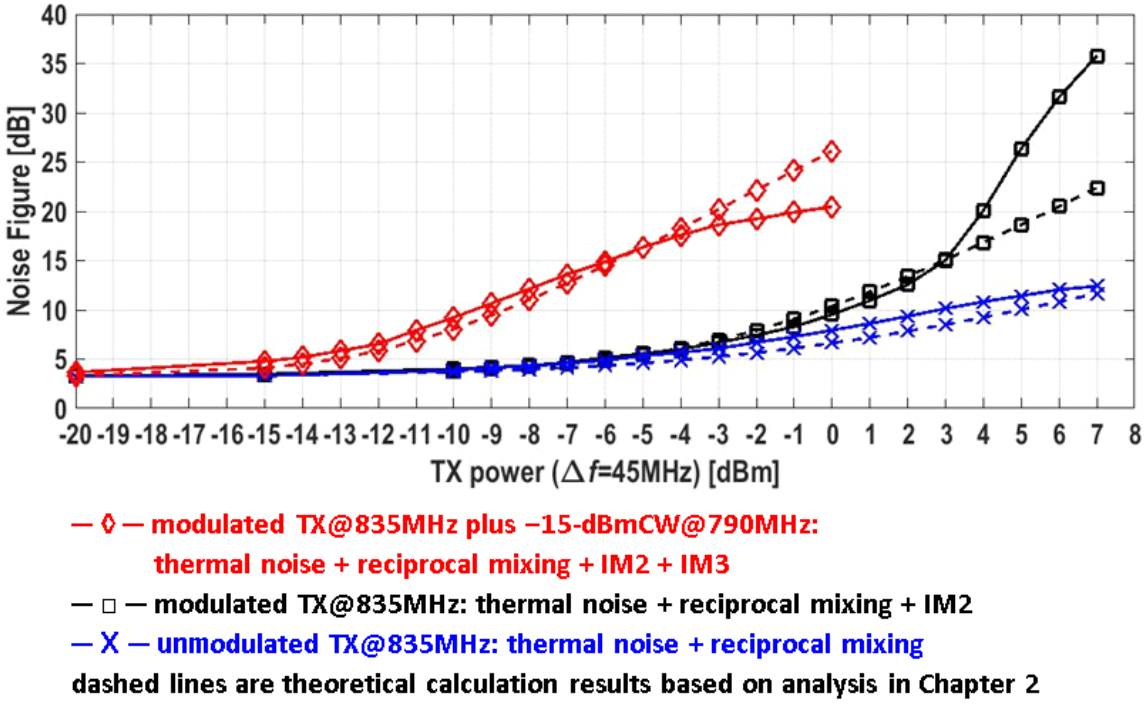


Fig. 6.3: Measured and calculated (based on analysis in Chapter 2) NF under different blocking scenarios.

As shown in Fig. 6.2, some customized filters are required to ensure the low in-band noise (i.e. low as kT) for the combined test signal. LTE band 5 is chosen due to the availability of these filters. LTE band 5 is a FDD duplex mode that deployed in the USA, India and Australia. The TX frequency is 824-849 MHz, and the RX frequency is 869-894 MHz, i.e. 45 MHz duplex spacing.

6.3.1 RX NF Measurement by Using Gain Method

The test setup in Fig. 6.2 is used to evaluate the sensitivity for an in-band CW signal at the RX band (880 MHz) plus 1.7 MHz offset is applied to the RX port of the triplexer. A 20-MHz BW modulated signal is applied at 835 MHz to the TX port, and a CW blocker is applied to the BLK port at 790 MHz. The triplexer [107] implements bandpass filtering

and combines the three signals, i.e. the sum is connected to the RF input port of the proposed RX test chip.

The measured and calculated (i.e. based on analysis in Chapter 2) NF as a function of blocker power under different blocker scenarios is shown in Fig. 6.3. Because the antenna is single-ended, while the implemented receiver is differential, a hybrid [108-110] is applied to perform single-ended to differential conversion. The hybrid and cable loss, the external buffer and spectrum analyzer noise were de-embedded. The measured NF by using gain method is 3.2 dB when there is no blocker signal present. However, the measured NF by using the Y-factor method in Chapter 5 was about 2.4 dB for an RX frequency around 1 GHz. The difference might be due to more inaccuracy of the gain method noise factor measurement. The result of gain method highly relies on the absolute accuracy of the spectrum analyzer that is used to measure the output noise and gain of the receiver. In contrast, the Y-factor is considered more accurate as its result is based on the noise ratio at two noise temperatures. There are some unavoidable uncertainties that can affect the accuracy of the Y-factor measurement, such as the uncertainty of the ENR of the noise source and also the impedance mismatch between DUT and the noise source. The uncertainty of the Y-factor NF measurement result is estimated as 0.12 dB by using the online tool provided by KEYSIGHT TECHNOLOGIES [111].

Next, we measured the NF when the TX modulation is off and the TX produces a single tone at 835 MHz. This corresponds to a blocker NF measurement (see solid curve with ×-marker in Fig. 6.3). Following that, the TX modulation is turned-on, the RX non-linearity and self-mixing mechanism (see. 2.4.4) cause IM2 that falls in the desired band to increase the noise floor (see solid curve with □-marker in Fig. 6.3). The measured NF degradation due to thermal noise, IM2 and reciprocal mixing is kept <10 dB when the TX power is <+0 dBm.

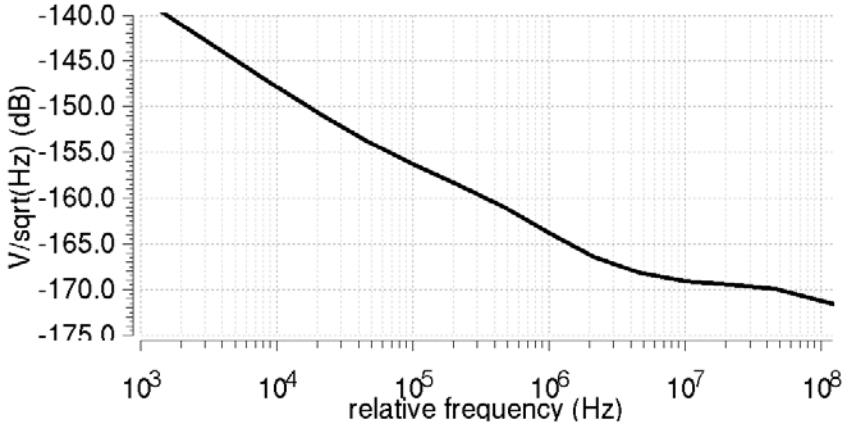


Fig. 6.4: Simulated phase noise of on-chip divider as a function of offset frequency for 1-GHz LO.

Finally, A OOB CW blocker $P_{\mathrm{cw,OOB}}$ at maximum power of −15 dBm [21] located at 790 MHz is also fed to the BLK port for IIP3 desensitization tests. The further NF degradation as a result of the 3rd order intermodulation P_{IIM3} of OOB CW blocker and modulated TX signal is shown as a solid curve with ◊-marker in Fig. 6.3. It degrades NF from 10 to 20 dB when modulated TX power is 0 dBm. The 3rd order intermodulation dominates the NF performance in this case.

Based on analysis in the section 2.3 and 2.4, some discussions are given as follows: As a result of reciprocal mixing, the noise floor N_{BN} (in dBm/Hz) induced by the continuous-wave (CW) blocker with power P_{b} (i.e. the blocker is TX leakage so that $P_{\mathrm{b}} = P_{\mathrm{TX}}$) and a phase noise at the relevant offset frequency $\mathcal{L}_{\omega}\{\Delta\omega\}$ can be derived from Eqn. (2.2):

$$N_{\mathrm{BN}} = P_{\mathrm{b}} + \mathcal{L}_{\omega}\{\Delta\omega\} = P_{\mathrm{TX}} + \mathcal{L}_{\omega}\{\Delta\omega\} \tag{6.11}$$

In the test setup up Fig. 6.2, the phase noise of the external filtered 2LO is minor while the on-chip divider contributes clock phase noise mainly. Fig. 6.4 shows the

simulated phase noise as a function of offset frequency for 1-GHz LO, resulting simulated $\mathcal{L}_{\omega}\{\Delta\omega\}$ = –170 dBc/Hz at Δf=45 MHz.

Using Eqn. (2.10) and assuming $C(N) = -11$ dB [31] for 1 data channel in TX ($N = 1$), expressing noise floor N_{IIM2} due to the 2nd order non-linearity resulting from self-mixing in dBm/Hz:

$$N_{\mathrm{IIM2}} = P_{\mathrm{IIM2}} - 10\,log(\mathrm{BW}) = 2P_{\mathrm{TX}} - IIP2 - 11 - 10\,log(\mathrm{BW}) \quad (6.12)$$

Where BW=20 MHz is channel bandwidth of the modulated TX. Using Eqn. (6.11), Eqn. (6.12) and measured IIP2 = +82 dBm (see Chapter 5) at Δf=45 MHz, resulting $N_{\mathrm{IIM2}} - N_{\mathrm{BN}} = P_{\mathrm{TX}} + 4$ [dB]. It indicates that: N_{IIM2} (due to second order non-linearity) will cause more NF degradation than N_{BN} (reciprocal mixing) when P_{TX} is higher than –4 dBm. The experimental result shown in Fig. 6.3 (see solid curves with □-marker and ×-marker) qualitatively fits the prediction.

Next, noise floor N_{IIM3} due to the 3rd order intermodulation of $P_{\mathrm{cw,OOB}}$= –15 dBm and P_{TX} is investigated. Using Eqn. (2.8) and expressing noise floor N_{IIM3} in dBm/Hz:

$$N_{\mathrm{IIM3}} = P_{\mathrm{IIM3}} - 10\,log(\mathrm{BW}) = P_{\mathrm{cw,OOB}} + 2P_{\mathrm{TX}} - 2IIP3_{\mathrm{req,IM}} - 10\,log(\mathrm{BW}) \quad (6.13)$$

As the measured IIP3 = +30 dBm (see Chapter 5) at Δf=45 MHz and TX channel BW = 20MHz, using Eqn. (6.12) and (6.13) to obtain $N_{\mathrm{IIM3}} - N_{\mathrm{IIM2}} = 18$ [dB]. This predicts the N_{IIM3} is obviously higher than N_{IIM2} in the test setup Fig. 6.2 and qualitatively matches the experimental result (see solid curves with ◊-marker and □-marker in Fig. 6.3).

6.3.2 Sensitivity Test for the RX in Diversity Antenna Path

Fig. 6.5 shows the diversity RX sensitivity test setup with a real cell phone. This test setup is the same as Fig. 6.2 except the isolation between main and diversity antenna path. In Fig. 6.5, the triplexer output is connected to main antenna path of a cell phone and the

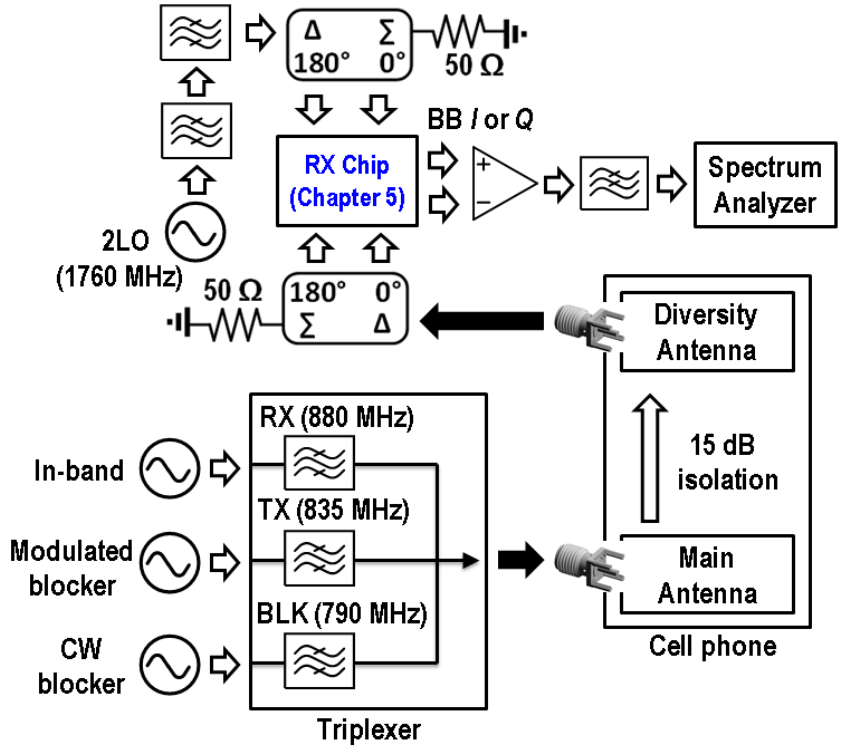


Fig. 6.5: LTE band 5 diversity RX sensitivity test setup with a practical cell phone.

receiver input is connected to the diversity antenna path. In contrast, the triplexer output is directly connected to the receiver input in Fig. 6.2 and there is no isolation.

The measured NF results as a function of modulated TX power for test setup in Fig. 6.2 and Fig. 6.5 are shown in Fig. 6.6. As the diversity antenna of a real mobile phone is connected to the RX chip, the measured NF is about 4.7 dB at very low TX power. On the other hand, the measured NF is about 3.2 dB as the triplexer is directly connected to the RF input of RX chip. This is because the antenna only provides the RX with an in-band 50-Ω impedance matching, while the output impedance of the triplexer is wideband 50-Ω impedance. The lower harmonic shunt impedance generates more noise current bringing, leading to higher NF [88].

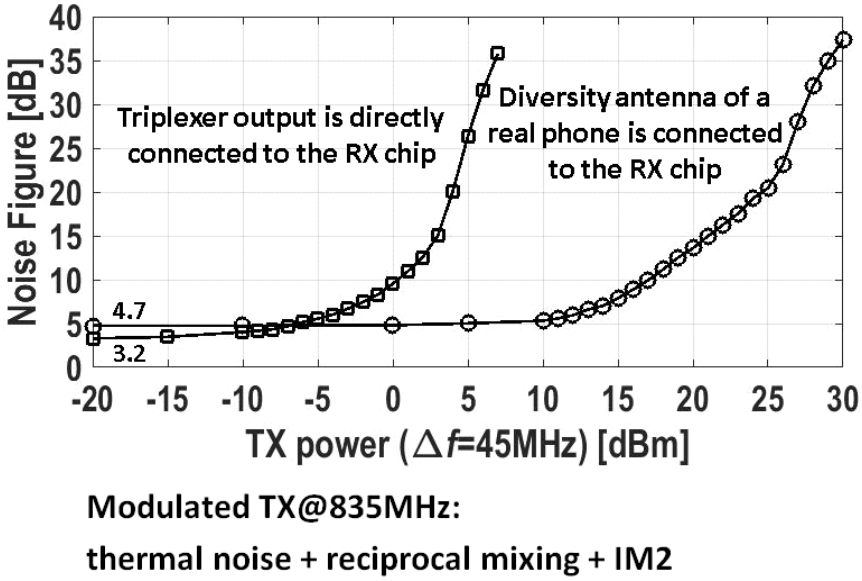


Fig. 6.6: The measured NF results as a function of modulated TX power for test setup in Fig. 6.2 and Fig. 6.5.

When achieving roughly the same NF, there is about 15-17 dB difference in TX power (see x-axis of Fig. 6.6) for these two measurement setups. It indicates there is about 15-17 dB isolation from main to diversity antenna path combined at TX frequencies of 835 MHz.

Fig. 6.7 shows measured NF of the RX chip using the test setup in Fig. 6.5. When the TX modulation is off and the TX produces a single tone at 835 MHz, this corresponds to a blocker NF measurement like solid curve with ×-marker in Fig. 6.3. The measured desensitization is only 0.7 dB for a 15-dBm blocker and 4.4 dB for 24-dBm blocker.

Next, the TX modulation is turned-on and the IM2 increases the noise floor. The measured desensitization due to IM2 and reciprocal mixing is about 3 dB when the TX power is +15 dBm. If the TX power is higher than +25 dBm, the NF deteriorates rapidly since the TX leakage power to diversity RX is higher than B1dB and gain compression worsens the NF as well.

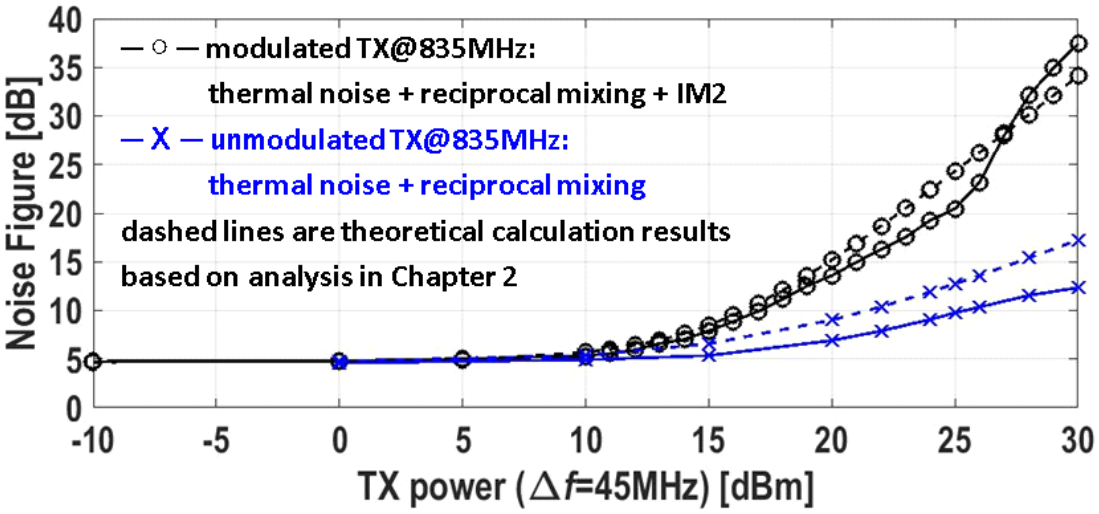


Fig. 6.7: Measured diversity RX NF as a function of TX power (Assuming isolation from main to diversity antenna path is 17 dB for theoretical calculation).

A −15 dBm OOB CW blocker $P_{\mathrm{cw,OOB}}$ at 790 MHz is also fed to the BLK port for 3rd order non-linearity desensitization tests. There is about 25 dB antenna isolation at Δf=90 MHz, the actual OOB CW blocker at the diversity RX is about −40 dBm. (The measured isolation as a function of frequency cannot be shown due to confidentiality concern.) Experiments shows that the NF results remains roughly the same, and there is no obvious further NF degradation due to the 3rd order intermodulation when there is isolation between the main and diversity receiver. In contrast, the 3rd order intermodulation dominates the NF result in test setup of Fig. 6.2 as there is no isolation.

Analysis based on the discussions in Chapter 2 can be applied to explain this difference: As the $P_{\mathrm{cw,OOB}}$= −40 dBm, the measured IIP3 and IIP2 are +30 dBm and +82 dBm (see Chapter 5) at Δf=45 MHz. Using Eqn. (2.8) and (2.10), $N_{\mathrm{IIM3}} - N_{\mathrm{IIM2}} = -7$ [dB] is obtained, where $N_{\mathrm{IIM3}} = P_{\mathrm{IIM3}} - 10log(\mathrm{BW})$, $N_{\mathrm{IIM2}} = P_{\mathrm{IIM2}} - 10log(\mathrm{BW})$ and BW is channel bandwidth of the modulated TX. The antenna isolation offers more N_{IIM3} reduction than N_{IIM2}. Because the slope of IM3 versus blocker power is 3 dB/dB (see Eqn. (2.6)),

while the slope of IM2 versus blocker power is 2 dB/dB (see Eqn. (2.7)). This qualitatively matches the experimental result and indicates that N_{IIM3} is always 7 dB (i.e. about 5 times) lower than N_{IIM2} when there is isolation reducing $P_{\mathrm{cw,OOB}}$.

On the whole, the 2nd non-linearity that dominates the NF degradation of the receiver in diversity antenna path test is due to component mismatch on the chip. Therefore, N_{IIM2} could be reduced by applying digitally assisted calibration [31, 112-114].

6.4 Conclusions

When frequency translation is involved in the circuit under test, some confusions may arise. The basics of two popular NF measurement techniques (i.e. Y-factor and gain method) are explained step by step to clarify possible confusions. Using Y-factor method, the measured result is DSB NF and a correction associated with noise folding needs to be taken into account if harmonic rejection is not implemented. In contrast, SSB NF is obtained by gain method and no correction associated with noise folding is needed whether harmonic rejection is implemented or not.

To demonstrate the blocker tolerance ability of the implemented receiver (i.e. the RX chip shown in Chapter 5) in the realistic use conditions, a LTE band 5 sensitivity test involved a practical mobile is built and performed. As an antenna with non-constant 50 Ω impedance will be connected to the RX test chip, the gain method is used for NF measurement.

In the first experimental setup, the in-band, modulated/unmodulated TX and OOB CW blocker signals are combined and directly connected to the RX test chip, namely there is no isolation between the TX and RX. The measurement shows the 3rd order intermodulation due to presence of OOB CW blocker and modulated TX signal dominates the NF degradation. The analysis based on the discussion in Chapter 2 shows that the 3rd order intermodulation is 64 times (i.e. 18 dB) higher than the 2nd order intermodulation, bringing a qualitative match with the experimental results.

Next, the RX chip is connected to the diversity antenna of a mobile phone, while the combined blocker signal is connected to the main antenna. In this setup, there is about 17 dB isolation from the blocker to RX input at 45 MHz offset frequency, while the isolation is about 25 dB at 90 MHz offset frequency. The dominant factor of NF degradation becomes 2^{nd} order non-linearity. Based on the discussion in Chapter 2, the 2^{nd} order intermodulation is expected to be 5 times (i.e. 7 dB) higher than the 3^{rd} order intermodulation, and a qualitative agreement with the experimental results is obtained. This is due to the fact that the isolation offers more IM3 reduction than IM2. Because the slope of IM3 as a function of blocker power is 3dB/dB (see Eqn. (2.6)), while the slope of IM2 as a function of blocker power is 2 dB/dB (see Eqn. (2.7)).

CHAPTER 7
Conclusions

7.1 Summary and Conclusions

In Chapter 1, the demands of supporting multi-band multi-standard in nowadays mobile handsets were described. It was concluded that off-chip SAW filters are often still used to prevent corruption of the desired band in the presence of strong out-of-band signals. However, supporting the plethora of existing and new bands is becoming troublesome with separate filters for each band. Reducing the cost and size of mobile phones motivates the research for seeking integrated (on-chip) BPF solutions.

In Chapter 2, main challenges associated with linearity for SAW-less receiver design are discussed: intermodulation distortion and gain compression. As out-of-band interferers undergo no or less filtering, much tougher IIP2, IIP3, −1-dB gain compression point and Blocker Noise Figure are required. A practical mobile phone system suffers from interferers, causing cross-modulation, 2^{nd} and 3^{rd} order intermodulation to desensitize receivers. A receiver in a practical mobile system such as 4G needs satisfactory linearity to deal with different blocking scenarios such as a modulated TX leakage, in-band blocking and out-of-band blocking while keeping the required sensitivity. A SAW filter can typically provide >50 dB TX-RX isolation to reduce linearity requirement of the receiver and phase noise requirement of the LO. Without using SAW-filters and in case there is no TX-RX isolation, the required IIP2 is about 100 dB higher, IIP3 is about 75 dB higher and phase noise of the LO must be about 50 dB lower than that for traditional receiver designs. This makes the SAW-less receiver designs very challenging.

In Chapter 3, different concepts targeting integrating RF BPFs on silicon were reviewed, such as a hybrid transformer-based duplexer, TX leakage cancellation, Q-enhanced LC-filter, g_m-C filter and passive switched-RC N-path filter. As the design challenge is high linearity, the use of passive components seems most promising. After a comparison of the pros and cons, the N-path filter or mixer-first receiver were selected to be further explored for dealing with very strong interferers in this research associated with RF receiver design. As the bandpass center frequency of the N-path filter can be accurately controlled by the LO clock signal, flexibility is achieved. Moreover, it is mainly composed of passive MOS switches and capacitors, lower cost and better performance will be obtained with process scaling.

In Chapter 4, aiming for enhanced selectivity and high linearity, a receiver combining 2-stage N-path filtering with passive zero-IF down-conversion is proposed. A cascade of a passive RF Voltage-in-Voltage-out (*V*-*V*) and a Voltage-in-Current-out (*V*-*I*) bandpass filter rejects out-of-band interference before signal amplification. A differential bottom-plate mixing technique was proposed to offer rather constant gate-source and gate-drain voltage of the MOSFET-switches, hence both in-band and out-of-band linearity are improved. Moreover, bottom-plate mixing allows for switch sharing to halve the effective switch resistance for a given switch size, improving linearity. The prototype chip was fabricated in a 28 nm CMOS technology, occupied a total area of 1 mm^2 (an active area of 0.49 mm^2), and consumed 38-96 mW for LO-frequencies of 0.1-2 GHz. While operating at an LO frequency of 1 GHz, a channel bandwidth of 13 MHz, an out-of-band IIP3 of +44 dBm (Δf = 80 MHz), IIP2 of +90 dBm (Δf = 80 MHz), and blocker 1-dB gain-compression point of +13 dBm (Δf = 80 MHz) was achieved, at a noise figure of 6.3 dB. The Bottom-plate mixing with switch sharing can offer higher linearity comparing to the conventional top-plate mixing. However, the parasitic capacitance to ground from all the MOM capacitors directly coupled to the RF input causes both gain and NF degradation. If 6 dB noise figure is acceptable, this limits the operating frequency to about 1 GHz in the

technology chosen. For a practical cell phone application, higher operating frequencies up to 4 GHz are required for 4G (4^{th} generation) networks, while the upcoming 5G (5^{th} generation) networks even demand operating frequencies up to 6 GHz. This pushed our research to topologies that can achieve lower noise at higher frequencies. Inspired by Sallen & Key filter implementations, a new mixer-first circuit topology with capacitive positive feedback was invented which can achieve lower noise (<3 dB) up to a few GHz, while also achieving about +40 dBm IIP3.

In Chapter 5, this mixer-first receiver enhanced with capacitive positive feedback was discussed. The roll-off is a bit less steep than in the implementation in Chapter 4, but lower noise figure and covering all sub-6 GHz cellular bands are achieved. Three types of feedback loops were deployed in the proposed mixer-first receiver design. First, a negative feedback Miller capacitor across the BB amplifier interacts with the source impedance via passive mixer switches. The resulting first order low-pass filter is frequency translated to a 2^{nd} order RF bandpass filter around LO frequency. Next, a positive feedback capacitor driven by the baseband amplified signal followed by an attenuator is added. The combination of the new positive feedback capacitor and the conventional negative feedback capacitor synthesizes complex poles, allowing for steeper filter roll-off than with a real pole. Finally, resistive complex feedback as proposed in [71] was added to correct the center frequency shifting problem due to the parasitic capacitance at the RF input. A prototype chip in 45nm PDSOI achieves a channel bandwidth of 20 MHz, an IIP3 of +39 dBm (Δf = 80 MHz), IIP2 of +88 dBm (Δf = 80 MHz) and blocker 1-dB gain compression point of +12 dBm (Δf = 80 MHz) at an operating frequency of 2 GHz. The noise figure ranges from 2.4 dB at a LO-frequency of 1 GHz to 5.4 dB at a LO-frequency of 6 GHz. Moreover, operating at 1.4 GHz with a 0-dBm blocker power (Δf = 80 MHz), the noise figure is still 4.7 dB. The measured LO leakage is lower than −65 dBm when LO frequency <4 GHz. The chip was fabricated by GlobalFoundries in a 45nm SOI technology and occupies an active area of 0.8 mm^2.

To test the latter receiver chip in realistic practical use conditions, Chapter 6 describes a system demonstration using a LTE band 5 sensitivity test setup. Using a triplexer, a desired in-band signal was combined with a TX signal (either modulated or not) and an out-of-band continuous-wave blocker. The combined signal was supplied to the chip input. When a −15 dBm out-of-band continuous-wave blocker and −10 dBm modulated TX signal are present, the measured noise figure degrades to almost 10 dB as a result of the third order non-linearity. Next, a real cell-phone body with antennas was involved in the measurement. The receiver chip was connected to the diversity antenna while testing signals were connected to the main antenna path. There was 15-20 dB isolation between main and diversity antennas, the measured noise figure was kept < 10 dB for modulated TX signals with a power up to +17 dBm. In this case, the receiver sensitivity limitation became second order non-linearity. The isolation from main antenna offers more IM3 reduction than IM2, because the IM3 as a function of blocker power has 3 dB/dB slope (see Eqn. (2.6)), while the IM2 as a function of blocker power has 2 dB/dB slope (see Eqn. (2.7)).

7.2 Original Contributions

* A cascade of a passive RF Voltage in-Voltage out and a Voltage in-Current out bandpass filter was proposed in a receiver design to enhance the BPF selectivity with high-linearity (Chapter 4).

* A bottom-plate mixing technique was proposed with switch sharing to enhance linearity by keeping both the gate-source and gate-drain voltage of the MOSFET-switches rather constant when turned on. The switch sharing halves its on-resistance for a given switch size to reduce the voltage swing across the switch for improving the linearity. (Chapter 4).

* A low-noise BB-amplifier was proposed with a new common mode control loop re-using current while extra power consumption and noise are avoided. (Chapter 4).

* A mixer-first receiver enhanced with capacitive positive feedback was proposed to obtain an improved filter roll-off and enhanced selectivity, while keeping low noise figure and high-linearity. (Chapter 5).

* The in-band and out-of-band non-linearity mechanism of MOS mixer switches was analyzed qualitatively (Chapter 4 and Chapter 5).

7.3 Recommendations for the Future Work

The passive switched-RC mixing circuits such as N-path filters and mixer-first receivers are attractive in wireless transceivers since high linearity switches and high density capacitances are available in CMOS technology. When applied in wireless receiver designs, this technique offers promising properties such as high-linearity, high compression point, high selectivity, low loss, and wide center frequency tuning range. However, some issues and limitations need to be further explored. Several recommendations for the future work are given below.

* Unwanted signals (interferers) or noise at harmonics of LO frequencies might be folded back to the desired frequency band causing sensitivity degradation when the harmonic frequencies are occupied by other applications. Harmonic rejection techniques [79, 80] can substantially alleviate this problem by offering >60 dB rejection. The rejection ratio is always limited since there is circuit component mismatch. A simple and low cost RF pre-filtering could be considered for achieving better rejection.

* At the antenna port, signals coupled from the LO or baseband via mixer switches may desensitize a receiver. This is usually called LO leakage and mainly due to mismatches such as phase asymmetry of LO clock pulses, up-converted offset voltages of BB amplifiers, unequal gate-drain or gate-source overlapped capacitances, and asymmetrical layout. Calibration techniques [78] can be further investigated to reduce LO leakage. If a circulator is used, this can also provide >20 dB reverse isolation to greatly alleviate this problem.

* As shown in the LTE system demonstration experiments (Chapter 6) that involved a real cell phone, the implemented receiver can maintain <10 dB noise figure in the presence of strong modulated TX signals up to +17 dBm. The proposed receiver serves as diversity receiver and the second order non-linearity dominates the achievable sensitivity in this LTE band 5 test setup. At a blocker frequency offset of 45 MHz, the proposed receiver achieved promising IIP2 that is +82 dBm, but extremely high IIP2 of about +103 dBm is required to tolerate the maximum TX power of +23 dBm and keeps the intermodulation product lower than thermal noise in a practical mobile phone. Since the second order non-linearity of a CMOS receiver is mainly due to mismatch, digitally assisted calibration [31, 112-114] could be applied to enhance IIP2.

* Local Oscillator phase noise requirements are likely the biggest challenge for the N-path filter or mixer-first receiver for commercial FDD applications. Reciprocal mixing of phase noise with a strong blocker causes noise figure degradation which is proportional to the blocker power and phase noise of the LO. In this thesis, the measurement setup involved external BPFs to greatly suppress the phase noise of the external LO generator and satisfactory results were obtained. However, this is likely not practical in products and makes the research on phase noise cancellation [93] relevant to relax the LO phase noise requirements.

Appendix

Analysis of the Attenuator Output of the Proposed Mixer-first Receiver

In Chapter 5, we used the $V_{\mathrm{o,diff}}$ as an output of the proposed mixer-first receiver (see Fig. A.1) that deployed positive feedback to enhance selectivity. However, there is an unwanted zero induced by the non-ideal attenuator in the transfer function $H_{\mathrm{o}}(s) = V_{\mathrm{o,diff}}(s)/(V_{\mathrm{s}}/2)$ (see Eqn. (5.7)), causing less filter roll-off at higher offset frequency from the LO frequency. Later, we realized the attenuator output $V_{\mathrm{a,diff}}$ can be adopted as the receiver output, resulting better selectivity than $V_{\mathrm{o,diff}}$. More detailed analysis is given as follows.

$H_{\mathrm{o}}(s) = V_{\mathrm{o,diff}}(s)/(V_{\mathrm{s}}/2))$ as a function of RF frequency is shown in Fig. A.2. The less steep filter shape at frequencies further away from LO frequency is due to the unwanted zero located at $(0.5R_{\mathrm{a}}C_{\mathrm{a}})^{-1}$. To achieve better selectivity than $H_{\mathrm{o}}(s)$, the attenuator output transfer $H_{\mathrm{a}}(s) = V_{\mathrm{a,diff}}(s)/(V_{\mathrm{s}}/2)$ can be used. $V_{\mathrm{a,diff}}(s)/V_{\mathrm{o,diff}}(s) = A_{\mathrm{a}}/(R_{\mathrm{a}}C_{\mathrm{a}}s + 1)$ is a low pass transfer where A_{a}=0.5 is the attenuation ratio. Combining $V_{\mathrm{a,diff}}(s)/V_{\mathrm{o,diff}}(s)$ with Eqn. (5.7), $H_{\mathrm{a}}(s)$ that can be written as:

$$H_{\mathrm{a}}(s) = \frac{V_{\mathrm{a,diff}}(s)}{V_{\mathrm{s}}/2} = \frac{V_{\mathrm{a,diff}}(s)}{V_{\mathrm{o,diff}}(s)}\frac{V_{\mathrm{o,diff}}(s)}{V_{\mathrm{s}}/2}$$

$$\approx -2\sqrt{2}\sqrt{4\gamma}\,\frac{R_{\mathrm{F}}/(1+g_{\mathrm{m}}(r_{\mathrm{o}}^{-1}+R_{\mathrm{a}}^{-1}+R_{\mathrm{F}}^{-1})^{-1})}{4R_{\mathrm{s}}+2R_{\mathrm{F}}/(1+g_{\mathrm{m}}(r_{\mathrm{o}}^{-1}+R_{\mathrm{a}}^{-1}+R_{\mathrm{F}}^{-1})^{-1})}\,\frac{g_{\mathrm{m}}(r_{\mathrm{o}}^{-1}+R_{\mathrm{a}}^{-1}+R_{\mathrm{F}}^{-1})^{-1}\omega_0^2}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}\,\frac{(0.5R_{\mathrm{a}}C_{\mathrm{a}}s+1)}{(R_{\mathrm{a}}C_{\mathrm{a}}s+1)} \quad \text{(A.1)}$$

ω_0^2 and Q can be obtained from Eqn. (5.8) and (5.9). The unwanted zero located at $(0.5R_{\mathrm{a}}C_{\mathrm{a}})^{-1}$ in Eqn. (A.1) is suppressed by the pole located at $(R_{\mathrm{a}}C_{\mathrm{a}})^{-1}$. Note that the

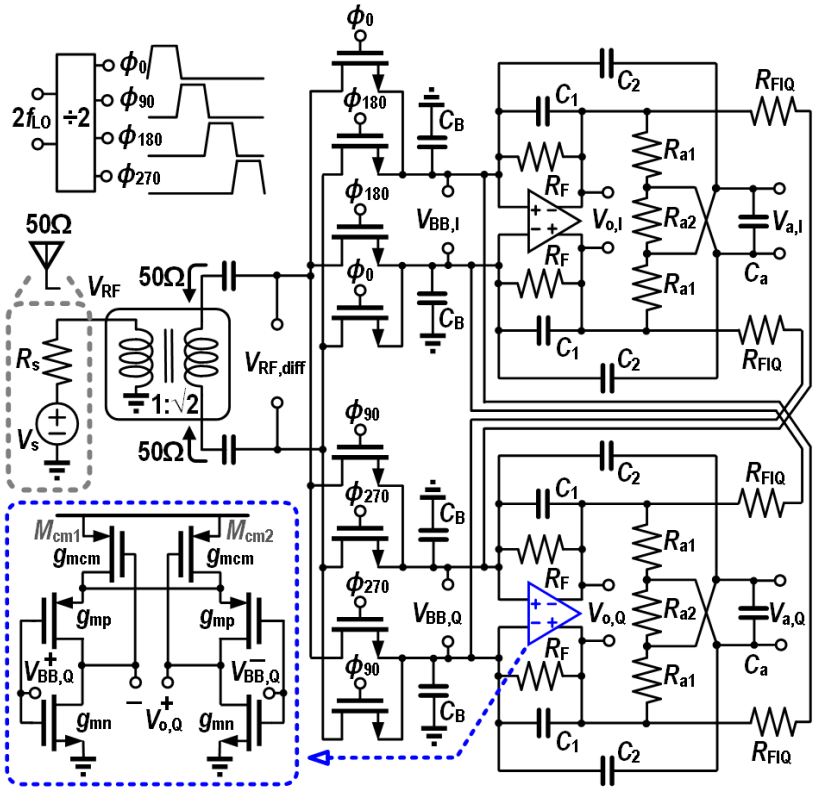


Fig. A.1: Circuit schematic of the proposed receiver in Chapter 5.

SNR or NF at $V_{\text{o,diff}}$ and $V_{\text{a,diff}}$ are quite similar (i.e. the simulated NF results are within 0.1 dB difference at 1-GHz LO) because the signal and noise are both attenuated at $V_{\text{a,diff}}(s)$.

To verify analysis, Fig. A.3 shows Spectre PSS PXF simulation results for the receiver circuit schematic of Fig. A.1 with ideal components. The filter roll off is slightly higher than 40 dB from 10 to 100 MHz offset frequencies. Comparing to $H_{\text{o}}(s)$ in Fig. A.2, $H_{\text{a}}(s)$ achieves more OOB rejection at the cost of 6 dB less gain. Remarking that the achieved linearity at $V_{\text{a,diff}}(s)$ remains the same as $V_{\text{o,diff}}$ because the signal and intermodulation products are both attenuated at $V_{\text{a,diff}}(s)$.

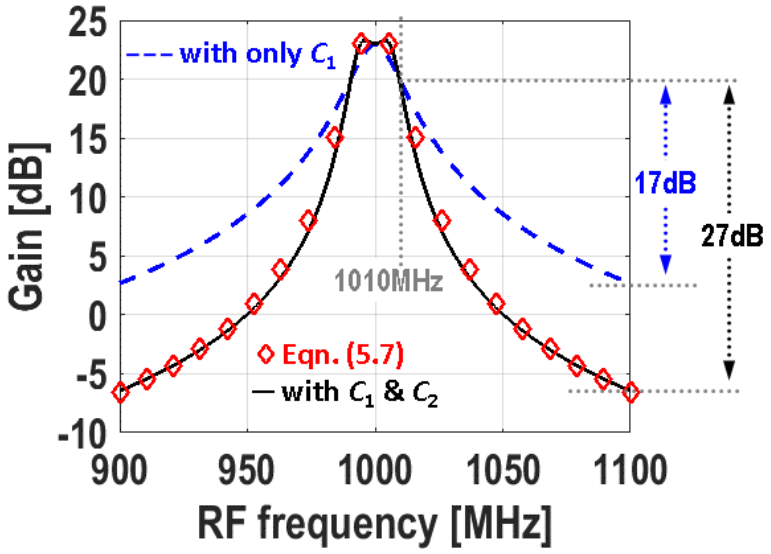


Fig. A.2: Simulated (PXF) and calculated (Eqn. (5.7)) gain $H_o(s) = V_{o,diff}(s)/(V_s/2)$ as a function of the RF frequency for the proposed mixer-first RX with C_1 and C_2 (solid line) and with only C_1 (dashed line).

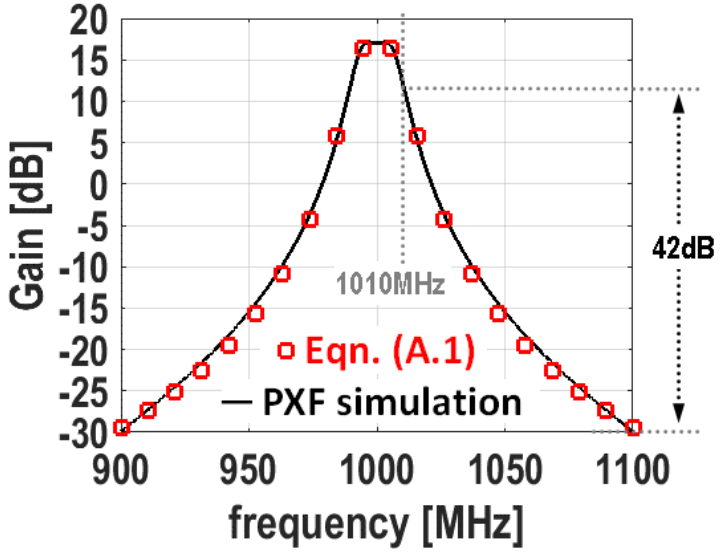


Fig. A.3: Simulated (PXF) and calculated (Eqn. (A.1)) attenuator output gain $H_a(s) = V_{a,diff}(s)/(V_s/2)$ as a function of the RF frequency.

List of Abbreviations

AAF	Anti-Aliasing Filter
AC	Alternating Current
ADC	Analog to Digital Converter
AFE	Analog Front-End
B1dB	Blocker 1-dB gain compression point
BAW	Bulk Acoustic Wave
BB	Baseband
BPF	Band Pass Filter
BSIM	Berkeley Short-channel IGFET Model
BW	Bandwidth
CA	Carrier Aggregation
CM	Common Mode
CMOS	Complementary Metal Oxide Semiconductor
CW	Continuous-Wave
DC	Direct Current
DSB	Double Side Band
DUT	Device Under Test
EM	Electro-Magnetic
ENR	Excess Noise Ratio
FDD	Frequency Division Duplex
FET	Field Effect Transistor
HPF	High Pass Filter
IC	Integrated Circuit
IIP2	Input-referred second-order Intercept Point
IIP3	Input-referred third-order Intercept Point

IM2	second-order intermodulation
IM3	third-order intermodulation
I/Q	In-phase / Quadrature
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LTE	Long Term Evolution
LTI	Linear Time Invariant
MIMO	Multiple-Input-Multiple-Output
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NF	Noise Figure
NMOS	N-type Metal Oxide Semiconductor
OOB	out-of-band
PA	Power Amplifier
PCB	Printed Circuit Board
PDSOI	Partially Depleted Silicon on Insulator
PMOS	P-type Metal Oxide Semiconductor
PSS	Periodic steady-state
QFN	Quad Flat No-leads
RC	Resistor-Capacitor
RF	Radio Frequency
RX	Receiver
SAW	Surface Acoustic Wave
SSB	Single Side Band
TDD	Time Division Duplex
TX	Transmitter

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List of Publications

Papers

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Patents

[1] Y. Lien, E. A. M. Klumperink, B. Nauta, ” WIRELESS COMMUNICATION RECEIVER,” U.S. Patent, US20170373710A1, Dec. 28, 2017.

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Yuan-Ching Lien
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About the Author

Yuan-Ching Lien was born in Taipei, Taiwan. He received the B.S. and M.S. degrees in electrical engineering from National Taiwan University. In 2007, he joined MediaTek Inc., Hsinchu, Taiwan. From 2014 to 2018, he did Ph.D. research at University of Twente, Enschede, The Netherlands. His research interests include reconfigurable RF front-ends, continuous-time filters and Nyquist rate data converters.