Interleaved Planar Packaging Method of Multichip SiC Power Module for Thermal and Electrical Performance Improvement

Fengtao Yang, *Student Member, IEEE*, Lixin Jia, *Member, IEEE*, Laili Wang, *Senior Member, IEEE*, Fan Zhang, *Member, IEEE*, Binyu Wang, *Student Member, IEEE*, Cheng Zhao, *Student Member, IEEE*, Jianpeng Wang, *Graduate Student Member, IEEE*, Christoph Friedrich Bayer, and Braham Ferreira, *Fellow, IEEE*

***Abstract*—Double-sided cooling based on planar packaging method features better thermal performance than traditional single-sided cooling based on wire bonds. However, this method still faces thermal and electrical challenges in multichip SiC power modules. Specifically, one is severe thermal coupling among parallel bare dies, and the other is unbalanced current sharing due to unreasonable layout design. This article aims to explore the potentials of SiC power devices in power module, which are higher current capability and reliability. The proposed packaging method is called interleaved planar packaging and can get rid of the optimizing contradiction between thermal and electrical performance. In this packaging method, there are two functional units: interleaved switch unit and current commutator structure. Benefited from the two units' electromagnetic and thermal decoupling effects, the interleaved power module features low loop inductance, balanced current, low coupling thermal resistance, and even thermal distributions. A 1200 V 3.25 mΩ half-bridge SiC power module based on interleaved planar packaging is fabricated and tested to verify this method's superiority.**

***Index Terms*—Multichip power module, packaging, parallel MOSFETs, silicon carbide.**

I. Introduction

WIDE band gap power device provides main impetus to the development progress of power electronics. Due to high blocking voltage, high operating temperature, fast switching speed, and low ON-resistance, SiC MOSFET is gradually taking over Si-IGBT in various application fields [1], [2]. SiC power module has the potentials to lift Si-IGBT application restrictions with higher efficiency, higher power density, and higher reliability. It has been widely accepted that packaging plays a significant role in exploring SiC devices' potentials. Both the parasitic inductances and thermal resistances need to be addressed for the power module packaging. With the proper packaging form, SiC power modules are expected to operate at higher junction temperature with smaller heatsink, thus reducing total size and weight while maintaining high efficiency or system reliability [3].

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Fengtao Yang, Lixin Jia, Laili Wang, Fan Zhang, Binyu Wang, Cheng Zhao, and Jianpeng Wang are with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 12480, China (e-mail: yangfengtao@stu.xjtu.edu.cn; lxjia@xjtu.edu.cn; llwang@mail.xjtu.edu.cn; zhangfan1990@mail.xjtu.edu.cn; wangbinyu@stu.xjtu.edu.cn; zhaocheng3117@stu.xjtu.edu.cn; wangjackmvp@stu.xjtu.edu.cn).

Christoph Friedrich Bayer is with the Fraunhofer Institute for Integrated Systems and Device Technology IISB, 28452 Erlangen, Germany (e-mail: christoph.bayer@iisb.fraunhofer.de).

Braham Ferreira is with the Department of Telecommunication Engineering, University of Twente, 3230 Enschede, The Netherlands (e-mail: j.a.ferreira@utwente.nl).

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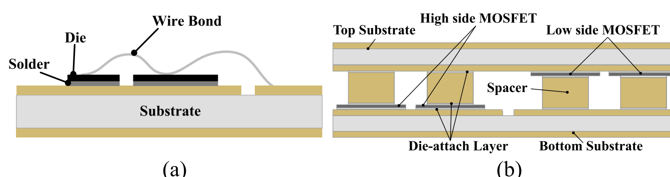

Fig. 1. Power module packaging structure. (a) Wire-bonding structure. (b) Conventional double-sided cooling structure with side-by-side layout (parallel dies in same bridge are attached at same substrate).

The conventional packaging method cannot fully use the SiC device potentials [4]–[7]. Fig. 1(a) shows the wire-bonding structure, which is extensively used. The wire bonds usually bring extra inherent parasitic inductances, which typically take a large part of the whole switching loop parasitic inductances and lack current carrying capability. For thermal performance, the single-sided cooling structure characterizes higher thermal resistances with limited heat dissipation capability. Thus, wire-bonding packaging is not preferred for SiC devices.

Some researchers use planar structures based on double-sided cooling to decrease thermal resistance or loop inductance. The typical structure is shown in Fig. 1(b). Several Si-based IGBT double-sided power modules are fabricated in [8]–[16]. Other researchers also develop the SiC double-sided cooling power modules. In [17], a half-bridge double-sided cooling power module, including single Si-IGBT and SiC-diode, uses the flexible printed circuit board to alternate aluminum wire bonds. In [18], a 1200 V/200 A full-bridge SiC double-sided power module with three parallel MOSFETs was fabricated. Liang [19] proposes a

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1200 V/100 A full SiC double-sided cooling module with two SiC MOSFETs and two SiC diodes in parallel. This module also integrates pin-fin cold plates and features high power density. In [20], a 1200 V/180 A SiC double-sided power module that optimizes the layout based on the P-cells/N-cells concept is proposed. Benefited from the concept, this module features low loop inductances. In summary, the mentioned literature usually focuses on reducing thermal resistances or loop inductances, but did not solve both problems at the same time. In higher power applications, some researchers make submodules paralleled to increase current capability. Other researchers parallel several dies with side-by-side layout [see Fig. 1(b)]. But, the severe thermal coupling and unbalanced current sharing among the dies usually are ignored. The two problems bring challenges in improving the current capability and reliability of SiC power module.

How to integrate parallel SiC MOSFETs in one power module is a critical challenge. One of the reasons is SiC MOSFET characterizes lower current capability because of small die size, which is caused by a compromise between costs and lower yield in immature manufacturing processes [21]. To improve the module's current capability, the common practice is parallelling several dies . But, it usually causes unbalanced current sharing. Besides, the current derating happens at high junction temperature. The practical solution is also to integrate parallel SiC dies, and unbalanced current sharing occurs similarly. Many researchers have proposed some solutions from the packaging point of view. Li [22] introduces the auxiliary source connection wire bonds to weaken the unbalanced current, which is reduced from 7 to 3.5 A under the 10 A ON-state current. In [23], by changing the wire bonds length to add the extra parasitic inductances into the source interconnection of individual bare dies, the unbalanced current is diminished. In [24], a stacked-ceramic-substrate structure is proposed to minimize the parasitic inductances and balance the current sharing. In [25], a passive balancing method that inserts one inductor and one resistor to balance current sharing is introduced. Wang *et al.* [26], develop a double-ended source layout for parallel bare dies to make a symmetrical power loop to improve dynamical current sharing. However, all these researches are only relative to the wire-bonding power module. These methods cannot be applied to planar packaging modules limited by structure and layout.

The other reason is the heat dissipation capability. Smaller SiC die's size mainly causes it. In the SiC planar module, the smaller die dimension brings more severe thermal coupling from two aspects.

1) Length and width of interconnection spacer must be reduced due to the small die size, and the thermal resistance increases correspondingly. Benefited from the spacer, the conventional double-sided power module can dissipate heat to both sides. Once the spacers' thermal resistance increases, the vertical heat dissipation through spacers will be weakened, and the thermal coupling in the lateral direction will be strengthened.
2) The distances among dies are shortened in SiC power module. In most cases, the volume of the module is designed to be small. Thus, the module features lower loop inductances and higher power density. However, it brings more severe thermal coupling because the adjacent dies become closer.

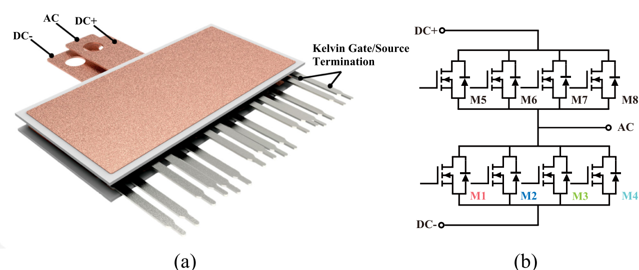

Fig. 2. General view of the power module based on interleaved planar packaging method. (a) Power module. (b) Equivalent circuit.

In the conventional double-sided cooling power module integrating SiC dies, the proportion of lateral heat transfer in dies' power dissipation increases, and the thermal improvement is diminished. Although the smaller die dimension facilitates the improvement of power density, it inevitably raises the challenge of thermal management.

In summary, from the perspective of heat dissipation and current sharing capability, the conventional planar packaging method based on double-sided cooling cannot make full use of SiC device potentials. Solving these problems from the outside of the power module is of limited effect, so a proper packaging method is the best solution.

This article proposes a novel packaging method called interleaved planar packaging. With the interleaved switch unit (ISU) and current commutator structure (CCS), electromagnetic and thermal decoupling can be simultaneously realized in the power module. Thus, the thermal and electrical performance can be significantly improved. It can break the limitation of the existing packaging method and explore the full potentials of SiC devices.

The rest of this article is organized as follows. Section II presents the details of the interleaved planar packaging method. Both the electrical and thermal performance of the proposed module is analyzed. Section III presents the details about fabrication progress. In Section IV, the relevant simulations and experiments are conducted to validated the packaging method's superiority. Finally, Section V concludes this article.

II. Interleaved Planar Packaging Method

In this section, the details of novel packaging method called interleaved planar packaging are presented. For the convenience of illustrating this method, a half-bridge power module is introduced.

A. Half-Bridge Power Module Based on Interleaved Planar Packaging Method

The general, lateral, and internal views of the proposed half-bridge power module are shown in Figs. 2–4, respectively. The half-bridge power module contains eight SiC MOSFET bare dies. Four of them are paralleled as low-side switches (M1, M2, M3, and M4) and others as high-side switches (M5, M6,

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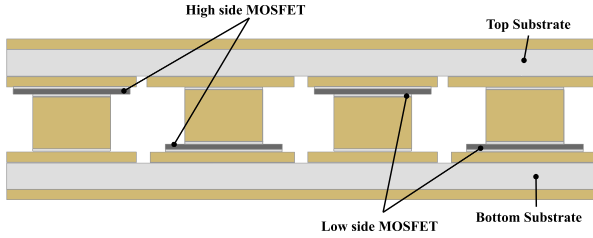

Fig. 3. Lateral view of the power module based on interleaved planar packaging method (only two parallel SiC MOSFETs in one side bridge are shown).

M7, and M8). Although the module uses the body diode to perform as freewheeling diodes, this packaging method is still suitable for the other forms with extra antiparallel diodes. The green area in the Fig. 4 represents the diode reserved soldering position. Soldering extra antiparallel diodes would not influence relevant analysis. The top substrate and bottom substrate play roles as electric conduction, thermal conduction, insulation, and mechanical support. The insulation of the substrate is ceramic. The spacer can conduct the current, transfer the heat dissipation, and guarantee electrical insulation distance. It consists of copper-molybdenum-copper laminate and has an adjustable coefficient of thermal expansion (CTE) that can be correlated with dies and substrates.

This novel packaging structure consists of two parts: ISU and CCS. The ISU features lower loop inductance and performs a thermal decoupling effect. CCS is named from being functionally similar to the current steering commutator in the direct current machine. Its primary functions are to connect ISUs and mitigate the current coupling effect that causes the unbalanced current during switch transients.

B. Interleaved Switch Unit

The interleaved planar packaging method makes any two adjacent parallel dies to interleave in spatial location. For better interpretation, a definition called ISU is introduced.

The parallel SiC MOSFETs are divided into different independent units. In this interleaved power module, SiC MOSFET M1, M2, M3, and M4 are divided into ISU1, ISU2, ISU3, and ISU4, respectively. These ISUs' locations in the power module are shown in Fig. 5.

In one structure, the drain current I_{D} and source current I_{S} conducting direction are opposite [see Fig. 6(a)]. In consequence, the parasitic inductances L_{D} and L_{S} are diminished by the mutual inductance effect. The mutual inductance weakening effect also exists in adjacent ISUs. Next, we only discuss this effect among the ISUs on the low-side half bridge, and the analysis on high-side switches is similar. When the current conducts through four low-side ISUs, any two adjacent structure's current direction is opposite [see Fig. 7(a)]. For instance, the current conducting direction ISU2 is opposite of ISU1 and ISU3. At the current switching transients, the magnetic flux induced by the ISU2 current loop influences ISU1 current loop and ISU3 current loop. Based on Faraday's law, that of two current loops will induce the electromotive force (EMF). Considering the opposite current direction, the EMF can be represented by a negative lump voltage source U^{induced} written as

$$U_{21}^{\text{induced}} = -M_{21}\frac{di_{\text{isu2}}}{dt} \quad and \quad U_{23}^{\text{induced}} = -M_{23}\frac{di_{\text{isu2}}}{dt} \quad (1)$$

where di_{ISU2}/dt is the current slew rate in ISU2 loop, M_{21} and M_{23} are the equivalent mutual inductances in ISU1 current loop and ISU3 current loop individually, and the minus sign represents the resistance to current change referring to Lenz's law. In consequence, any current loop is subject to mutual inductance weakening effect. In the proposed power module, the self-inductances of ISU2 are approximately 1.76325 nH. Under the effect of internal and ISU1s mutual inductance, ISU2's parasitic inductance is reduced 0.75981 nH and equal to 1.00342 nH (about 56.9%). Thus, the parasitic loop inductances are diminished.

Besides, not only does this structure has superiority in electrical characteristics, but also in thermal performance. The interleaved planar packaging method shrinks the equivalent thermal coupling resistance ξ_{ij} (the detailed definition of ξ_{ij} can be found in the Appendix) by increasing the distance between adjacent dies in the z-direction (see Fig. 8). Thus, the heat transfer path of thermal coupling is elongated. Benefited from ISU, the proposed half-bridge power module has even and faint thermal coupling effect. This packaging method wholly utilizes the superiority of the 3-D packaging-structure flexibility to increase heat transfer distance but not swell power module size.

Notably, ξ_{ij} are almost dependent on size of dies, dies' location, and equivalent convection heat transfer coefficient (*htc*) between heatsink and cooling systems [27], [28]. In some SiC special applications, such as high ambient temperature and traditional cooling methods are not available or inefficient, optimizing ξ_{ij} is a relatively efficient approach.

C. CCS and the Current Decoupling Effect

To perform correctly electrical conduction pathway, the ISUs need a structure to connect. Thus, the CCS is proposed, and it features low common parasitic inductance to attenuate current coupling effect among parallel SiC MOSFETs. Fig. 5 shows the CCSs' location in the half-bridge power module. The current conduction path is shown in Fig. 9. We can easily find the mutual inductance effect existing on the CCS. The equivalent circuit with the parasitic inductance distribution (not include terminations) is depicted in Fig. 10. For the sake of simplicity, the parasitic inductance distribution in the low-side bridge is shown in Figs. 11 and 12. The inductances L_1–L_7, L_{16}–L_{19} stand for the CCS's parasitic inductances in low-side bridge. These parasitic inductances already include mutual inductances from other branches. Parts of these inductances exist in two or more paralleling commutation branches, such as L_2 in the branches of M1, M2, and M3. So, these inductances are called common parasitic inductances. Also, not all common parasitic inductances are strongly relevant to current sharing. Some inductances simultaneously affect two or more parallel SiC MOSFETs at the switching transients, thus named current coupling parasitic inductances. For example, L_3 causes the unbalanced current between M1 and M2 at switching transients. Next, further

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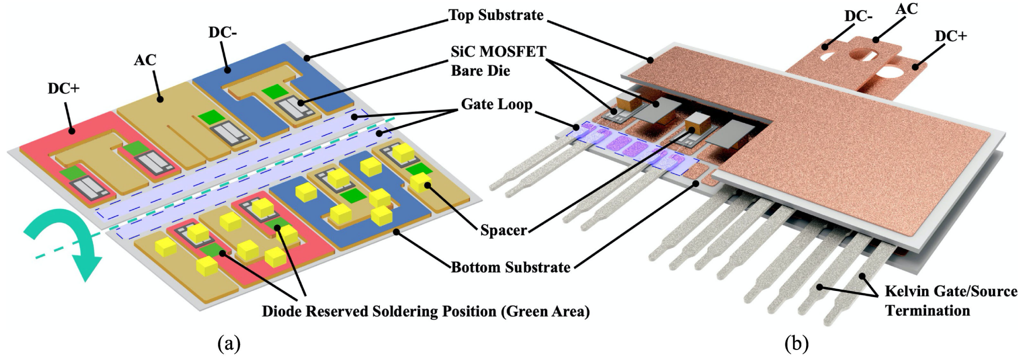

Fig. 4. Internal view of the power module based on interleaved planar packaging method. (a) Internal view (the wire bonds and termination are omitted). (b) Partial section view.

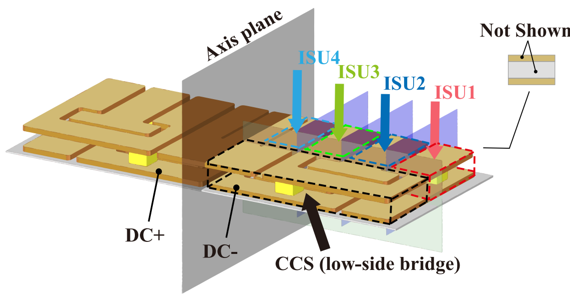

Fig. 5. Location of the ISU and CCS in the whole half-bridge power module (the right of axis surface is low-side). For simplicity purpose, the part of top substrate is not shown.

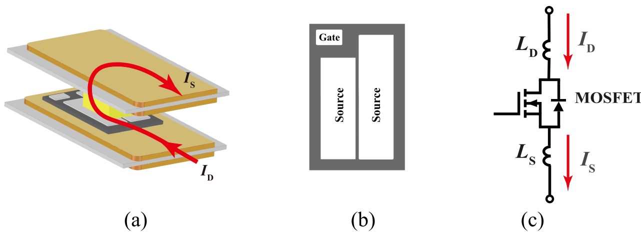

Fig. 6. ISU with SiC MOSFET die. (a) Single ISU diagram. (b) Profile of bare die (the backside pad is drain). (c) Equivalent circuit of ISU.

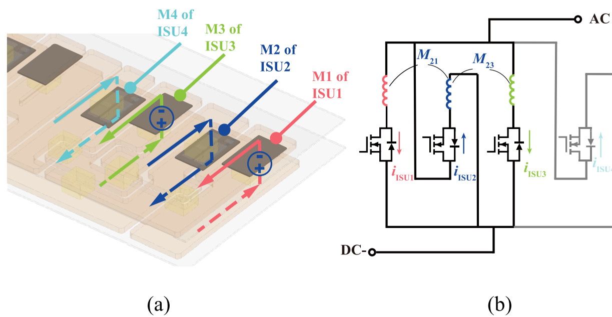

Fig. 7. Mutual inductance weakening effect. (a) Effect among low-side ISUs. (b) Equivalent circuit.

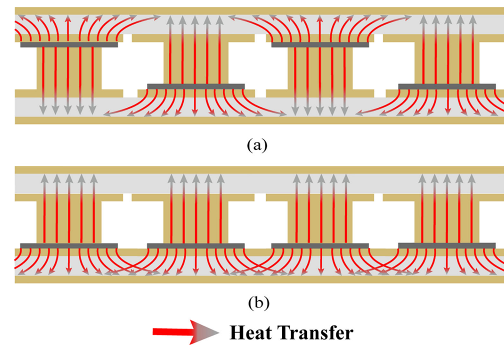

Fig. 8. Illustration of heat transfer pathway among four paralleling SiC MOSFETs in a certain *htc*. (a) Proposed structure. (b) Convectional structure.

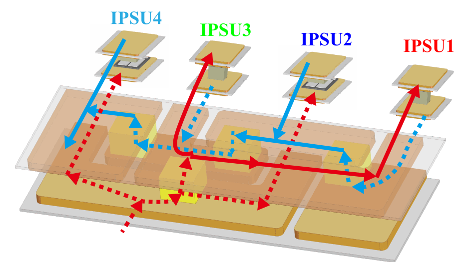

Fig. 9. Structure and current conduction path of low-side bridge CCS (solid line represents the current through top substrate while dotted line represents the current through bottom substrate; red line represents the drain current while blue line represents the source current).

explanations about common inductances and current coupling inductances are presented.

Due to CCS, parasitic inductances of the interleaved power module are more convoluted than regular power module. In the power module, the commutation loop parasitic inductances usually include the drain/source inductances, which only locate in the power loop, and the common source inductances, which coexist in the power loop and gate loop. Because of Kelvin connection in the proposed module, the common source inductances are very small and can be ignored. So, there are two kinds of loop inductances. One is the peculiar inductance, such as L_5 and L_9, which only affect the M1. And peculiar inductances exist in ISU and CCS. Others are common parasitic inductances that concurrently affect two or more parallel MOSFETs. These common inductances exist in the CCS. The distribution is shown in Fig. 11, and the equivalent circuit is shown in Fig. 10. Table I gives L_1–L_{19} inductance values extracted by ANSYS Q3D at 100 MHz solution frequency.

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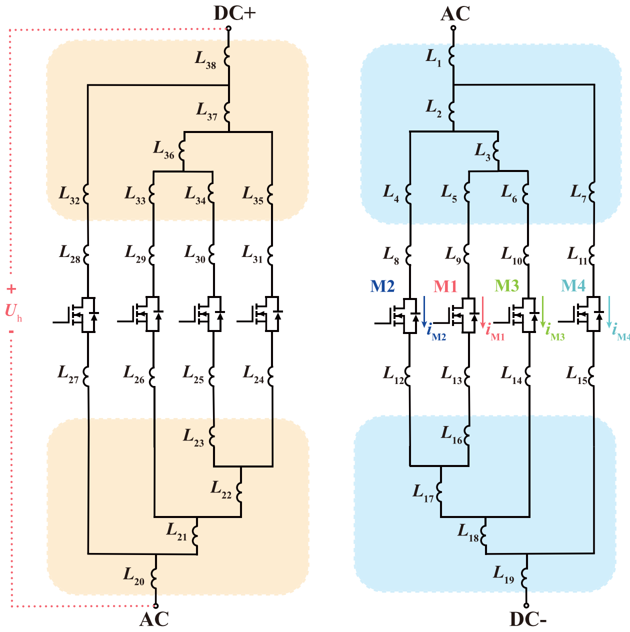

Fig. 10. Circuit of parasitic inductance distribution in the half-bridge power module (the inductances in shadow area represents the IPU's parasitic inductances, others are CCS's parasitic inductances).

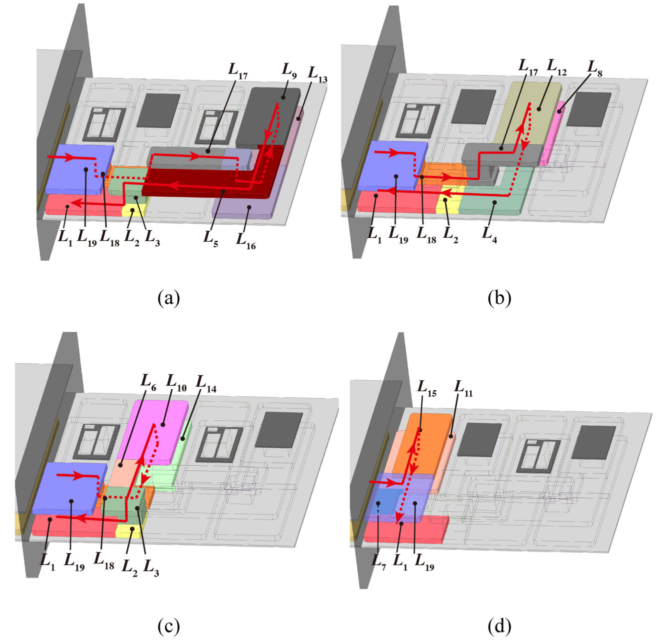

Fig. 12. Diagram of parasitic inductance distribution with the current conduction path. (a) M1. (b) M2. (c) M3. (d) M4.

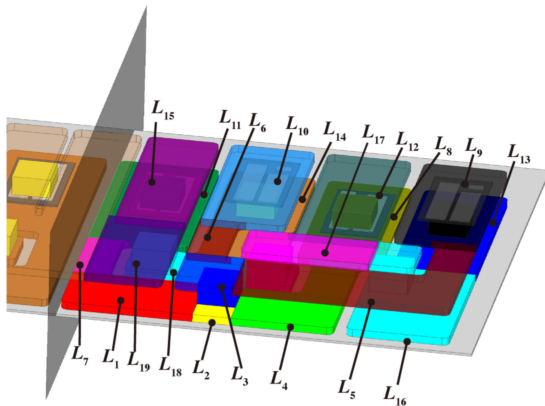

Fig. 11. Diagram of parasitic inductance distribution in power module of low side bridge.

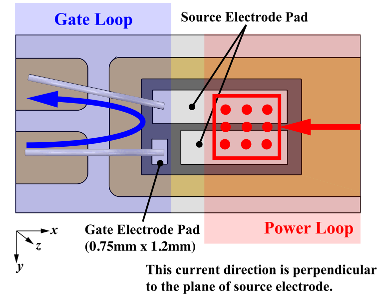

Fig. 13. Kelvin connection and the elimination of mutual inductance (the backside of bare die is drain electrode pad; the gate loop is represented by blue solid line and the power loop current is indicated by red symbols).

TABLE I
SIMULATION RESULTS OF PARASITIC INDUCTANCES

	Result (nH)		Result (nH)		Result (nH)
L_1	0.3011	L_8	0.5036	L_{15}	0.0858
L_2	0.0001	L_9	0.6818	L_{16}	0.2235
L_3	0.1678	L_{10}	0.7271	L_{17}	0.1991
L_4	1.2343	L_{11}	0.6710	L_{18}	0.3978
L_5	2.1322	L_{12}	0.1352	L_{19}	0.2992
L_6	0.9492	L_{13}	1.3052		
L_7	0.7930	L_{14}	0.1579		

The unbalanced current between low sides bridge is expressed as (B3) in the Appendix. There are two factors to inducing unbalanced current: peculiar inductances and common inductances. For example, the unbalanced current between the i_{M1} and i_{M2} is correlative to the peculiar inductances, which are the L_5, L_9, L_{13}, L_{16} in M1 branch, the L_4, L_8, L_{12} in M2 branch, and the common inductances L_3. It is noted that L_3 exists in the M2 and M3 current branches but causes an unbalanced current between the M1 and M2 branches. The reason is that L_3 couples the di_{M3}/dt to M2 branch but not M1 branch. In the first equation of (B3), the term "$L_3 \cdot d(i_{\mathrm{M1}}+i_{\mathrm{M3}})/dt$" demonstrates the current coupling effect. By the way, L_2 is the common inductance between the M1 and M2 current branches and does not bring an unbalanced current. It is better to name L_3 as the coupling parasitic inductance between the M1 and M2 current branches. The sum of peculiar inductances in the M1 or M2 branch is small due to the mutual inductance eliminating effect and has far little influence on current sharing performance [29]. Thus, the sum of peculiar inductances in each parallel branch can be replaced by L'_{D}, and (B3) is rewritten as (2), shown at the bottom of next page.

In the (2), $d(i_{\mathrm{M1}} - i_{\mathrm{M2}})/dt$, $d(i_{\mathrm{M2}} - i_{\mathrm{M3}})/dt$, $d(i_{\mathrm{M3}} - i_{\mathrm{M4}})/dt$ and $d(i_{\mathrm{M1}} - i_{\mathrm{M4}})/dt$ are the difference slope between the two current branches and features much smaller values than the branch current slope. So, these different slopes can be neglected compared with the branch current slope. It is then apparent that the rest terms are all relative to

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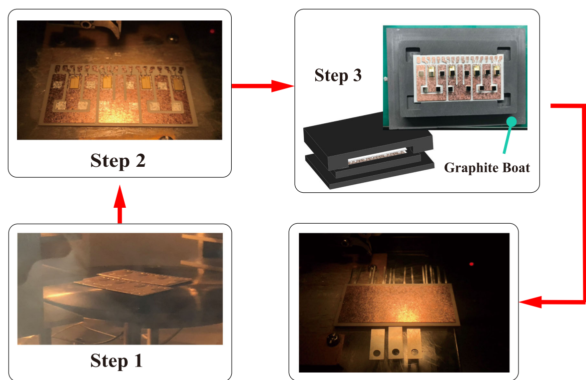

Fig. 14. Half-bridge power module fabrication progress.

the coupling inductances, such as L_2, L_3, and L_{18}, which cause unbalanced current between the M3 and M4 current branches. It means that the coupling inductances are the main factors of unbalanced current.

It can be summarized about current coupling effect. The loop parasitic inductances, including common source inductances and drain/source inductances, are the primary medium of current coupling. The common source inductances have an immense influence on unbalanced current, and many researchers have studied it. Not all the drain/source parasitic inductances have a considerable effect on unbalanced current. They can be divided into three types determined by different current coupling effects.

1) Peculiar inductance, which only exists on the single parallel branch, has little influence on unbalanced current. The current coupling effect does not perform through peculiar inductances.
2) Common inductance existing in the two current branches does not influence the unbalanced current, referring to two concerned current branches. There is no current coupling effect.
3) Common inductance exists on one of the two current branches while also exists on other current branches. It couples the current change of other current branches to the two concerned branches and causes unbalanced current. So, it is called the coupling inductance. The bigger coupling inductance is, the more severe unbalanced current occurs.

Benefited from CCS, the half-bridge power module has little coupling inductance and more balanced current.

D. *Optimization for Gate Loop*

Two optimization methods—the Kelvin connection and the specific layout—are introduced to eliminate the adverse parasitic inductances. Kelvin connection is adopted to eliminate negative feedback in gate loop. As illustrated in Fig. 13, the power loop and the gate loop have a common terminal "source electrode pad". It means that the power loop and gate loop are separated at the source electrode pad with a large conductive area. The common source inductance can be considered as being almost eliminated, and the two loops are decoupled. Furthermore, wire bonds are utilized to connect the gate loop from bare dies to substrate. Thus, the gate loop mainly conducts on the *XY* plane while the power loop conducts the *XZ* plane. The magnetic flux induced by power loop barely penetrates the surface enclosed of gate loop. So, the gate loop mutual inductance induced by power loop is nearly equal to zero (less than 0.012 nH simulated by ANSYS Q3D).

III. Fabricating Progress of Interleaved Planar Packaging Method

A 1200 V 3.25 mΩ half-bridge power module is fabricated in the laboratory. The main fabricating progress is shown in Fig. 14 and Table II presents the details about main components and materials.

The details of the fabrication process are follows.

1) *Step1*: SiC MOSFET bare dies are attached to the active metal bonding (AMB) substrate using $Au_{80}Sn_{20}$ solder. The $Au_{80}Sn_{20}$ eutectic solder has high thermal conductivity, good creep resistance, high liquidus point, and well wettability. Silicon nitride ceramic features high bending strength and better thermal conductivity to perform better in harsh environments. The attaching progress is conducted in the vacuum oven to prevent oxidation with a peak temperature up to 380 °C and held for 1 h to get a high melting point.
2) *Step 2*: as shown in Fig. 14, five-mile thin wire bonds connect the source and gate of dies to AMB bare copper for gate loop. As mentioned above, the gate loop made up of wire bonds forms the Kelvin connection and is not influenced by the power loop.
3) *Step 3*: with the help of a graphite boat to fix the position, the spacer, top, and bottom substrate are soldered together using Au-Sn solder in the vacuum oven with a peak temperature of up to 430 °C. The encapsulating silicon gel is not used for thermal and current experimental measurement.

IV. Simulation and Experimental Results

A. *Thermal Performance Under Low htc*

The thermal performance utilizing the interleaved planar packaging method is validated by extracting the thermal coupling matrix (TCM). First, the feasibility of fabricating progress is validated. Besides, considering the proposed structure, the thermal infrared radiation camera cannot measure SiC MOSFET dies' temperature. So, the fiber optic temperature sensor is used to acquired bare dies' thermal data. Fig. 15 shows the TCM measurement platform, and Table III introduces the details of experimental equipment. Other details on measurement are shown in Figs. 16 and 17.

To get each parallel dies' self-heating and thermal coupling resistances, we adapt the approach presented in the Appendix. In detail, one die is only applied to a series of power dissipations. The temperature rise, which is caused by self-heating and coupling power dissipation, can be gained from the fiber optic temperature sensor. Fig. 18 shows the experiment thermal response curve. In this experiment, SiC MOSFETs operate in the

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TABLE II
COMPONENTS AND MATERIALS IN THE PROPOSED POWER MODULE

Components	Material	Specifications
MOSFET bare dies	Silicon Carbide	CREE-CPM312000013C-1200V-13mΩ, die size: 7.26 mm × 4.36 mm, top side metallization: Au
Eutectic Solder	$Au_{80}Sn_{20}$	Solidus/liquidus point: 280/280 °C
Spacer	Copper/Molybdenum/Copper	Cu/Mo/Cu thickness: 1/4/1 in total 2.5mm and 2.3mm, CTE: 6 ppm/°C
Substrate	Silicon Nitride & Copper	Si_3N_4 AMB size: 66 mm × 32.5 mm, Cu/Si_3N_4/Cu thickness: 0.3mm/0.63mm/0.3 mm, partial gold-plated to 2µm
Wire bonds	Aluminum	Diameter: 5mil

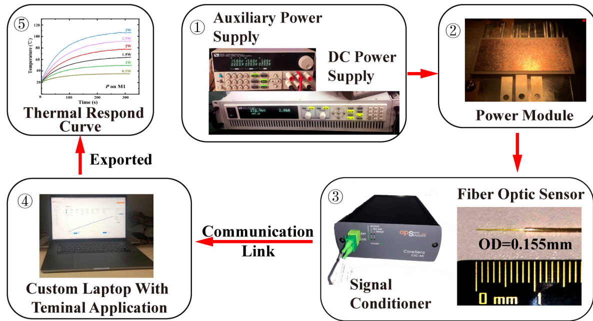
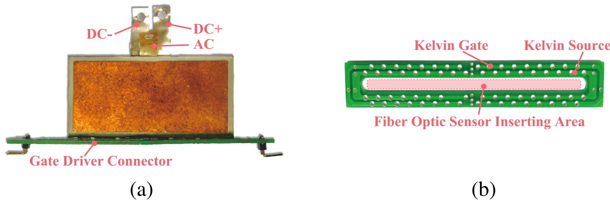


Fig. 15. Diagram of TCM measurement platform.

TABLE III
DETAILS OF EXPERIMENTAL EQUIPMENT

Objective	Details
Fiber optic sensor & signal conditioner	Opsens OTG-F, OD = 0.155mm; CoreSens CSC-AC-S1, 1000Hz sample rate
Oscilloscope	Tektronix MDO4054C, 500MHz, 2.5GS/s
Signal Generator	Keysight 33500B
DC power supply	ITECH IT6726V 1200V/5A/3000W
Auxiliary power supply	ITECH IT6302 0~30V, 3Ax2CH/0-5V,3A
Rogowski coil current probe	CWT06: 30MHz bandwidth, 150A; CWTMini HF1B: 30MHz bandwidth, 300A
Voltage probe	Tektronix TPP0500B 300V/500MHz; TPP0850 1000V/800MHz



(a) (b)

Fig. 16. Experimental fixture. (a) Power module with gate driver connector. (b) Details of gate driver connector.

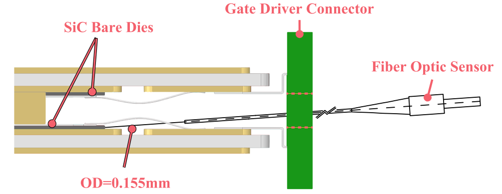
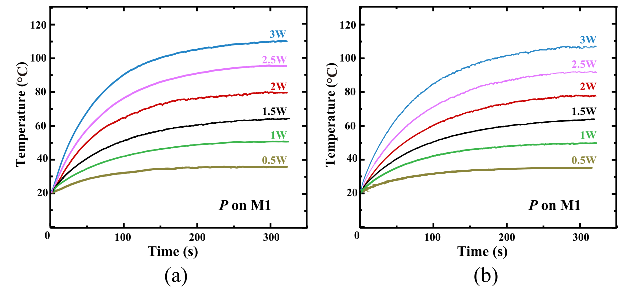


Fig. 17. Diagram of thermal measurement.



(a) (b)

Fig. 18. Diagram of experimental thermal response curves under a series of power dissipation on M1. (a) M1 thermal response curve and (b) is M2.

ohmic region to get a certain power dissipation. Then, a series of P-ΔT curves can be got in the terminal application. According to (A5), the slew rate k of these curves represents self-heating or coupling thermal resistances. In Fig. 33, a series of power dissipation from 0.5 to 3 W stepping 0.5 W is applied on the die M1, and the static temperature can be obtained from the thermal response curve. Thus, the proposal's TCM under low *htc* can be gotten as (C1). Even thermal resistance distribution in (C1) demonstrates that the power module does not have fatal defects like pseudosoldering, cold soldering, and unacceptable void rate [30], [31]. The fabricating progress of the interleaved planar packaging method is reasonable and feasible.

$$\begin{cases} i_{\mathrm{M2}} - i_{\mathrm{M1}} = \left[L'_{\mathrm{D}} \frac{d(i_{\mathrm{M1}} - i_{\mathrm{M2}})}{dt} + L_3 \frac{d(i_{\mathrm{M1}} + i_{\mathrm{M3}})}{dt} \right] / Ron \\ i_{\mathrm{M3}} - i_{\mathrm{M2}} = \left[L'_{\mathrm{D}} \frac{d(i_{\mathrm{M2}} - i_{\mathrm{M3}})}{dt} - L_3 \frac{d(i_{\mathrm{M1}} + i_{\mathrm{M3}})}{dt} + L_{17} \frac{d(i_{\mathrm{M1}} + i_{\mathrm{M2}})}{dt} \right] / Ron \\ i_{\mathrm{M4}} - i_{\mathrm{M3}} = \left[L'_{\mathrm{D}} \frac{d(i_{\mathrm{M3}} - i_{\mathrm{M4}})}{dt} + (L_2 + L_{18}) \frac{d(i_{\mathrm{M1}} + i_{\mathrm{M2}} + i_{\mathrm{M3}})}{dt} + L_3 \frac{d(i_{\mathrm{M1}} + i_{\mathrm{M3}})}{dt} \right] / Ron \\ i_{\mathrm{M4}} - i_{\mathrm{M1}} = \left[L'_{\mathrm{D}} \frac{d(i_{\mathrm{M1}} - i_{\mathrm{M4}})}{dt} + (L_2 + L_{18}) \frac{d(i_{\mathrm{M1}} + i_{\mathrm{M2}} + i_{\mathrm{M3}})}{dt} + L_{17} \frac{d(i_{\mathrm{M1}} + i_{\mathrm{M2}})}{dt} + L_3 \frac{d(i_{\mathrm{M1}} + i_{\mathrm{M3}})}{dt} \right] / Ron \end{cases} \quad (2)$$

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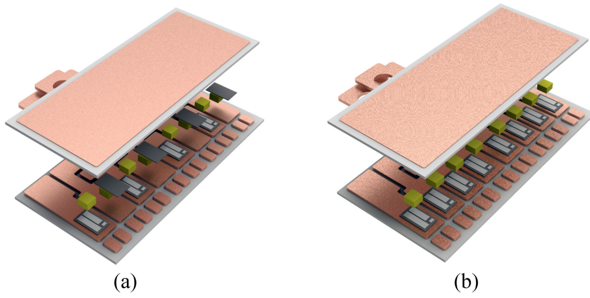

Fig. 19. Diagram of two simulation power module (Kelvin gate/source termination is not shown). (a) Interleaved planar power module. (b) Convectional side-by-side power module.

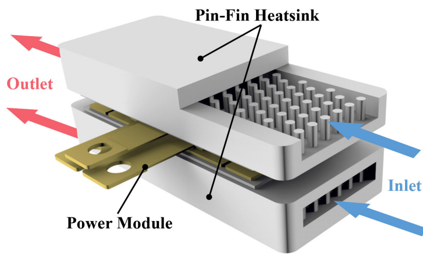

Fig. 20. Planar power module with pin-fin heatsinks.

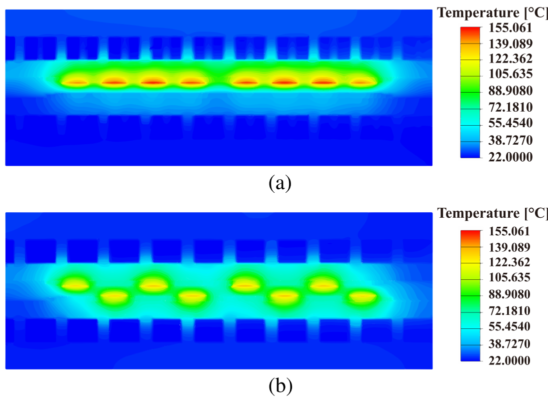

Fig. 21. Temperature distribution between (a) conventional and (b) interleaved power module. This view is the vertical section of whole power module with heatsinks.

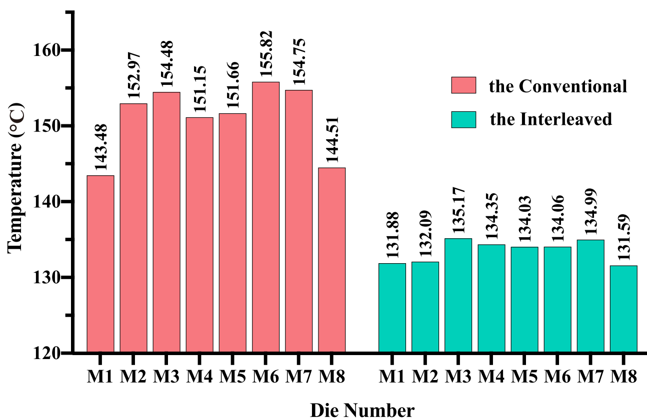

Fig. 22. Temperature distribution between the conventional and interleaved power module.

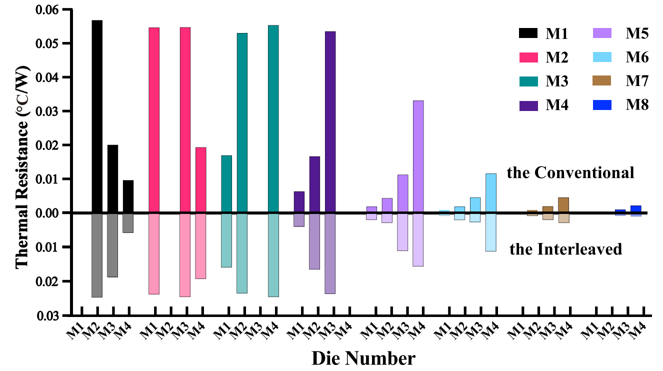

Fig. 23. Comparison of equivalent thermal coupling resistances.

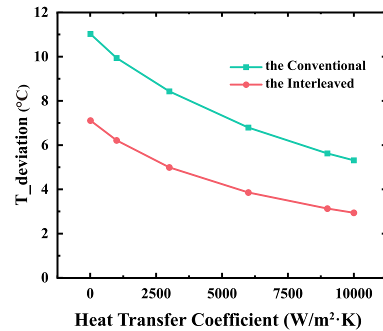

Fig. 24. Temperature deviation in the conventional and interleaved power module versus different *htc*.

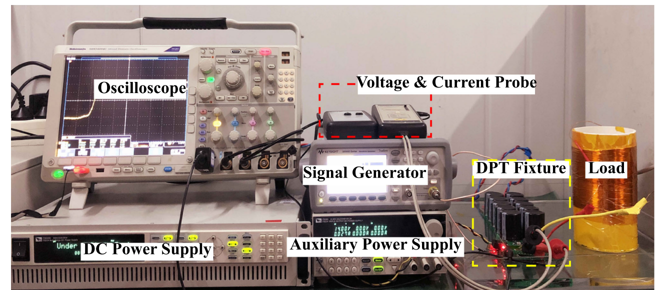

Fig. 25. Photograph of the double pulse test setup.

B. Thermal Performance Under High htc

To illustrate the thermal performance under high *htc*, we conduct several simulations via ANSYS ICEPAK. There are two reasons as follows.

1) Unlike the wire-bonding power module, the dies' temperature must be measured by the contact-type probe without module capsulation. It is not sensible to conduct long-term thermal experiments for safety consideration;
2) Several obvious and uncontrollable factors exist in power module, such as solder layer defects, the characteristic consistency of devices, substrate, and spacer. Laboratory fabrication cannot avoid these problems well. The experimental result may not indicate thermal performance correctly.

The schematic diagram of simulating power module is shown in Fig. 19. A conventional layout that features side-by-side dies, like the structures in [13], [14], and [16], is also researched.

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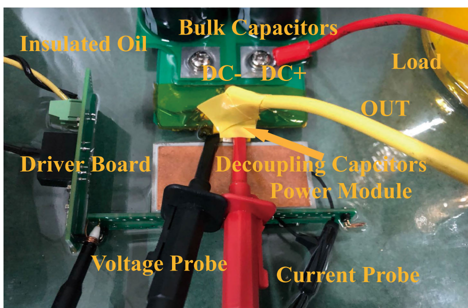

Fig. 26. Photograph of the double pulse test fixture.

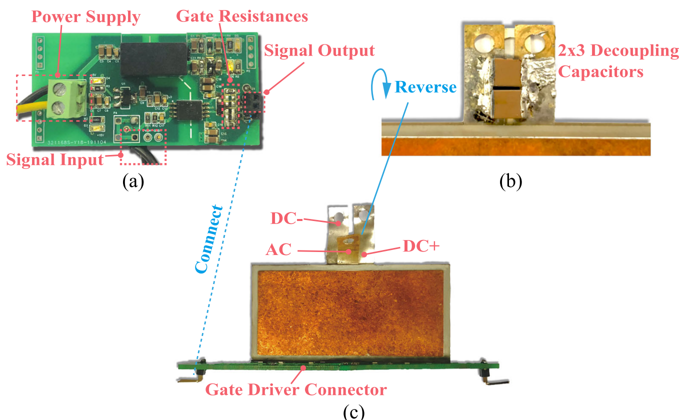

Fig. 27. Details of DPT fixture. (a) Gate driver board. (b) Decoupling capacitors. (c) Power module with gate driver connector.

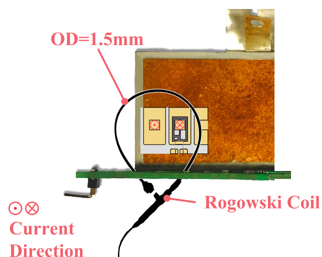

Fig. 28. Diagram of current measurement for current sharing.

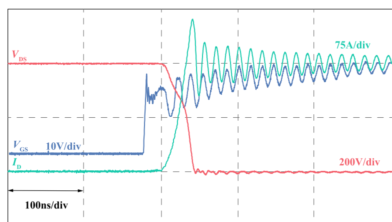

Fig. 29. Turn-ON switching waveforms.

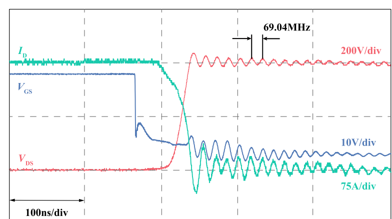

Fig. 30. Turn-OFF switching waveforms.

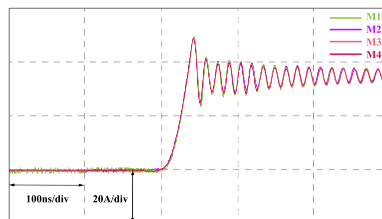

Fig. 31. Turn-ON switching waveforms among the low-side paralleling SiC MOSFETs.

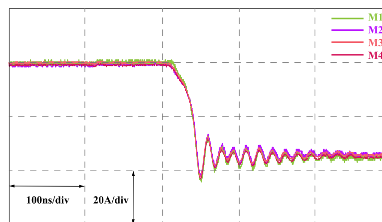

Fig. 32. Turn-OFF switching waveforms among the low-side paralleling SiC MOSFETs.

Because of the symmetrical layout, the low-side bridge's thermal distribution is the same as the high-side bridge [32]. So, the low-side bridge is studied. Fig. 20 shows the whole finite-element method (FEM) module, including the power module and pin-fin heatsink. The FEM module is simulated with water coolant entering the inlet at 22 °C at 12 L/min flow rate under total 3000 W power dissipations. The results are shown in Figs. 21 and 22. The conventional power module's maximum temperature is 155.82 °C while 135.17 °C in the interleaved power module. Fig. 22 shows the temperature mismatch that the maximum temperature deviation in the conventional module is 12.34 °C while 3.40 °C in the interleaved module (the reason for abnormal temperature distribution including M4 and M5 is that the area between that of two dies is slightly bigger than paralleling dies in order to solder AC terminal), and it is evident that the interleaved module has better even temperature distribution. The result demonstrates that the interleaved structure effectively reduces the thermal resistance and the uneven thermal coupling effect.

Furthermore, the TCM under high *htc* is conducted to further illustrate the thermal performance. A series of power dissipations from 50 to 250 W are applied on the parallel SiC MOSFET dies in low-side half bridge. The boundary is forced convection with water coolant entering the inlet at 22 °C at 4 L/min flow rate. Figs. 34 and 35 show the simulation temperature rises versus a series of power dissipations in the convectional and interleaved power module, respectively. Equation (C2) and (C3) in the Appendix are the TCMs of conventional and interleaved power modules, respectively. From these two TCMs, it can be concluded that the equivalent thermal coupling resistance of adjacent die decreases by approximately 57%. As shown in Fig. 23, the equivalent thermal coupling resistances decrease a lot. The different temperature rises between two power modules is mainly caused by the different degree of thermal coupling, and the inconsistency of thermal coupling effect causes the uneven temperature in one power module. The interleaved module

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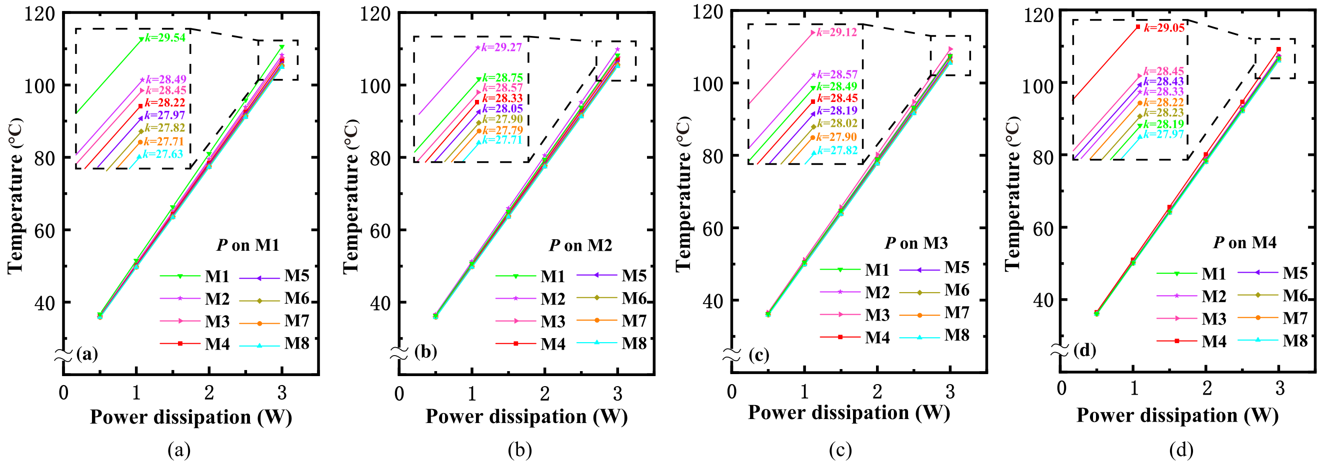
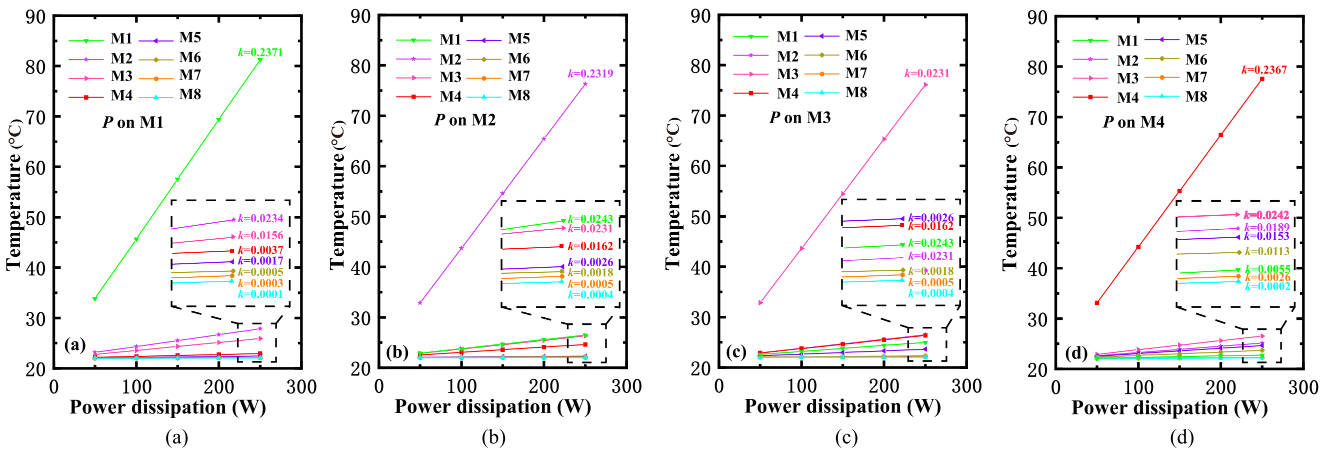


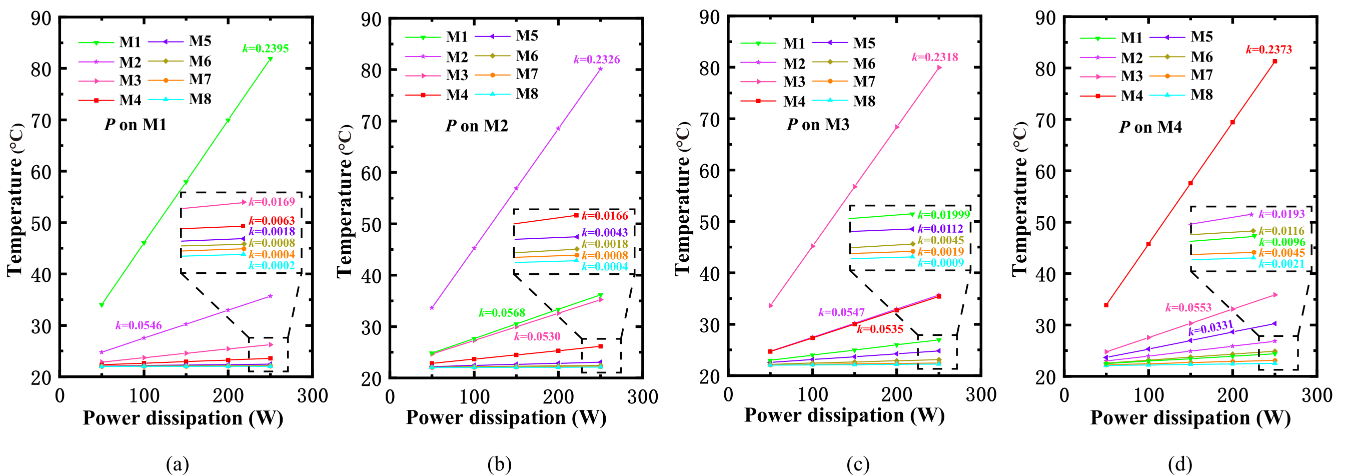
(a) (b) (c) (d)

Fig. 33. Experimental temperature rises with a series of power dissipation P in the proposed power module. (a) P is applied on the die M1. (b) P is applied on the die M2. (c) P is applied on the die M3. (d) P is applied on the die M4.



(a) (b) (c) (d)

Fig. 34. Simulation temperature rises with a series of power dissipations P in the proposed power module. (a) P is applied on die M1. (b) P is applied on die M2. (c) P is applied on die M3. (d) P is applied on die M4.



(a) (b) (c) (d)

Fig. 35. Simulation temperature rises with a series of power dissipations P in the conventional power module. (a) P is applied on die M1. (b) P is applied on die M2. (c) P is applied on die M3. (d) P is applied on die M4.

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characterizes smaller and more even thermal coupling effect. Given the influence of different coolant temperatures between inlet and outlet which causes uneven thermal distribution, the interleaved module still has better thermal performance. So, it has better robustness in thermal performance of balancing temperature distribution.

Furthermore, a simulation referring to temperature deviation and *htc* is conducted. A group of *htc* under total 2000 W power dissipations is applied to the conventional and proposed module. The results are shown in Fig. 24. The interleaved module features a more balanced temperature distribution in the whole *htc* range (100–10000 W/m^2·K). Therefore, the thermal performance of the proposal is superior to the convention cooling under low *htc*. The even temperature distribution, which is mainly determined by thermal coupling effect, is essential to the module lifetime. Ferreira *et al.* [34] has verified that mitigating the temperature mismatch can prolong the B10 lifetime of the most thermal stressed die and the whole module.

C. Electrical Performance

In this section, the fabricated half-bridge power module is tested by double pulse test (DPT) at room temperature. The experimental equipment and DPT fixture are shown in Figs. 25 and 26, respectively. Fig. 27 shows the details of DPT fixture. The current probe inserts into inside of module (see Fig. 28) and measures the spacer current. Because the measurement current is the sum of two or three or four spacers' current, the gained current data need to be calculated. To improve the voltage insulation class, we immerse the power module in insulated oil. Consequently, the fabricated module is tested under 400 V/150 A for safety consideration. The low-side switches are tested while high-side switches keep turn-OFF. The signals offered by signal generator are applied on driver board, which offers a +15/0 V gate pulse with the gate on and off resistances of 5Ω.

The results are shown as Figs. 29-32. Figs. 29 and 30 show the switching waveforms of the low-side total switching characteristics. The overshoot voltage is about 33 V (8% of the 400–V voltage). The ring frequency of the $V_{\rm DS}$ is about 69.04 MHz. According to the datasheet, the MOSFETs parasitic capacitance is about 1.4 nF at 400 V with four parallel SiC MOSFETs. The loop parasitic inductance can be calculated by

$$L = \frac{1}{4\pi^2 f^2 C{\rm oss}} = 3.8\ {\rm nH}. \tag{21}$$

The simulation result is 3.14 nH (by ANSYS Q3D). Noted that there are two reasons for the deviation between simulation and experiment. One is the parasitic capacitance of four parallel SiC MOSFETs is an estimated value. The other reason is the parasitic capacitances between the MOSFET's electrode and cooper layer of the substrate.

Figs. 31 and 32 shows the current sharing performance among the low-side parallel SiC MOSFETs. The maximum unbalanced current is 2.5 A (about 6% of the steady-state current). The results show that the interleaved module features excellent current sharing.

D. Discussion

For thermal improvement, the interleaved planar packaging method has two advantages in thermal performance: low temperature rise and balanced thermal distribution. Benefited from the ISU, the coincidence of heat transfer path between adjacent dies is reduced (as shown in Fig. 8). After that, the temperature rise is smaller than the conventional module. As the lower ξ_{ij} in the proposal under high *htc*, the thermal coupling effect is weak compared to the whole heat transfer process. The temperature mismatch is degraded. Traditional cooling methods are not available or inefficient at high ambient temperature, such as water liquid cooling and air cooling. The up-to-date method which can work at high temperature is expensive and complicated [35], [36]. It is hard to enhance the module thermal performance by improving the *htc*. Utilizing the interleaved packaging method is an effective way to improve cooling capability. It is significant to further make full use of SiC devices at high ambient temperature.

For electrical improvement, there are two mutual inductance weakening effects: in the inner ISUs and among ISUs. Benefited from two weakening effects, the proposal features low loop parasitic inductances and low common coupling inductances. The CCS guarantees the correct electrical connection and features low common coupling inductance, which performs current coupling effect. As demonstrated in the experiment, the power module has excellent switching performance and current sharing.

V. Conclusion

This article proposes a novel packaging method called interleaved planar packaging. Utilizing this method, a 1200 V/3.25 mΩ half-bridge power module prototype is fabricated. For thermal performance, the thermal coupling resistance of adjacent dies is reduced by 57%, and the module gets excellent even thermal distributions. For electrical performance, this power module features low loop inductance which is 3.8 nH. The low parasitic inductance evidently reduces the turn-OFF voltage overshoot. The maximum unbalanced current is about six percent of the steady-state current. The quite low rate ensures the thermal and electrical balance in the power module.

The proposed packaging method is not only confined to the power module presented in this article. Based on the concept of ISU, the power module can possess better electrical and thermal performance with the CCS guaranteeing the proper electrical connection. It gets rid of the optimizing contradiction between electrical and thermal performance. Compared to conventional planar power module, this packaging method can parallel more SiC MOSFETs with better current sharing and cooling capability. In a harsh environment, such as high ambient temperature or no active cooling system, the interleaved planar module also features excellent thermal performance.

Appendix

A. Definition of Equivalent Thermal Coupling Resistance

The temperature rise of the *i*th bare die due to the *j*th bare die's thermal coupling is defined as $\Delta T_{\rm coupl_}ij$, and the coupling heat

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transfer rate is $P_{\text{coupl_}ij}$. So, the thermal coupling resistance can be written as

$$R_{\text{coupl_}ij} = \frac{\Delta T_{\text{coupl_}ij}}{P_{\text{coupl_}ij}},\ (i \neq j). \tag{A1}$$

Then, we use the symbol β_{ij} for representing the proportion of $P_{\text{coupl_}ij}$ to *j*th bare die's total power dissipation P_j. Equation (A1) can be modified as

$$R_{\text{coupl_}ij} = \frac{\Delta T_{\text{coupl_}ij}}{\frac{P_{\text{coupl_}ij}}{Pj} P_j} = \frac{\Delta T_{\text{coupl_}ij}}{\beta_{ij} P_j}. \tag{A2}$$

According to (A2), the *i*th bare die's thermal coupling temperature rise affected by the P_j can be obtained as

$$\Delta T_{\text{coupl_}ij} = R_{\text{coupl_}ij} \cdot (\beta_{ij} P_j). \tag{A3}$$

Furthermore, we can define the equivalent thermal coupling resistance ξ_{ij} as follows:

$$\xi_{ij} = R_{\text{coupl_}ij} \beta_{ij} \tag{A4}$$

or

$$\xi_{ij} = \frac{\Delta T_{\text{coupl_}ij}}{P_j}. \tag{A5}$$

The TCM, which exposes the level of thermal coupling effect, can be written as (A6) shown at the bottom of this page, where ΔT_j is the temperature rise of *j*th bare dies, R_{ii} is the self-heating resistance. Equation (A6) also can be simplified as

$$\Delta T_i = R_{ii} P_i + \sum_{j=1, i \neq j}^{j} \xi_{ij} P_j,\quad (i, j = 1, 2, 3, \cdots, n)\,. \tag{A7}$$

Equation (A5) provides an approach to calculating ξ_{ij}. We can apply P_j on the *j*th bare die and measure the *i*th bare die's temperature rise. In the meanwhile, (A4) reveals which parameters domain the thermal coupling effect. Notably, ξ_{ij} is not affected by P_j but $R_{\text{coupl_}ij}$ and β_{ij}.

B. Analysis of the Unbalanced Current

According to the Kirchhoff laws, the voltage drop of each parallel branches loop parasitic inductances including the common inductances can be expressed as (B1)–(B2) shown at the bottom of this page [35], where the U_{DC} is the dc-bus voltage, the U_{h} is the voltage drop between the DC+ and ac terminals, U_{M} is the voltage drop between the drain and source of the low-side half-bridge SiC MOSFETs. We can assume that the resistances of parallel SiC MOSFETs R_{on} are equal at the same moment. Thus, the unbalanced current between low-side bridges is expressed as (B3) shown at the bottom of this page.

$$\begin{bmatrix} \Delta T_1 \\ \Delta T_2 \\ \cdots \\ \Delta T_{i-1} \\ \Delta T_i \end{bmatrix} = \begin{bmatrix} R_{11} & \xi_{12} & \cdots & \xi_{1,j-1} & \xi_{1,j} \\ \xi_{21} & R_{22} & \cdots & \xi_{2,j-1} & \xi_{2,j} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \xi_{i-1,1} & \xi_{i-1,2} & \cdots & R_{i-1,j-1} & \xi_{i-1,j} \\ \xi_{i,1} & \xi_{i,2} & \cdots & \xi_{i,j-1} & R_{i,j} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_{i-1} \\ P_i \end{bmatrix} \tag{A6}$$

$$\begin{bmatrix} U_{\text{DC}} - U_{\text{h}} - U_{\text{M1}} \\ U_{\text{DC}} - U_{\text{h}} - U_{\text{M2}} \\ U_{\text{DC}} - U_{\text{h}} - U_{\text{M3}} \\ U_{\text{DC}} - U_{\text{h}} - U_{\text{M4}} \end{bmatrix} = \begin{bmatrix} L_{11} & L_1 + L_2 + L_{17} + L_{18} + L_{19} & L_1 + L_2 + L_3 + L_{18} + L_{19} & L_1 + L_{19} \\ L_1 + L_2 + L_{17} + L_{18} + L_{19} & L_{22} & L_1 + L_2 + L_{18} + L_{19} & L_1 + L_{19} \\ L_1 + L_2 + L_3 + L_{18} + L_{19} & L_1 + L_2 + L_{18} + L_{19} & L_{33} & L_1 + L_{19} \\ L_1 + L_{19} & L_1 + L_{19} & L_1 + L_{19} & L_{44} \end{bmatrix} \begin{bmatrix} di_{\text{M1}}/dt \\ di_{\text{M2}}/dt \\ di_{\text{M3}}/dt \\ di_{\text{M4}}/dt \end{bmatrix} \tag{B1}$$

$$\begin{cases} L_{11} = L_1 + L_2 + L_3 + L_5 + L_9 + L_{13} + L_{16} + L_{17} + L_{18} + L_{19} \\ L_{22} = L_1 + L_2 + L_4 + L_8 + L_{12} + L_{17} + L_{18} + L_{19} \\ L_{33} = L_1 + L_2 + L_3 + L_6 + L_{10} + L_{14} + L_{18} + L_{19} \\ L_{44} = L_1 + L_7 + L_{11} + L_{15} + L_{19} \end{cases} \tag{B2}$$

$$\begin{cases} i_{\text{M2}} - i_{\text{M1}} = \left[(L_5 + L_9 + L_{13} + L_{16}) \frac{di_{\text{M1}}}{dt} - (L_4 + L_8 + L_{12}) \frac{di_{\text{M2}}}{dt} + L_3 \frac{d(i_{\text{M1}} + i_{\text{M3}})}{dt} \right] / Ron \\ i_{\text{M3}} - i_{\text{M2}} = \left[(L_4 + L_8 + L_{12}) \frac{di_{\text{M2}}}{dt} - (L_6 + L_{10} + L_{14}) \frac{di_{\text{M3}}}{dt} - L_3 \frac{d(i_{\text{M1}} + i_{\text{M3}})}{dt} + L_{17} \frac{d(i_{\text{M1}} + i_{\text{M2}})}{dt} \right] / Ron \\ i_{\text{M4}} - i_{\text{M3}} = \left[(L_6 + L_{10} + L_{14}) \frac{di_{\text{M3}}}{dt} - (L_7 + L_{11} + L_{15}) \frac{di_{\text{M4}}}{dt} + (L_2 + L_{18}) \frac{d(i_{\text{M1}} + i_{\text{M2}} + i_{\text{M3}})}{dt} + L_3 \frac{d(i_{\text{M1}} + i_{\text{M3}})}{dt} \right] / Ron \\ i_{\text{M4}} - i_{\text{M1}} = \left[(L_5 + L_9 + L_{13} + L_{16}) \frac{di_{\text{M1}}}{dt} - (L_7 + L_{11} + L_{15}) \frac{di_{\text{M4}}}{dt} + (L_2 + L_{18}) \frac{d(i_{\text{M1}} + i_{\text{M2}} + i_{\text{M3}})}{dt} + L_{17} \frac{d(i_{\text{M1}} + i_{\text{M2}})}{dt} \right. \\ \qquad \left. + L_3 \frac{d(i_{\text{M1}} + i_{\text{M3}})}{dt} \right] / Ron \end{cases} \tag{B3}$$

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$$\begin{bmatrix} 29.54 & 28.49 & 28.45 & 28.22 & 27.97 & 27.82 & 27.71 & 27.63 \\ 28.75 & 29.27 & 28.57 & 28.33 & 28.05 & 27.90 & 27.79 & 27.71 \\ 28.49 & 28.57 & 29.12 & 28.45 & 28.19 & 28.02 & 27.90 & 27.82 \\ 28.19 & 28.33 & 28.45 & 29.05 & 28.43 & 28.23 & 28.22 & 27.97 \\ 27.97 & 28.22 & 28.23 & 28.43 & 29.05 & 28.45 & 28.33 & 28.19 \\ 27.82 & 27.90 & 28.02 & 28.19 & 28.45 & 29.12 & 28.57 & 28.49 \\ 27.71 & 27.79 & 27.90 & 28.05 & 28.33 & 28.57 & 29.27 & 28.75 \\ 27.63 & 27.71 & 27.82 & 27.97 & 28.22 & 28.45 & 28.49 & 29.54 \end{bmatrix} \tag{C1}$$

$$\begin{bmatrix} 0.2317 & 0.0234 & 0.0156 & 0.0037 & 0.0017 & 0.0005 & 0.0003 & 0.0001 \\ 0.0243 & 0.2319 & 0.0231 & 0.0162 & 0.0026 & 0.0018 & 0.0005 & 0.0004 \\ 0.0184 & 0.0242 & 0.2307 & 0.0233 & 0.0108 & 0.0026 & 0.0017 & 0.0006 \\ 0.0055 & 0.0189 & 0.0242 & 0.2367 & 0.0153 & 0.0113 & 0.0026 & 0.0002 \\ 0.0002 & 0.0026 & 0.0113 & 0.0153 & 0.2367 & 0.0242 & 0.0189 & 0.0055 \\ 0.0006 & 0.0017 & 0.0026 & 0.0108 & 0.0233 & 0.2307 & 0.0242 & 0.0184 \\ 0.0004 & 0.0005 & 0.0018 & 0.0026 & 0.0162 & 0.0231 & 0.2319 & 0.0243 \\ 0.0001 & 0.0003 & 0.0005 & 0.0017 & 0.0037 & 0.0156 & 0.0234 & 0.2371 \end{bmatrix} \tag{C2}$$

$$\begin{bmatrix} 0.2395 & 0.0546 & 0.0169 & 0.0063 & 0.0018 & 0.0008 & 0.0004 & 0.0002 \\ 0.0568 & 0.2326 & 0.0530 & 0.0166 & 0.0043 & 0.0018 & 0.0008 & 0.0004 \\ 0.0200 & 0.0547 & 0.2318 & 0.0535 & 0.0112 & 0.0045 & 0.0019 & 0.0009 \\ 0.0096 & 0.0193 & 0.0553 & 0.2373 & 0.0331 & 0.0116 & 0.0045 & 0.0021 \\ 0.0021 & 0.0045 & 0.0116 & 0.0331 & 0.2373 & 0.0553 & 0.0193 & 0.0096 \\ 0.0009 & 0.0019 & 0.0045 & 0.0112 & 0.0535 & 0.2318 & 0.0547 & 0.0200 \\ 0.0004 & 0.0008 & 0.0018 & 0.0043 & 0.1166 & 0.0530 & 0.2326 & 0.0568 \\ 0.0002 & 0.0004 & 0.0008 & 0.0018 & 0.0063 & 0.0169 & 0.0546 & 0.2395 \end{bmatrix} \tag{C3}$$

C. Simulation and Experiment Results

(C1)–(C3) shown at the top of this page.

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Fengtao Yang (Student Member, IEEE) was born in Shandong, China, in 1994. He received the B.S. degree in electronic and electrical engineering from the China University of Mining and Technology, Xuzhou, China, in 2016. He is currently working toward the Ph.D. degree in electronic and electrical engineering with Xi'an Jiaotong University, Xi'an, China.

His current interests include advancement in electrical performance, thermal management, operation temperature, power density and integration of power modules, especially applied in wide-bandgap semiconductor device-based, high-current, high-temperature, high-frequency power conversion systems.

Lixin Jia (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1989, 1992, and 2003, respectively.

He was an Associate Professor in 2005. He is currently a Professor with the School of Electrical Engineering, Xi'an Jiaotong University. His main research interests include the application of industrial intelligent control in power systems and the applications of power electronics in power systems.

Laili Wang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China, in 2004, 2007, and 2011, respectively.

Since 2011, he has been a Postdoctoral Research Fellow with the Department of Electrical Engineering, Queen's University, Kingston, ON, Canada. From 2014 to 2017, he was an Electrical Engineer with Sumida, Pointe Claire, QC, Canada. In 2017, he was a Full Professor with Xi'an Jiaotong University. His research interests include package and integration, wireless power transfer, and energy harvesting.

Dr. Wang is currently an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is the Vice Chair of TC2 (Technical Committee of Power Conversion Systems and Components) in Power Electronics Society (PELS), Co-Chair of System Integration and Application in ITRW (International Technology Roadmap for Wide Band-Gap Power Semiconductor), and the Chair of IEEE China Power Supply Society and PELS Joint Chapter in Xi'an, China.

Fan Zhang (Member, IEEE) was born in Shaanxi, China, in 1990. He received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2012 and 2018, respectively.

From March 2017 to March 2018, he was a Visiting Scholar with the Center for High-Performance Power Electronics, The Ohio State University, Columbus, OH, USA. Since 2018, he has been a Faculty Member with the School of Electrical Engineering, Xi'an Jiaotong University, where he is currently an Associate Professor. His research interests include applications of power semiconductor devices, high-voltage converter topologies, and solid-state circuit breaker.

Binyu Wang (Student Member, IEEE) was born in Shaanxi, China, in 1993. He received the B.S. degree in electrical engineering in 2015 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree in electronic and electrical engineering.

His research interests include the reliability of power semiconductor modules and thermal management in modular multilevel converters.

Cheng Zhao (Student Member, IEEE) was born in Shanxi, China, in 1996. He received the B.S. degree in electrical engineering from Jilin University, Changchun, China, in 2017. He is currently working toward the Ph.D. degree in electronic and electrical engineering with Xi'an Jiaotong University, Xi'an, China.

His research interests include packaging and applications of power semiconductor devices and parallel operation of SiC MOSFETs.

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Jianpeng Wang (Student Member, IEEE) was born in Heilongjiang, China, in 1995. He received the B.S. degree in electrical engineering in 2017 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree in electronic and electrical engineering.

His research interests include the packaging and reliability of power semiconductor modules.

Christoph Friedrich Bayer was born in Albertshofen, Germany, on June 27th, 1987. He received the German Diploma in physics from the University of Würzburg , Würzburg, Germany, in 2011.

In the beginning of 2012, he was with the Fraunhofer Institute for Integrated Systems and Device Technology, Erlangen, Germany, where he works on electrical, thermal, and mechanical simulations for applications in power electronics. After three years, he switched to the devices and reliability department while still focusing on simulation for packaging and testing topics in power electronics.

Braham Ferreira (Fellow, IEEE) received the Ph.D. degree in electrical engineering from Rand Afrikaans University, Johannesburg, South Africa.

In 1981, he was with the Institute of Power Electronics and Electric Drives, Technical University of Aachen, Aachen, Germany, and was a System Engineer with ESD Pty (Ltd.) from 1982 to 1985. From 1986 to 1997, he was with the Department of Electrical Engineering, Rand Afrikaans University, where he held the Carl and Emily Fuchs Chair of Power Electronics in later years. From 1998 to 2018, he was the Chair in Power Electronics and Electrical Machines, Delft University of Technology, Delft, The Netherlands. He was the Head of the Department from 2006 to 2010 and was the Director of the Delft-Beijing Institute of Intelligent Science and Technology, from 2017 to 2018. He is currently a Professor of power electronics with the University of Twente, Enschede, The Netherlands. He is the author or the coauthor of 100 journal and transactions articles, 300 conference articles, and 15 patents.

Dr. Ferreira was the recipient of the 15 Prize Paper Awards, the IEEE IAS Gerald Kliman Innovator Award, and the IAS Outstanding Achievement Award. He is the Chair of the IEEE ITRW. He was the President of the IEEE Power Electronics Society, from 2015 to 2016.

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