# Materials Characterization of CIGS solar cells on Top of CMOS chips

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## ABSTRACT

In the current work, we present a detailed study on the material properties of the CIGS layers, fabricated on top of the CMOS chips, and compare the results with the fabrication on standard glass substrates. Almost identical elemental composition on both glass and CMOS chips (within measurement error). From X-ray diffraction measurement, except two peaks from the Si <100> substrate, the diffraction peaks from CIGS solar cell CMOS chip and that on glass substrate coincide for all three temperatures. Helium ion microscope images of the cross-section and top view of the CIGS layers, shows that the grain size is suitable for high efficiency solar cells.

## INTRODUCTION

Ubiquitous computing [1] requires the development of hundreds of working micro-electronic devices everywhere and whenever [2]. Traditional power supplies cannot meet the energy needs of such systems: cable wiring is prohibitively expensive and sometimes unavailable; contemporary batteries can only supply very little total energy (~1-3 J/mm$^3$) until they run out; and their lifetime is anyway limited to 1-3 years [3, 4]. The development of new batteries is slow: *the energy density of batteries has only increased by a factor of five over the last two centuries* [5, 6].

Advances in low-power Complementary Metal Oxide Semiconductor (CMOS) very large scale integration (VLSI) have led to the dramatic decreases in power consumption. Theoretically, it was predicated that the power consumption of different motes will be below 10 μW in the foreseeable future [7]; practically, it was reported that a CMOS image sensor can operate continuously at 70 μW/cm$^2$ [8] and a temperature sensor requires less than 40 $\mu$W continuous power supply [9]

*Energy scavenging*-also known as *Energy harvesting*-has recently drawn huge interests in both academia and industry. The concept is to power micro-electronic devices by gathering energy from the environment surrounding the device itself. It is a potential solution for powering various low power electronic devices for autonomous systems; that is, maintenance free systems. Different approaches exist for the energy harvesting, and Lu *et al*. [10] describe the effects of trying to monolithically integrating solar cells on top of CMOS chips as energy harvesters to convert light into electricity, thus to power the underneath integrated circuits (IC). Fig. 1 shows an envisaged system design for such PV energy harvesters.

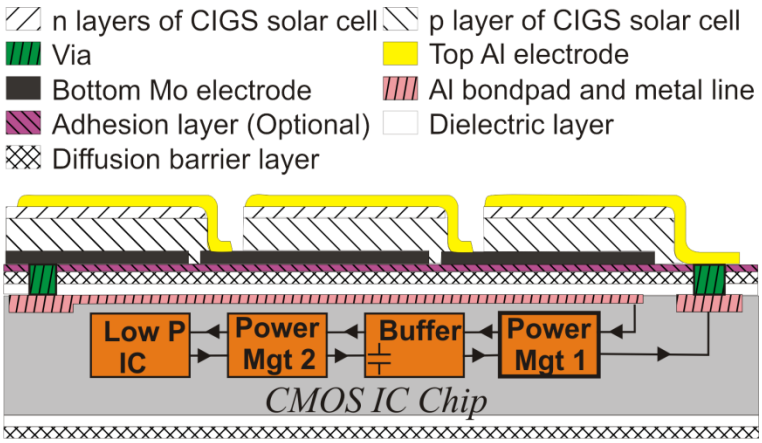


**Fig. 1. Envisaged autonomous microchip comprising of a PV cell for energy collection, power management circuits, integrated energy storage (e.g. high-density capacitor or solid-state battery) and low-power circuits. The PV cell can be realized on the chip's front or back side.**

The $Cu(In_{1-x}Ga_x)Se_2$ (CIGS) solar cell is a competitive candidate for the light harvesters due to its high photovoltaic (PV) efficiency [11], long term reliability, and good radiation hardness [12]. The monolithically integrated devices bear the promise of a smaller overall size, and reduced manufacturing cost per system. By creating a photovoltaic cell above an existing IC, the transistor and interconnect density are uncompromised. Integration of the CIGS *material* on top of CMOS was presented in [13]. In our recent article [10], we presented the results of the CMOS compatibility and the PV performance of the monolithic integration of CIGS *solar cells* on top of unpackaged 0.13-µm (Cu-PCM), 0.18-µm (Ring Oscillator) and 0.25-µm (Timepix) CMOS microchips. Here we presented the detailed analysis of the material properties of the CIGS layers on CMOS chip substrate, which is critical to assure the proper PV performance of the solar cells.

## EXPERIMENT

Fig. 2 shows the schematic view of a CIGS solar cell fabricated on top of a CMOS chip. After the CMOS electrical characterization, the chips were passivated, followed by the conventional CIGS solar cell process: magnetron-sputtering of Mo, then three-stage-co-evaporation of CIGS, chemical bath deposition of CdS, sputtering of intrinsic and Al-doped ZnO, then sputtering of the Al/Ni top electrode. Some samples were not further processed after the CIGS co-evaporation for characterization of the material's property of the CIGS layer only. After the PV characterization of the realized solar cell, the solar cell stack and the passivation layers were removed from some of the CMOS chips in order to test the CMOS chip again. The detailed experiment procedures were described somewhere else [10].

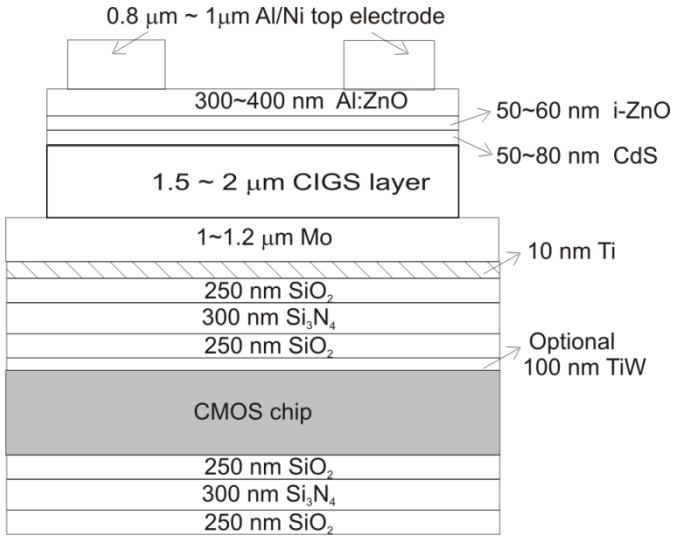


**Fig. 2. Schematic view of a CIGS solar cell fabricated on top of a CMOS chip (not to scale). The 100 nm TiW layer is only applied to Cu-PCM chips as an etch-stop layer; the SiO2, $Si_3N_4$ and $SiO_2$ thin films stacks are protecting passivation layers; 10 nm Ti is administrated between the top $SiO_2$ and the bottom Mo electrode for better adhesion. In these experiments, no interconnection was made between the solar cell and the CMOS.**

In order to make a fair comparison, a sample holder (see the left side in Fig. 3) was designed to fabricate the solar cells on CMOS chips and the glass reference in the same run, with the same process conditions. The samples, after the whole solar cell stack layers were finished, were also shown in the right side in Fig. 3.

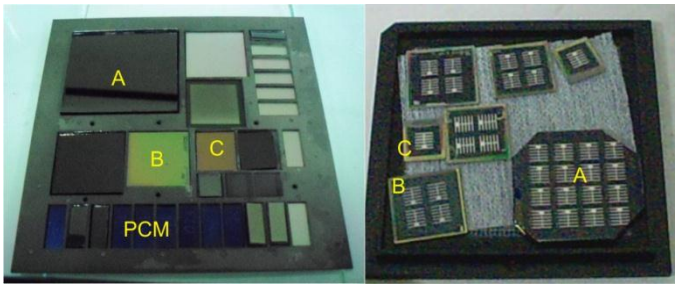


**Fig. 3: Left: 10x10 cm2 sample holder for different types of samples for CIGS solar cell deposition experiments. Right: finished samples with CIGS solar cells on top. In both images, A, B, C denote the glass reference plates, Cu-PCM chips and Timepix chips, respectively. Additional test samples are included in the same run.**

## Material characterization of the CIGS solar cell on CMOS chip

Our approach is to combine standard CMOS with standard PV processing, assuming that the two may take place in different manufacturing facilities. Trying to replace the standard soda lime glass substrate of CIGS solar cell by the CMOS chips may influence the properties of the CIGS layer, which will leads to a malfunctioned solar cell. In this section, we will present the material characterization of the CIGS solar cells by different methods.

### Physical characterization by Helium Ion Microscopy

Fig. 4 shows the images of the integrated CIGS solar cells on top of three generation CMOS chips. The solar cells have an active area of 0.29 $cm^2$, and the patterning was realized by mechanical scribing.

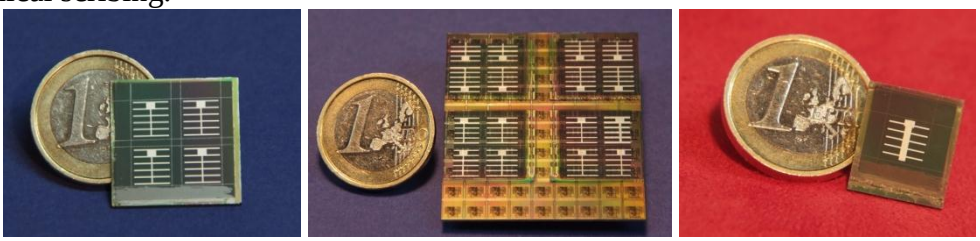

**Fig. 4. Imagines of integrated CIGS solar cells on top of the unpackaged 0.13-µm, 0.18-µm and 0.25-µm CMOS microchips. The integrated solar cells have an active area of 0.29 cm2, and the patterning between the cells are realized by mechanical scribing.**

Fig. 5 shows Helium Ion Microscope (HIM) [14] cross-sections of the CMOS chips with solar cells on top. On the left side in Fig. 3, we can see the metal levels of the CMOS chips, and the layer by layer structure of the CIGS solar cell on top of the CMOS chips. The CMOS has some topography (approximately 1 µm), as visible from the nonplanar solar cell thin films. The figure suggests that the step coverage of the solar cell layers is sufficient to cope with this topography. On the right side in Fig. 5 illustrates the crystal structure of the Mo, CIGS, ZnO and Al grid. The Mo and CIGS have columnar polycrystalline structure. The grain size of the Mo layer is around 60 nm, as derived from X-ray diffraction (XRD) data using the Scherrer equation. From the top-view HIM microscopy in Fig. 6, the grain size of the CIGS is well above half a micrometer, whichis similar as that of the reference cell on the glass substrate.. These grain sizes depend on the process conditions [15, 16], the obtained values are suitable for good CIGS solar cell performance.

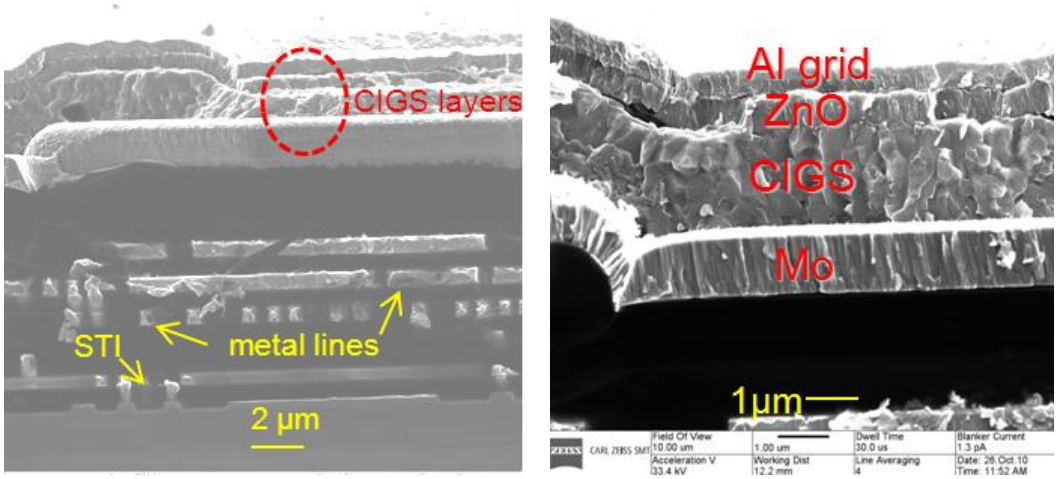


**Fig. 5. HIM images of the cross section view of the CIGS solar cell on top of the CMOS chip. Left: Going from bottom to top, the chip's shallow trench isolation and metal line interconnects are visible, followed by the CIGS solar cell layer stack. Right: Zoomed-in image of the CIGS solar cell layers on a CMOS chip. The columnar poly crystal structure of different layers can be distinguished in the picture**.

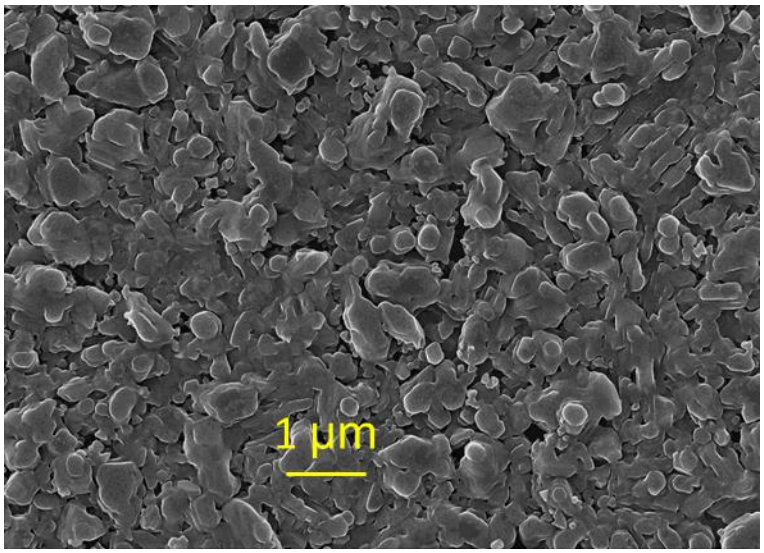


**Fig. 6. HIM image of top view of the CIGS layer (not the completed CIGS solar cell) on top CMOS chip. The grain size of CIGS on glass can also be larger than 0.5 µm, which is necessary for high efficiency CIGS solar cells.**

## Crystallinity analysis by X-ray Diffraction spectroscopy

$Cu(In_{1-x}Ga_x)Se_2$ (CIGS) is a semiconducting I-III-$VI_2$ compound with chalcopyrite poly crystal structure [17]. The main diffraction peaks are <112> and <220/204>. For higher efficiency CIGS solar cell, the peak ratio between <112> and <220/204> should be smaller [18, 19]. Fig. 7 shows the XRD measurements of the CIGS thin film on CMOS chip and that on glass substrate at different temperatures. For the same temperature, the CIGS thin films are deposited on these two substrates in the same run for the same temperature.

For all three temperatures, except two peaks from the Si <100> substrate, the diffraction peaks of the CIGS thin film on CMOS chip film coincide with that on glass substrate. But the peak ratio between <112> and <220/204> of the CIGS thin film on CMOS is larger than that on glass substrate, which results a lower PV efficiency on CMOS substrate [10]. However the peak ratio difference becomes smaller with the increasing temperature, also the ratio is still less than 4 for all three temperatures, which is suitable for high efficiency CIGS solar cells.

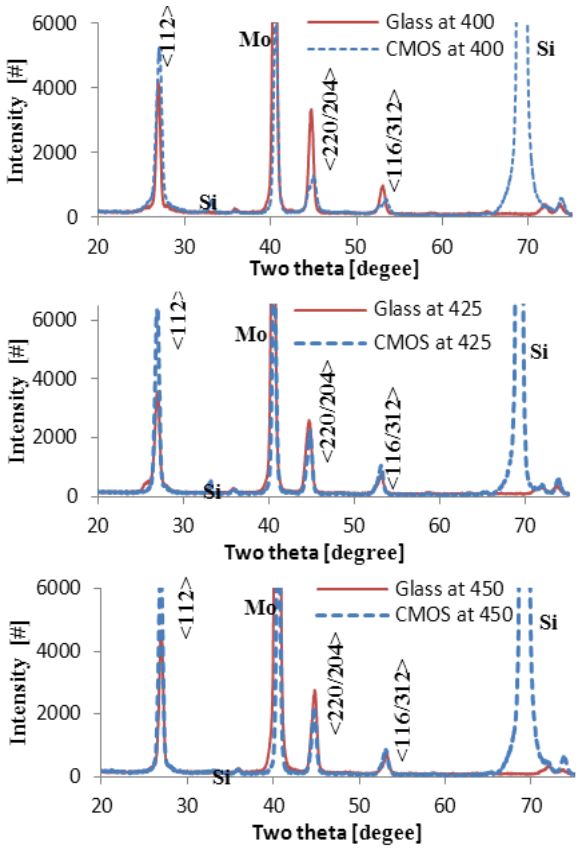


**Fig. 7. XRD data comparison of CIGS on glass substrate and that on Cu-PCM substrate fabricated at different temperatures. For all temperatures, except two peaks from the Si <100> substrate, the diffraction peaks from CMOS chip and glass substrate coincide. The peak ratio between <112> and <220/204> the on CMOS is larger than that on glass, but the ratio is still less than 4 for all temperatures.**

## Chemical composition analysis by X-ray fluorescence (XRF)

The CIGS thin film originated from $CuInSe_2$, which is a ternary compound. In order to tune the bandgap of this semiconductor material, part of the In atoms in the lattice are substituted by Ga atoms. However there is optimum Ga ratio for high PV efficiency, and for high PV efficiencies, each element should have their respective optimum percentages, which are listed in the second row of Table 1.

X-ray fluorescence was used to determine the atomic chemical composition of the CIGS thin film on glass and that on glass substrate. The results were listed in Table 1 and Fig. 8. From then we can see that identical composition on CMOS chip and on glass can be achieved, and they can also within the expected optimum values.

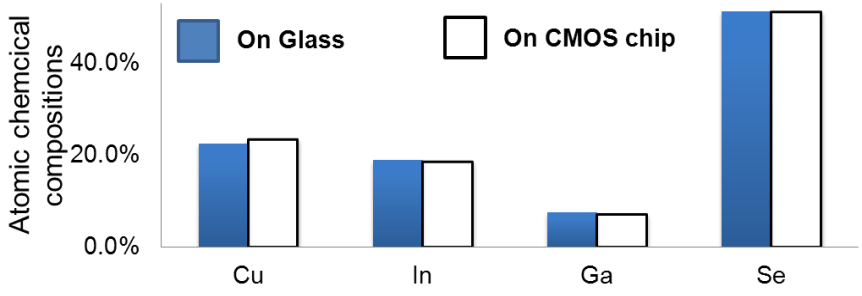

**Fig. 8. Atomic chemical composition comparisons of CIGS thin film on glass and on CMOS chip. The CIGS thin films are fabricated at 425 ºC.**

**Table 1: Atomic chemical composition by XRF of CIGS layers deposited on various substrates and at different temperatures.**

| T (ºC) | substrate | Cu (at.%) | In (at.%) | Ga (at.%) | Se (at.%) | Cu/ (In+Ga) | Ga/ (In+Ga) |
|---|---|---|---|---|---|---|---|
| | **Expected** | *22-24* | *19-20* | *6-7* | *50-51* | *0.88-0.91* | *0.25-0.27* |
| 400 | **Glass** | 22.8 | 18.7 | 7.6 | 51.0 | 0.87 | 0.29 |
| | **CMOS** | 22.5 | 18.0 | 8.2 | 51.2 | 0.86 | 0.31 |
| 425 | **Glass** | 22.4 | 18.9 | 7.5 | 51.2 | 0.85 | 0.28 |
| | **CMOS** | 23.4 | 18.5 | 7.1 | 51.1 | 0.84 | 0.28 |
| 450 | **Glass** | 23.6 | 20.8 | 4.8 | 50.2 | 0.92 | 0.19 |
| | **CMOS** | 22.7 | 21.5 | 4.4 | 50.3 | 0.87 | 0.17 |

## CONCLUSIONS

From comparison of the XRD and the XRF analysis of the CIGS layers, we conclude that an identical crystallinity and chemical composition can be obtained on CMOS and on glass. From HIM images, we can see that the CIGS on CMOS chip can have a columnar structure with the grain size larger than 0.5 μm.

Changing the substrate from glass to CMOS chip only have insignificant influence on the material properties of the CIGS solar cell layer.

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