THIS ARTICLE HAS BEEN ACCEPTED FOR PUBLICATION IN IEEE JOURNAL OF SOLID-STATE CIRCUITS. THIS IS THE AUTHOR'S VERSION WHICH HAS NOT BEEN FULLY EDITED AND CONTENT MAY CHANGE PRIOR TO FINAL PUBLICATION. CITATION INFORMATION: DOI 10.1109/JSSC.2023.3255741.

A Predistortion-less Digital MIMO Transmitter with DTC-Based Quadrature Imbalance Compensation

Joep Zanen, *Student Member, IEEE*, Eric Klumperink *Fellow, IEEE*, and Bram Nauta, *Fellow, IEEE*

***Abstract*—A 4-element multi-input multi-output (MIMO) switched capacitor power amplifier (SCPA) in 22nm fully depleted silicon-on-insulator (FD-SOI) is presented as a software-defined radio. To omit the digital predistortion (DPD) and digital quadrature correction power consumption of this wide modulation bandwidth MIMO transmitter, constant-conductance SCPA drivers and a wideband low-impedance power supply are used for linearization. Digital-to-time converter (DTC) based clock calibration is used for quadrature imbalance correction, improving image rejection to >53 dB. This allows for up to 80 MHz DPD-less single carrier 1024-quadrature amplitude modulation (QAM) transmission, with an error vector magnitude (EVM) <–39.4 dB. RF bandwidths up to 160 MHz are demonstrated for multi-carrier 1024QAM signals, supporting data rates up to 1.18 GBps. A second-order Chebyshev bandpass filter using bondwires as inductors is used as a matching network, supporting carrier frequencies from 1.64 GHz to 3.28 GHz, while omitting the required chip area for integrated inductors. MIMO experiments demonstrate the beamforming capabilities for single and multi-beam communication.**

***Index Terms*—CMOS integrated circuits, digital beamforming, radio frequency digital-to-analog converter (RF-DAC), switched capacitor power amplifier (SCPA), digital-to-time converter (DTC).**

I. Introduction

THE trend towards increasing data rates and number of simultaneous users in a crowded spectrum requires additional forms of diversity apart from frequency. Multi-input multi-output (MIMO) communication systems exploit spatial diversity, creating multiple channels, extending beyond the Shannon-Hartley limit for capacity per channel.

In MIMO applications with n_t transmit antennas and a normalized effective isotropic radiated power (EIRP), the transmit power per amplifier decreases with n_t^2 due to the array gain, but the required power for digital predistortion (DPD) increases with n_t or n_t^2 [1]. For increasing bandwidth and low EIRP, the power consumption for the DPD can exceed that of the power amplifier (PA) [1]. In these scenarios, system efficiency can benefit from a transmitter that is linear enough to function without DPD, even when this comes at the cost of PA drain efficiency. Direct digital RF transmitters have shown high DPD-less linearity with better than -35 dB error vector magnitude (EVM) [2]–[8], as required for 1024QAM [9], and are CMOS compatible. Direct digital RF transmitters for MIMO have been demonstrated [10]–[13] with a best achieved EVM of -30 dB [13]. In single-element applications, switched capacitor power amplifier (SCPA) digital transmitters with a DPD-less EVMs better than -40 dB have been demonstrated [6]–[8], indicating the potential for highly linear MIMO transmitters based on the SCPA concept.

This work is part of the TTW-research program MIRABEAM with project-number 14689, which is financed by the Dutch Research Council (NWO).

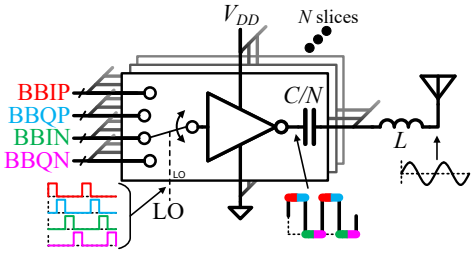


Fig. 1. A quadrature SCPA as a unary RF-DAC, generating an RF signal with four samples per carrier period to achieve quadrature modulation. Colors of the output waveform of the unit cell inverter indicate which baseband input is selected.

The SCPA has been introduced in [14] and consists of a digital multiplexer as mixer, and a capacitive digital-to-analog converter (DAC) to convert this signal to the analog domain. A series inductor is used to cancel the effect of the series capacitance on the SCPA output impedance. A quadrature SCPA implementation with quadrature combiner in the digital domain, before the DAC, is indicated in Figure 1. The mixer-DAC combination will be further referred to as a Radio Frequency DAC (RF-DAC). The quadrature implementation in Figure 1 gives 3dB more output power than a conventional quadrature transmitter with analog quadrature combination, and circumvents the bandwidth expansion of a polar transmitter [15], [16]. The unit cell inverter outputs can be regarded as the time multiplexed baseband inputs, constructing a modulated RF carrier of four samples per carrier period, achieving quadrature modulation, with timing controlled by the LO. The implementation based on switches and accurately matched capacitors makes it intrinsically highly linear [14]. This linearity is predominantly limited by the code-dependence output impedance [14], [17] and the quality of the power supply, as the supply voltage is the reference voltage for the RF-DAC [18]. Techniques to linearize the code-dependent output conductance have been proposed in [7], [8], and a wideband low-impedance supply was proposed in [19]. For wide modulation bandwidth, the supply impedance should remain low over a large frequency range, or nonlinear memory effects will occur.

For a highly linear SCPA, EVM can still be limited by quadrature imbalance rather than nonlinear distortion. In this case digital compensation is needed [8], which requires continuous processing in the digital domain, hence increasing digital

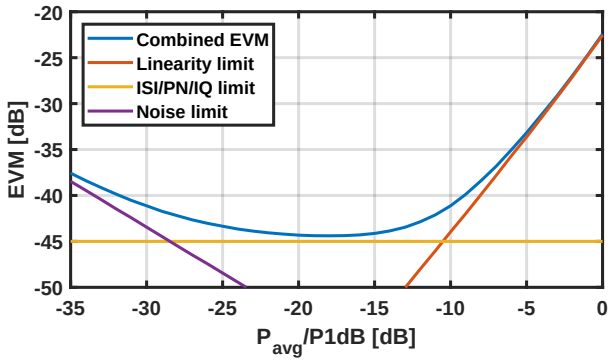


Fig. 2. Simulated EVM for a 1024QAM signal over back-off, including limits due to noise, due to ISI, phase noise (PN) and quadrature imbalance (IQ), and due to nonlinear distortion. Only ISI was simulated for the yellow line.

power consumption. Imbalance in the clock generation, clock distribution, or in the multiplexer in Figure 1 will result in quadrature imbalance and degrade EVM. These layout and mismatch effects are constant after production, and hence can be compensated for using a one-time calibration. A calibration technique using digital-to-time converters (DTCs) in the clock paths will be proposed to compensate the quadrature imbalance.

This work presents a MIMO SCPA in 22nm fully depleted silicon-on-insulator (FD-SOI) CMOS, with high image rejection using DTCs and calibration, high DPD-less linearity using constant output conductance driver cells [8], wide modulation bandwidth using a wideband power supply and matching network, and one octave of RF bandwidth. Section II discusses the EVM limits for 1024 quadrature amplitude modulation (QAM) signals, and the implications of using SCPAs for this application. In Section III the quadrature imbalance calibration technique is described. Section IV elaborates on a time-skewed reclocking technique, relaxing timing requirements for the baseband data. MIMO linearity considerations are discussed in Section V, and the chip implementation including a bondwire based Chebyshev matching network and a wideband low impedance supply is presented in Section VI. Section VII presents the single-element and MIMO measurement results. Section VIII concludes the work.

II. EVM LIMITS

The most dominant impairments limiting transmitter EVM include nonlinear distortion at high transmit power, phase noise, inter-symbol interference (ISI) and quadrature imbalance at medium transmit power, and thermal and quantization noise at low transmit power [7], [20]–[23]. Typically, these impairments result in a bathtub curve for EVM as a function of transmit power as in Figure 2. These impairments and the effect of using SCPAs will be discussed in this section, in order to clarify potential benefits of using an SCPA.

A. Low back-off: linearity

To increase power amplifier linearity, back-off can be applied to reduce the power P_{avg} of the modulated carrier, albeit at the cost of power efficiency [23]. A memory-less nonlinear amplifier can be described by a first-order plus third-order polynomial. MATLAB simulations have been run to model the distortion of a 1024QAM modulated carrier with a broadly used raised-root cosine transmit filter with a roll-off factor of 0.35. The resulting linearity limit over back-off has been indicated in red in Figure 2.

In [8], an EVM up to –45.5 dB was achieved. To leave a budget for other impairments, a 3 dB more strict linearity limit is set as a requirement. In the third-order model, this –48.5 dB EVM requires a back-off of –12.2 dB with respect to the 1-dB compression point (P1dB). From the measured $P_{\text{avg}} = 5.1$ dBm (3.2 mW) in [8] follows a required P1dB $=$ 17.3 dBm (54 mW). For a class A amplifier with a theoretical peak efficiency of 50% [23] and a peak power of 54 mW[1], this would result in a DC power consumption of 107 mW, while producing only 5.1 dBm of output power: a power efficiency of 3.0%. The SCPA in [8] however achieves a power efficiency of 8.8%, which is almost three times the power efficiency of an ideal class A amplifier with similar linearity. To the best of the authors' knowledge, no DPD-less transmitters have been published which feature both a better EVM and drain efficiency than the work in [8].

B. Medium back-off: ISI, phase noise, and IQ imbalance

In practice, when increasing back-off to improve linearity, EVM will be limited due to memory effects, phase noise, and quadrature imbalance [20]–[22]. Phase noise can be limited by using a clock source and distribution circuits with sufficiently low phase noise, requiring better than –44 dBc local oscillator (LO) integrated phase noise for 1024QAM [24]. Quadrature imbalance compensation will be discussed in Section III.

Bandwidth limitations and memory effects, such as thermal effects, and supply and bias modulation [25], lead to linear and nonlinear dispersion in the Volterra series transfer of a transmitter, respectively. This causes ISI. As an example of a linear dispersion effect due to a parasitic pole, a 0.56% (–45 dB) settling error remains during the transition from one symbol to the next[2]. This incurs an ISI of –45 dB, and consequently an equal EVM limit. This –45 dB ISI from symbol $x[n]$ to symbol $x[n+1]$ is modeled and its simulated effect on EVM is indicated in yellow in Figure 2. Phase noise and quadrature imbalance are not considered in this simulation. To achieve the EVM reported in [8], the ISI requirement is < -45.5 dB. In linear amplifier classes, EVM is limited by dispersion due to bandwidth limits in the signal path, bias networks and power supplies, as well as thermal memory effects [22], [26]. Typically, these bias, supply and thermal variations result in nonlinear dispersion, which are difficult to compensate for using DPD [22], [23].

SCPAs reduce the number of dispersion effects with respect to class A or AB amplifiers. Firstly, due to the largely digital architecture, a large number of parasitic poles in the analog

[1]Assuming the third-order model is applicable up to P1dB, and P1dB is not limited by e.g. clipping to the supplies.

[2]This implies a (baseband equivalent) pole frequency f_{p} relative to the symbol rate f_{sym} as: $f_{\text{p}} = -\frac{1}{2\pi}\ln\left(10^{-\frac{45}{20}}\right) f_{\text{sym}} = 0.82 f_{\text{sym}}$

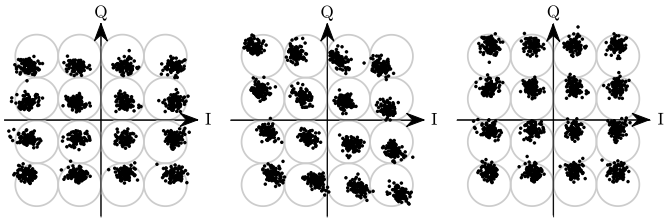


Fig. 3. Examples of 16QAM constellations with (a) quadrature gain imbalance, (b) quadrature phase imbalance and (c) LO leakage.

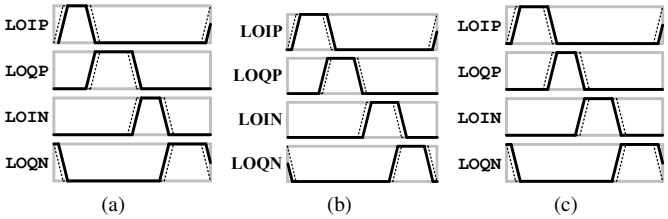


Fig. 4. Adjusted clocks to correct for (a) gain imbalance, (b) phase imbalance and (c) LO leakage (nominal clocks in dashed lines). Combinations possible.

signal path of conventional transmitters are eliminated. Secondly, there are no DC transistor biasing networks with their respective nonlinear memory effects [22], [23]. The supply voltage does function as a DC reference voltage for the SCPA, but as this is only one node, it is feasible to add large off-chip decoupling and multiple bondwires to keep the impedance of this node low, as will be discussed in Section VI-C. Lastly, as the SCPA output power is determined by capacitor ratios rather than gain from temperature sensitive transconductances, the SCPA is also much less susceptible to temperature variations and hence thermal memory effects. This temperature stability will be demonstrated in Section VII-D. Memory effects via the power supply can be minimized with a wideband low impedance supply.

C. Large back-off: noise

At large back-off, EVM is limited by both thermal and quantization noise. In an SCPA, the only analog node is the low-impedance and rail-to-rail swing RF output, where thermal noise is of little concern. As the SCPA is a DAC, its quantization also degrades EVM at large back-off [7]. Minimizing this to acceptable levels can be achieved by using a sufficient number of bits and oversampling ratio.

In conclusion, SCPAs are a promising candidate for low EVM DPD-less transmitters due to their high linearity for their power consumption, limited electrical and thermal memory effects, and low thermal noise due to their largely digital implementation and low impedance output stage.

III. Quadrature Imbalance Compensation

For highly linear transmitters, quadrature imbalance can become the limiting factor for EVM,as indicated by the EVM floor in Figure 2. Quadrature imbalance can stretch, shear or offset a QAM constellation as illustrated in Figure 3. Contrary to classical transmitters, the baseband signals are in the digital domain, and no analog quadrature mismatch compensation can be applied at baseband. In [8], compensation for these effects in the digital domain is used to meet the 1024QAM EVM. This compensation does require digital signal processing on every baseband sample, and thus power. Alternatively, [27] demonstrates circuit level image and LO leakage reduction to $<$–64 dBc, using signal sign changes in the clock path instead of the data path.

In transmitter transmitter, we propose to suppress quadrature imbalance by using clock phase calibration as in Figure 4. The gain imbalance in Figure 3a is restored by decreasing I and increasing Q duty-cycles as in Figure 4a, the quadrature phase imbalance in Figure 3b is restored by moving I backward and Q forward in time as in Figure 4b, and the LO leakage in Figure 3c are be restored by decreasing IP and increasing IN duty cycle as in Figure 4c. These clock adjustments could be realized using a DTC clock buffer with programmable delay for both rising and falling edges.

The required delay resolution is finest at the maximum operating frequency of 3.28 GHz, where one programmable unit delay step results in the largest phase step, and most relaxed at the minimum operating frequency of 1.64 GHz. MATLAB simulations indicate a resolution of 427 fs or 213 fs is required to keep the effects of quadrature imbalance on EVM below -50 dB for a 1.64 or 3.28 GHz carrier, respectively, such that quadrature imbalance has a negligible effect on EVM compared to other transmitter impairments. The maximum mismatch in clock propagation delay which was compensated for in [8] was 3.5 ps. A range of 10 ps for the DTCs in this design covers this maximum with a factor 3 margin.

For each of the four quadrature clock phases in every transmitter, a DTC as in Figure 5 is added. The DTC has a 6-bit programmable drive strength to drive internal net v_{slew}. The 75 always-on and 63 programmable slices give the desired range and resolution. The decoder, buffers and inverters are digital library cells, and the unit slices are based on tri-state buffers from the digital library, modified to have separate control for the PMOS and NMOS. Transistor MN3 functions as a load capacitance. The basis on digital library cells results in a compact DTC layout of 12$\times$15 µm. Using local digital buffers for the control signals and a low-impedance supply network, the simulated post-layout performance in Figure 6 is achieved. The most strict 213 fs resolution requirement at 3.28 GHz is met for codes 0 up to 38 in Figure 6b. This results in a tuning range of 6 ps in Figure 6a, which covers the mismatch found in [8] with a margin of a factor 1.7 which is a smaller safety margin than the desired factor 3 in this worst-case scenario. Image rejection measurements in Section VII indicate the range and resolution suffice in this design for carrier frequencies up to 3 GHz.

The DTC delay from CLK_{IN} to CLK_{OUT}in Figure 5 is kept minimal by using a high drive-strength DTC slices, in the range of 34 to 48 ps, and the currents during a transition are high due to the fast slew rate. These short delays and large currents result in negligible phase noise [28] related

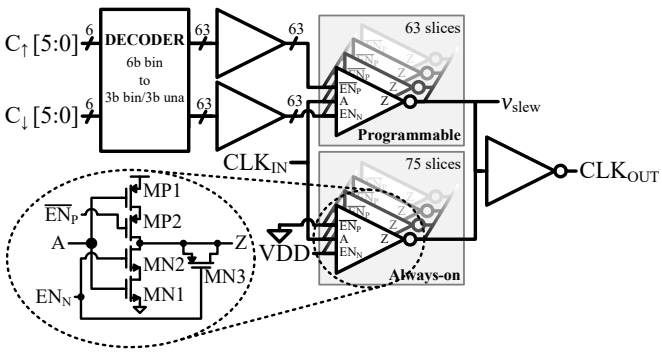
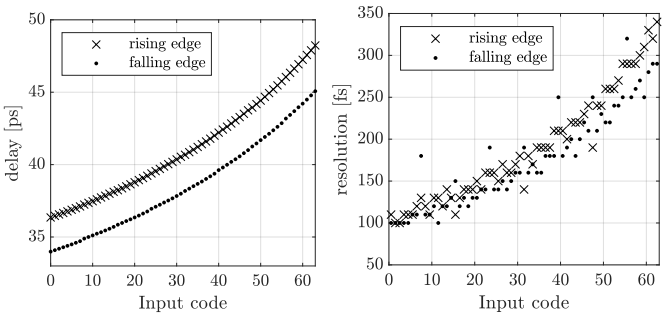


Fig. 5. DTC circuit based on digital library cells. Transistor MN3 functions as a load capacitance.



(a) (b)

Fig. 6. (a) Simulated post-layout Δt tuning range and (b) resolution for both rising and falling edges.

EVM degradation compared to the the effects of RF-DAC nonlinearity and quantization noise. As the load capacitance to the clock network on $\mathrm{CLK_{OUT}}$ is much larger than the parasitic capacitances in the DTC circuit, increasing the buffer width for drive strength does not have a significant impact on clock power consumption.

There are eight clock edges to calibrate in each SCPA: an optimization problem with eight degrees of freedom. The adjusted clocks in Figure 4 however show how to correct for quadrature imbalance and LO leakage. Measurements in Section VII indicate LO leakage in this system is small, so only quadrature phase and gain imbalance need to be calibrated for. To support this, two calibration parameters are proposed:

1) Phase correction code C_ϕ: to shift the I LO backward and Q LO forward in time as in Figure 4b.
2) Gain correction code $\mathrm{C}_{\hat{A}}$: to decrease the I LO duty cycle and increase the Q LO duty cycle as in Figure 4a.

These codes can have positive and negative values. The DTC codes for the clock edges are chosen as:

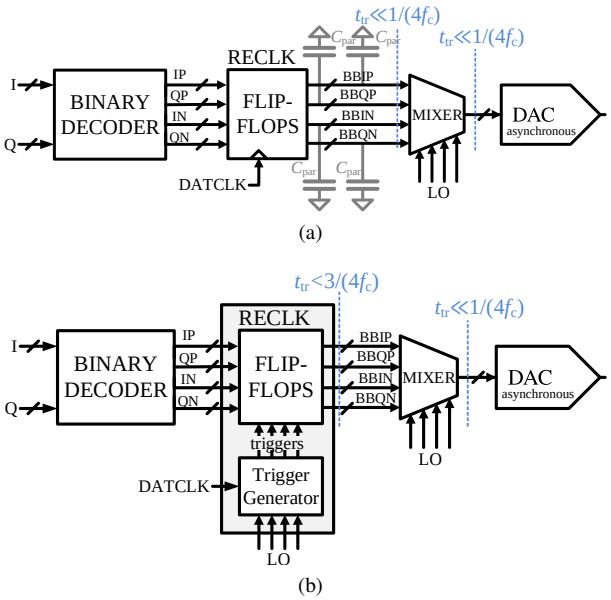


Fig. 7. (a) Conventional reclocking where all baseband inputs are reclocked at the same time. (b) Time-skewed reclocking. Maximum transition times t_{tr} are indicated in blue.

$$\mathrm{C_{IP\uparrow}} = +\mathrm{floor}((\mathrm{C}_\phi+1)/2) + \mathrm{floor}((\mathrm{C}_{\hat{A}}+1)/2) + B \quad (1a)$$
$$\mathrm{C_{IP\downarrow}} = +\mathrm{floor}((\mathrm{C}_\phi+1)/2) - \mathrm{floor}((\mathrm{C}_{\hat{A}}+1)/2) + B \quad (1b)$$
$$\mathrm{C_{QP\uparrow}} = -\mathrm{floor}((\mathrm{C}_\phi+0)/2) - \mathrm{floor}((\mathrm{C}_{\hat{A}}+0)/2) + B \quad (1c)$$
$$\mathrm{C_{QP\downarrow}} = -\mathrm{floor}((\mathrm{C}_\phi+0)/2) + \mathrm{floor}((\mathrm{C}_{\hat{A}}+0)/2) + B \quad (1d)$$
$$\mathrm{C_{IN\uparrow}} = +\mathrm{floor}((\mathrm{C}_\phi+1)/2) + \mathrm{floor}((\mathrm{C}_{\hat{A}}+1)/2) + B \quad (1e)$$
$$\mathrm{C_{IN\downarrow}} = +\mathrm{floor}((\mathrm{C}_\phi+1)/2) - \mathrm{floor}((\mathrm{C}_{\hat{A}}+1)/2) + B \quad (1f)$$
$$\mathrm{C_{QN\uparrow}} = -\mathrm{floor}((\mathrm{C}_\phi+0)/2) - \mathrm{floor}((\mathrm{C}_{\hat{A}}+0)/2) + B \quad (1g)$$
$$\mathrm{C_{QN\downarrow}} = -\mathrm{floor}((\mathrm{C}_\phi+0)/2) + \mathrm{floor}((\mathrm{C}_{\hat{A}}+0)/2) + B \quad (1h)$$

Where subscripts IP/QP/IN/QN indicate the four quadrature LO signals, and ↑/↓ indicate the rising and falling clock edges, respectively. Every even C_ϕ value, $\mathrm{floor}((\mathrm{C}_\phi+1)/2)$ increases by one (for the I codes), and at every odd C_ϕ value, $\mathrm{floor}((\mathrm{C}_\phi+0)/2)$ increases by one (for the Q codes). Analogously, this applies to the $\mathrm{C}_{\hat{A}}$ terms. Compared to linear mapping, taking the gain and phase correction codes out of the floor operations[3], an intermediate step is added, increasing resolution. The constant B is chosen such that the lowest DTC code is zero. This keeps the DTC delay near its minimum, where the resolution is finest. The C_ϕ and $\mathrm{C}_{\hat{A}}$ approach reduces the degrees of freedom from eight to two, simplifying calibration. The routing of the clock distribution network can result in a layout dependent LO time skew, which is unequal for the different transmitters. To compensate this mismatch, all four transmitters will need to be calibrated individually.

IV. Time-skewed Reclocking

Conventional digital quadrature modulators in [15], [27], [29] apply reclocking of the baseband signals before the

[3]Replacing 'floor$((\mathrm{C}_\phi+1)/2)$' by C_ϕ, and similarly for the other floor operations.

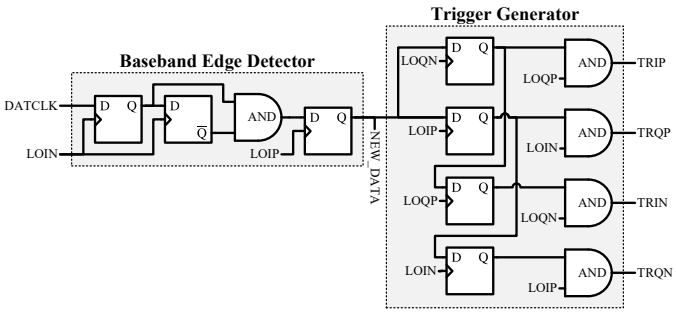


Fig. 8. Trigger generator circuit based on digital library cells.

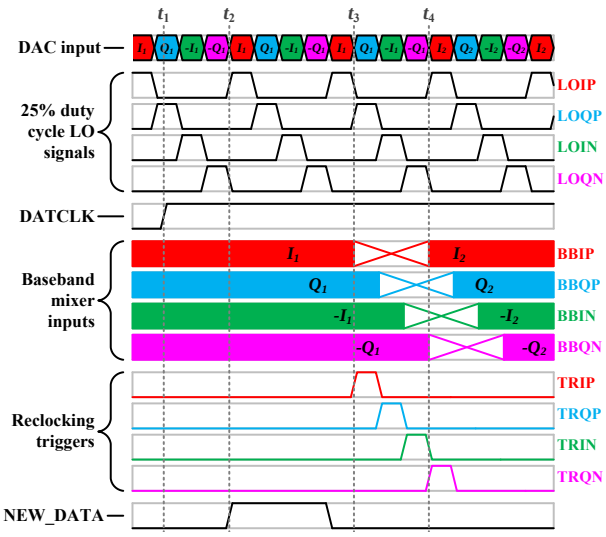


Fig. 9. Waveforms for the time-skewed trigger generator with indicated transition times for the baseband signals.

mixer, as indicated in Figure 7a. After a rising edge in the baseband clock signal DATCLK, the thermometer coded quadrature baseband signals BBIP, BBQP, BBIN and BBQN will transition simultaneously. To minimize the parasitics on the signal between the mixer and the DAC, the mixer cells are typically implemented inside the DAC unit cells, as was indicated in Figure 1. As the physical locations of these unit cells are distributed over the RF-DAC, the routing of the baseband signals is not matched in terms of length and parasitic capacitances C_{par}. At the input of the mixer cells, this time mismatch can lead to glitching using conventional reclocking, if some of the thermometer coded bits arrive before others do. As the quadrature mixer in Figure 7a always multiplexes one of its four inputs to the DAC, this glitching is propagated to the DAC. Transmission times t_{tr} much shorter than the LO pulse width are required for the mixer inputs to minimize this glitching: $t_{\text{tr}} \ll 1/(4f_c)$. For long wiring of the reclocked baseband signals with limited node bandwidth [30] and high f_{c}, this becomes increasingly difficult.

The digital mixer only selects each input 25% of the carrier period. The remaining 75% can be exploited for transition times when using time-skewed triggers instead of a shared reclocking signal for all four quadrature baseband signals, as indicated in Figure 7b. To generate the required reclocking triggers, the circuit in Figure 8 is used. A timing diagram is given in Figure 9. At time t_1, a rising edge in baseband clock DATCLK indicates new quadrature baseband data is available. At the next rising edge of LOIP at time t_2, a signal NEW_DATA is set high to start a sequence of retiming triggers. At the falling edge of LOIP, a trigger TRIP is generated to update the BBIP input during the 75% window where this input is unselected. Similar triggers are generated for the other baseband inputs, with a skew of $1/(4f_{\text{c}})$ to each next trigger, reclocking the respective baseband data during the 75% windows.

In this retiming approach, the clock rate of the signals before the mixer is limited to the baseband sample rate, the retimed quadrature signals require a transition time of $t_{\text{tr}} < 3/(4f_{\text{c}})$ rather than $t_{\text{tr}} \ll 1/(4f_{\text{c}})$ using conventional reclocking, and only the signals between the mixer and DAC need to have sharp transitions relative to the $4f_{\text{c}}$ DAC sample rate.

V. MIMO SCPA Linearity Considerations

A. Code-dependent output impedance

Typically, SCPA linearity is limited by AM-PM distortion due to unequal output impedance of switching and non-switching driver cells, resulting in a code-dependent output impedance [7], [8], [14], [17]. A highly linear SCPA exploiting output conductance linearization was proposed in [8], achieving a DPD-less EVM of -45.5 dB and an adjacent channel leakage ratio (ACLR) of -50 dB. The modified SCPA driver cells with drain resistors in Figure 10a linearize the output conductance g_{cell} over input voltage V_{in}. When the drain resistors are much smaller than the transistor on-resistances $R_{\text{D}} \ll R_{\text{on}}$, the drain resistors can be neglected. For logic 'high' and 'low' input signals V_{in}, $g_{\text{cell}} = 1/R_{\text{on}}$. Halfway a transition between the states, when $V_{\text{in}} \approx V_{\text{DD}}/2$, both transistors operate in the saturation region, resulting in a low output conductance. g_{cell} has a dip during the transition, as indicated by the dashed line in Figure 10b. When $R_{\text{D}} \gg R_{\text{on}}$ and logic 'high' and 'low' inputs are applied, R_{on} can be neglected and $g_{\text{cell}} = R_{\text{D}}$. Halfway during the transition, both transistors conduct, and the driver output conductance is the parallel of the two drain resistors $g_{\text{cell}} = 2/R_{\text{D}}$, resulting in a peak in output conductance, as indicated by the dash-dot line in Figure 10b.

The optimal value for R_{D} was found using DC simulations, where the output impedance of the driver neither has a peak or a dip, indicated by the solid line in Figure 10b, and the effective output conductance of switching and a non-switching drivers are equal, canceling the dominant source of distortion in SCPAs. Transient simulations and measurements in [8] indicate this DC optimized R_D also cancels amplitude modulation to phase modulation (AM-PM) distortion. Back-bias voltages V_{b1} and V_{b2} allow for NMOS and PMOS on-resistance calibration, respectively [8]. By scaling the widths of all components in Figure 10a, the SCPA output impedance remains low, to limit power efficiency degradation. As derived

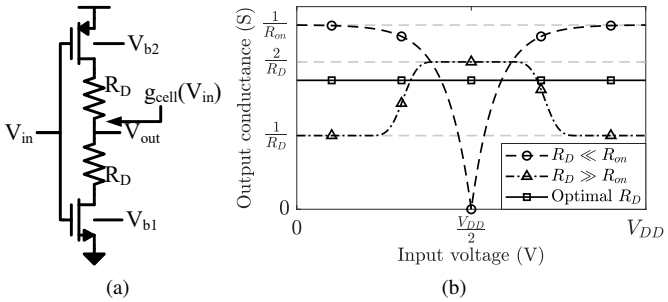


Fig. 10. Constant output conductance driver cell from [8]. (a) Circuit. (b) Sketched output conductance.

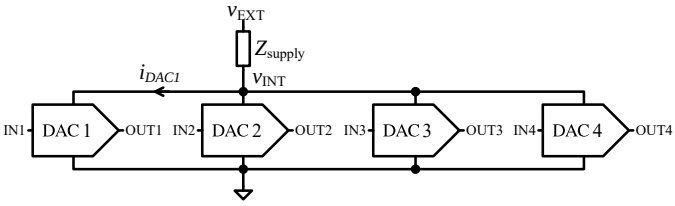


Fig. 11. Code-dependent supply currents to one of the RF-DACs result in a drop in internal supply voltage, affecting linearity for all RF-DACs.

in [8], the simulated peak drain efficiency drops from 50% to 39% when adding these linearization drain resistors. This sizing was re-used in this design. Increasing linearity by operating at 6 dB back-off will degrade drain efficiency more than this, as will be indicated in Figure 19b. Technology nodes with shorter gate lengths decrease both the gate capacitance and R_{on} of the used transistors. As SCPA AM-PM conversion is proportional to R_{on} [17], the short core devices in the used 22nm FD-SOI technology give an additional benefit with respect to other published high linearity SCPAs [5]–[7].

B. Power supply impedance

Apart from code-dependent SCPA output impedance, linearity is limited by the power supply quality. A single supply voltage is assumed, with a Thévenin equivalent supply voltage of v_{EXT} and supply impedance of Z_{supply}. This supply can be either on-chip or off-chip. Code-dependent supply current will result in a voltage drop over Z_{supply}, regardless of whether star connections to ground and the supply are used. As the SCPA is a DAC with its supply as reference voltage, this will result in nonlinear behavior [18], [19]. When multiple SCPAs are connected to the same power supply as in Figure 11, this can result in forms of cross-intermodulation. When DAC1 draws a code-dependent supply current i_{DAC1}, this results in a drop in the internal supply voltage v_{INT}. This will not only result in supply-induced distortion in DAC1, but in all four RF-DACs connected to this supply as a form of nonlinear crosstalk. This effect is limited by keeping Z_{supply} as low as possible over a wide frequency range, as will be elaborated in Section VI.

C. Nonlinear coupling

Linearity of MIMO transmitters can be further limited by parasitic coupling between the four transmitter paths [1], [31]. An advantage of digital transmitters with respect to their analog counterparts, is that their internal signals are digital logic signals, which make them robust to crosstalk. As long as the crosstalk is low enough to not result in bit-flips, the digital signals are unaffected. Coupling between the analog RF outputs can still be present and can result in reverse intermodulation distortion (RIMD) [32]. In [33] it is however shown that class D architectures, such as the SCPA driver cells, show little RIMD. MIMO distortion will lead to intermodulation, following a different array pattern than the one set in the precoder weights [34]. Beam pattern measurements in Section VII will show close resemblance to the theoretical beam patterns, indicating limited MIMO distortion.

The digital internal nodes and class D output make the SCPA a suitable candidate for DPD-less linear MIMO applications, as long as a low-impedance power supply can be realized.

VI. Circuit Implementation

A. Implementation in 22nm FD-SOI CMOS

A MIMO transmitter featuring four SCPAs is designed in Global Foundries 22FDX™ 22nm FD-SOI CMOS technology with a supply voltage of 0.9V. An overview of this design is given in Figure 12. Though this IQ-sharing quadrature SCPA implementation is less power efficient than its polar counterpart [16], it does not suffer from nonlinearity introduced by finite bandwidth of the control signals, or delay between the phase and amplitude control paths [35]. The 8-bit SCPAs have 5 unary and 3 binary coded bits. For linearity, the constant output conductance driver of Figure 10a is used, dimensioned for an output conductance of 2.4mS per cell, resulting in a transmitter output impedance of 1.6Ω for each pseudo-differential RF-DAC half. This pseudo-differential implementation also cancels even-order distortion, which could be caused by unequal rising and falling edges in single-ended output drivers. DTCs are used on all four 25% duty cycle clock phases in all four transmitters to compensate for quadrature imbalance. An external field-programmable gate array (FPGA) is used to generate digital baseband data, synchronized to the divided LO. A die photograph is shown in Figure 13. The total active area for all four SCPAs and auxiliary circuits for clock generation and communication with the FPGA is 0.33 mm^2.

B. Bondwire Chebyshev matching network

Digital transmitters typically use integrated inductors in their matching network [2], [5]–[7], [10], [13], [14], [19], [27], requiring significant chip area. In this implementation, a wideband Chebyshev bandpass matching network is used to bring the RF signals off-chip. This matching network allows for a trade-off between fractional bandwidth, passband ripple and impedance transformation ratio, where two of these three variables can be chosen freely. Bondwires inside a QFN package are used as inductors. Using bondwires instead of an on-chip inductor or transformer reduces loss in the matching network, due to the high quality factor with respect to integrated inductors [36]. It also decreases chip

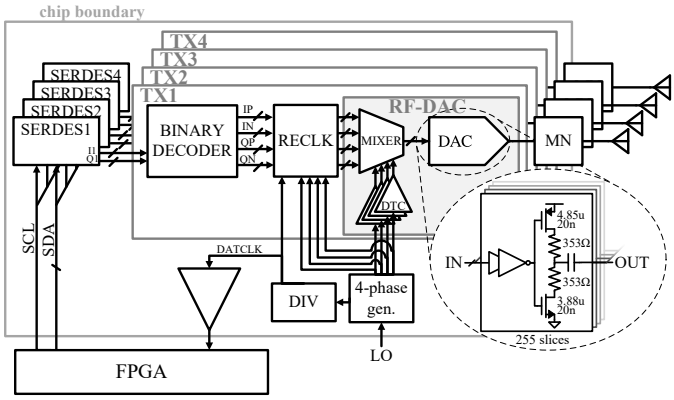


Fig. 12. Overview of the transmitter implementation. Single-ended equivalent is shown. The actual implementation is pseudo-differential.

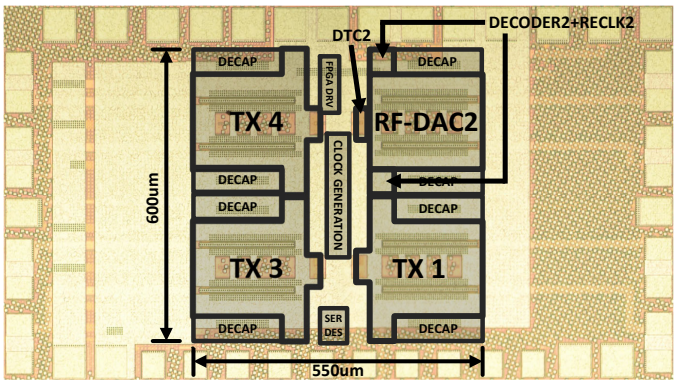


Fig. 13. Die photograph of the MIMO transmitter.

area, albeit at the cost of required external components in this application. A second order lowpass prototype Chebyshev matching network was designed and transformed to a fourth order bandpass filter using the transform in [37]. Next, the inductive tee transformation from [23], [38] was used to provide frequency-independent impedance transformation by swapping the position of the two inductors. The final matching network in Figure 14 is the differential version of this. The differential inputs allow to combine the power of two pseudo-differential SCPAs. An additional advantage of this matching network is that the return path for the RF output current is not via the ground wiring, which could cause ground bounce and further supply related nonlinear effects.

The simulated transfer of the lumped element Chebyshev filter is indicated in Figure 15, along with the transfer when inductance varies $\pm 20\%$, due to e.g. inaccuracy in bondwire modeling. As the impedance transformation in [38] is dependent on inductor ratios, the effect of increasing all inductor values by the same factor is small. The lower and upper cut-off frequency do change with inductor values, but as the Chebyshev filter has a wide fractional bandwidth, the effect around the center of the passband is limited, at < 1 dB deviation from the nominal scenario, over a 51% fractional bandwidth for this $\pm 20\%$ inductance variation. In the physical implementation,

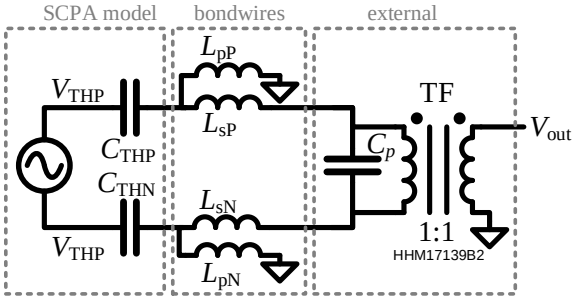


Fig. 14. Chebyshev bandpass matching network. SCPA modeled as its Thévenin equivalent circuit and bondwires as inductors.

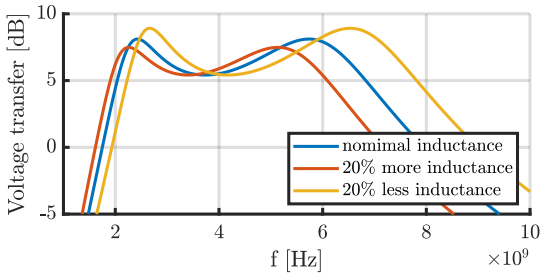


Fig. 15. Voltage transfer of the lumped element Chebyshev matching network in Figure 14, indicating transfer in case of inductance variation.

additional factors will influence the frequency transfer, such as the transfer of the used transformer, and PCB transfer. Initial estimations for physical bond wire configurations are made using the models for arrays of bondwires from [39] as the inductors in Keysight ADS. PCB layout and C_p value were optimized using 3D EM simulations in Cadence Clarity.

Figure 16 shows a photograph of a decapsulated chip on the measurement PCB. The matching network bondwires acting as the inductors are marked in blue, and the PCB layout of the matching network including the parallel capacitor C_p and the transformer is shown.

C. Low-impedance supply

An external Texas Instruments TPS7A7001DDAR low-dropout regulator and muRata LLL185R71A224MA01L low equivalent series resistance decoupling capacitors generate a low impedance supply for DC and low frequencies. For medium frequencies up to the the signal envelope bandwidth, external low equivalent series inductance capacitors are used, as indicated in pink in Figure 16. To minimize series inductance, these capacitors are connected via ground and supply planes, they are placed as close as possible to the chip, and multiple short bondwires are used. 620 pF on-chip decoupling keeps the supply impedance low for high frequencies, for the carrier frequency and higher. The combination of the external regulator, external decoupling with low series inductance and resistance connections, and on-chip decoupling keeps the supply impedance low enough to support up to 160 MHz DPD-less 1024QAM orthogonal frequency-division multiplexing (OFDM).

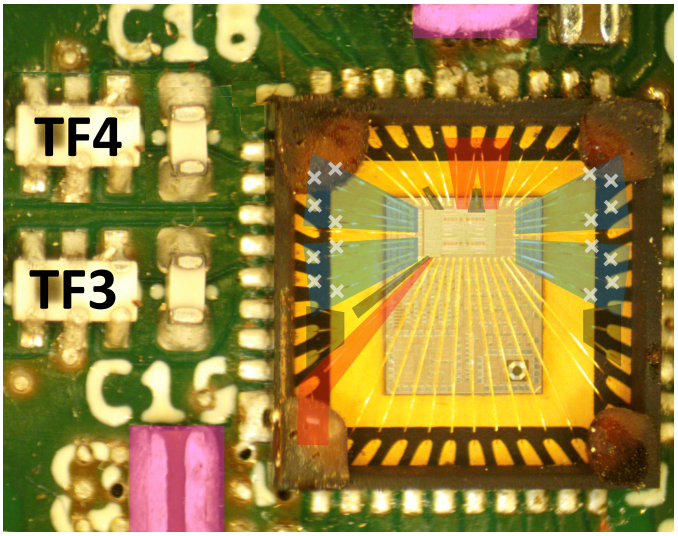


Fig. 16. Photograph of the decapsulated chip on PCB. Bondwires for matching network, supply and ground are indicated in blue, red and black, respectively. White crosses indicate matching network bonds. Low-inductance decoupling capacitors in pink, with two more on the opposite side of the PCB. TF4 and C18 had been removed from this defective PCB and were edited in. Other components are unedited, except for marking.

VII. Experimental Results

A. Quadrature imbalance calibration

For QAM signals, quadrature gain and phase imbalance result in a rectangular and sheared transmitted constellations, respectively, as well as a spectral image. These effects degrade EVM and the transmit spectrum, respectively. The spectral image can be quantified using IRR. A single-sideband test signal is transmitted 20 MHz above the carrier frequency. The output signal is analyzed using a DSA-Z 204a oscilloscope. Quadrature imbalance will result in an image tone 20 MHz below the carrier. This experiment is shown for 1.9 GHz and 3.0 GHz carrier frequencies in Figure 17a and 17b, indicating IRRs of 33 dB and 27 dB, respectively. The search algorithm indicated in Figure 18 was used to find the optimal C_ϕ and $C_{\hat{A}}$. Calibration results are indicated in Figure 17c and 17d. The IRRs after quadrature calibration in Figure 17e and 17f have improved to 59 dB and 55 dB at 1.9 GHz and 3.0 GHz respectively, both below LO leakage levels, which will be shown to suffice for 1024QAM. By tuning the clock phases as in Figure 4c, LO leakage could also be suppressed using the same hardware. This would however require additional calibration steps, and is not needed to meet the 1024QAM EVM requirements. The chip was calibrated only once per carrier frequency and RF-DAC. The C_ϕ and $C_{\hat{A}}$ settings found here were used in all following experiments.

B. RF passband, output power and efficiency

To measure the output power over carrier frequency, the baseband I and Q values are set to maximum, and the LO frequency is varied. The resulting output power for all four PAs can be seen in Figure 19a. Over the range from 1.64 GHz to 3.28 GHz, a maximum output power of 9.0 dBm ±1.7 dB

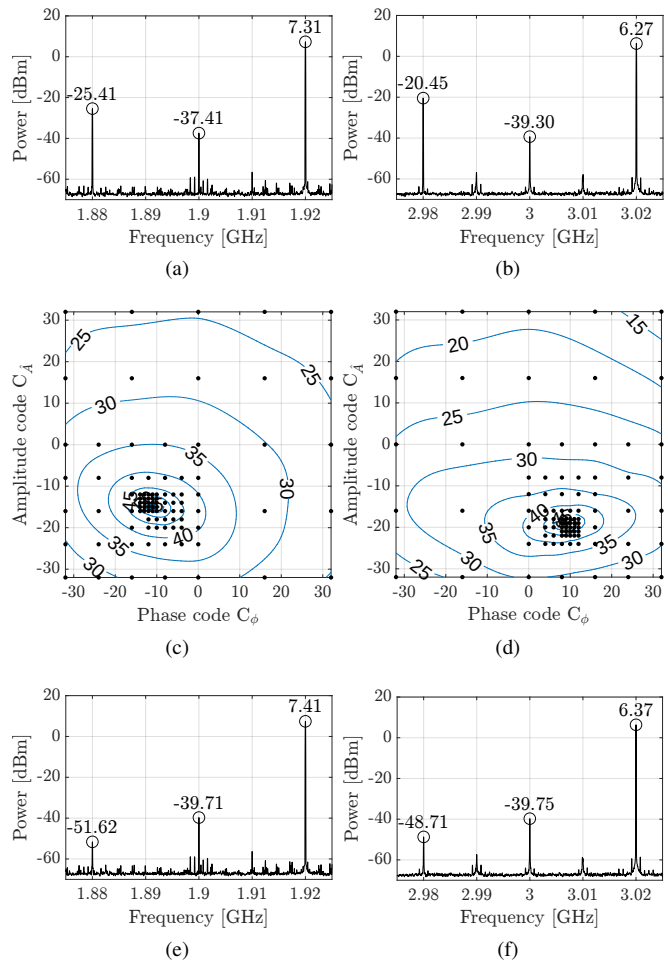


Fig. 17. Single-sideband test using a 20MHz signal. Uncalibrated IRR at 1.9 GHz (a) and 3.0 GHz (b), IRR versus calibration code at 1.9 GHz (c) and 3.0 GHz (d), indicating the measured points of the search algorithm, and IRR after calibration at 1.9 GHz (e) and 3.0 GHz (f).

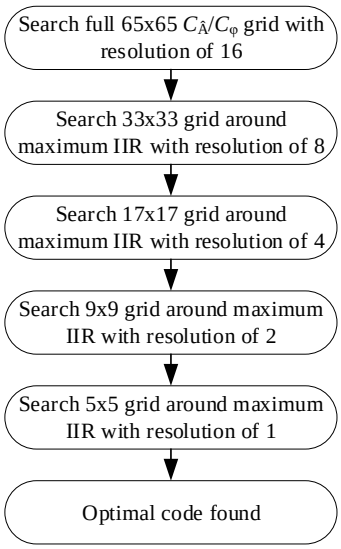
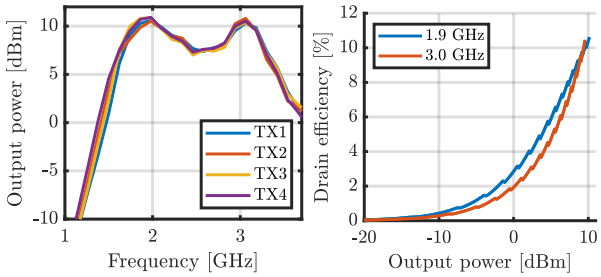


Fig. 18. Flowchart for the quadrature imbalance calibration search algorithm.



(a) (b)

Fig. 19. Maximum output power over frequency (a) and drain efficiency over output power (b).

was realized, demonstrating the performance of the matching network over a full octave. Within this frequency range, the worst-case amplitude mismatch between the four channels is 1.3 dB, at a carrier frequency of 1.74 GHz.

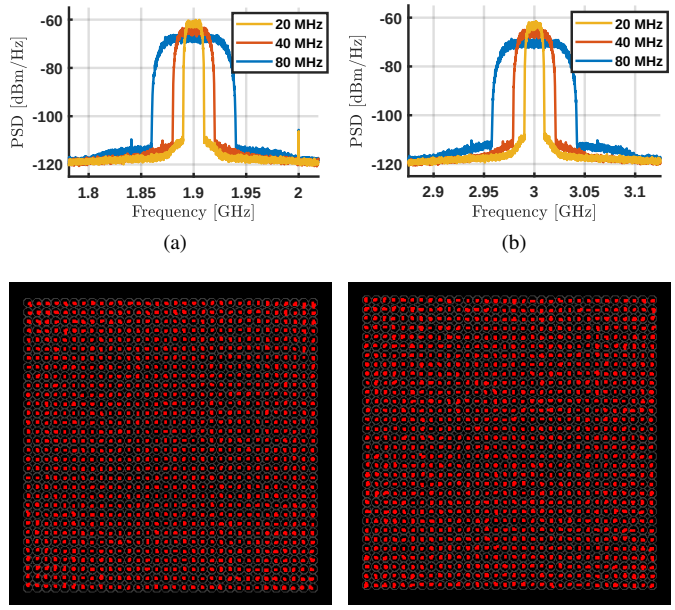
The drain efficiency (DE) of a single RF-DAC, as indicated in Figure 12, over output power has been measured for equal I and Q codes at 1.9 and 3.0 GHz carrier frequencies and is shown in Figure 19b, indicating a maximum DE of 10.6% and 10.5%, respectively.

C. 1024QAM measurements

Single carrier 1024QAM signals are transmitted with signal bandwidths f_{BW} from 20 to 80 MHz without DPD or digital compensation for quadrature imbalance. Tuning the back-bias voltages had no observable effect on ACLR, indicating that linearity is not limited by output conductance linearity, but by another factor, such as the supply impedance. For all following experiments, these back-gate voltages are grounded off-chip. The spectra for the 1024QAM signals are shown in Figure 20a for a 1.9 GHz carrier and Figure 20b for a 3.0 GHz carrier. The corresponding constellations for the 20 MHz 1024QAM signals are indicated in Figure 20c and 20d, respectively. For 160 MHz bandwidth measurements, 8×20 MHz 1024QAM OFDM is used. For a single-carrier signal, the frequency responses of the matching network and channel would need to be flat over the full 160 MHz signal bandwidth to avoid dispersion. In multi-carrier modulation such as OFDM, only the subcarrier bandwidth needs to have a flat response [40]. These OFDM measurements are indicated in Figure 21. This wide signal bandwidth does however result in significant sampling aliases around the 250 MHz sampling frequency offset. This could be improved by e.g. increasing the oversampling rate, using digital interpolation filters [11], [12], or mixed signal finite impulse response filters with upsampling to $4f_c$ [4]. An overview of EVM, ACLR, average output power P_{avg} and average RF-DAC DE η_{avg} for these modulated carriers are shown in Table I. All scenarios meet the −35 dB EVM requirement for 1024QAM demodulation [9].

D. Temperature stability

The measurements in Table I were conducted at a temperature of 35°C, measured on the top of the QFN package using a thermocouple. This is higher than room temperature as the



(a) (b)

(c) (d)

Fig. 20. Spectra for 1024QAM signals with a carrier frequency of 1.9 GHz (a) and 3.0 GHz (b), and their respective 20 MHz constellations indicating −43.3 dB EVM at 1.9 GHz (c), and −42.7 dB EVM at 3.0 GHz (d).

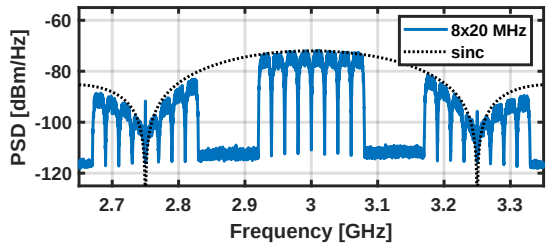


Fig. 21. Spectrum for 8 carrier 160 MHz 1024QAM OFDM, showing spectral aliases following the sinc function. Additional suppression comes from the matching network frequency response, shown in Figure 19a.

measurement PCB is placed on top of a power consuming FPGA board. To measure the temperature stability of both the quadrature error compensation and the constant output conductance linearization, the chip was heated to an arbitrary stable temperature using hot air, and the 20 MHz 1024QAM signal at 1.9 GHz was measured again. At a temperature of 88°C, measured on top of the package, and without DTC recalibration, the resulting EVM and ACLR were −42.6 and −47.5 dB, respectively. This is an EVM degradation of only

TABLE I
OVERVIEW OF 1024QAM MEASUREMENT RESULTS

f_c [GHz]	1.9				3.0			
f_{BW} [MHz]	20	40	80	8×20	20	40	80	8×20
EVM [dB]	-43.3	-41.4	-37.1	-36.3	-42.7	-42.8	-39.4	-35.4
lower/upper ACLR [dB]	-47.8 /-47.7	-46.5 /-46.2	-44.0 /-43.8	N/A[a]	-48.0 /-48.2	-45.9 /-46.1	-43.3 /-43.3	N/A[a]
P_{avg} [dBm]	3.83	3.87	3.75	0.91	2.89	2.85	2.83	–0.02
η_{avg} [%]	5.0	5.0	4.9	2.7	3.2	3.2	3.2	2.0

[a] ACLR cannot be measured due to aliasing in the adjacent channel.

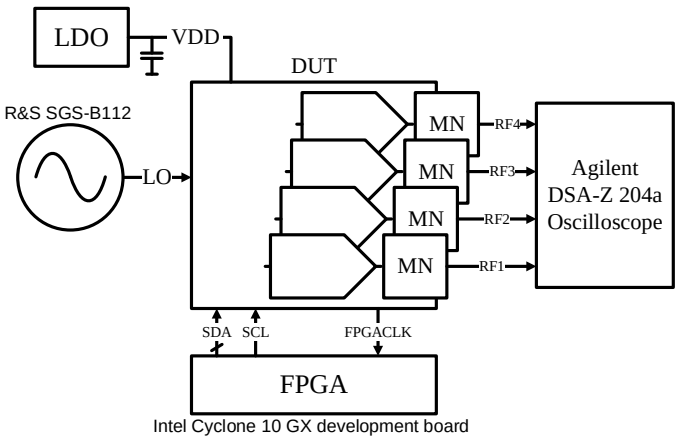


Fig. 22. Overview of the MIMO measurement setup.

0.7 dB due to a temperature increase of 53°C. The measured EVM still suffices the −35 dB 1024QAM specification [9]. When temperature variation would result in e.g. ±5% DTC delay variation, this gives a similar time error at the minimum delay of 38 ps (±1.9 ps delay variation) and at maximum delay of 48 ps (±2.4 ps delay variation), with only 26% difference between the best-case and worst-case scenario.

E. MIMO experiments

To evaluate MIMO SCPA performance in a well-controlled RF environment, wired experiments have been conducted for a 3.0 GHz carrier frequency, using the measurement setup in Figure 22. The four RF outputs are captured simultaneously, and the corresponding spatial patterns are generated in MATLAB, assuming isotropic antennas with $\lambda/2$ spacing. Matched SMA cables were used between the measurement PCB and the oscilloscope. The mutual coupling matrix $\mathbf{H}_\mathrm{M}$, including on-chip, packaging, PCB, and measurement setup coupling was characterized. A sine wave at the carrier frequency and maximum amplitude was transmitted in one of the four SCPAs, while the other SCPAs are set to zero amplitude. By measuring the gain and phase of RF1–RF4 at the oscilloscope inputs, the coupling coefficients from the transmitting SCPA to the four oscilloscope inputs can be found. This procedure is repeated for all four SCPAs to find all components of $\mathbf{H}_\mathrm{M}$. The precoder weights are compensated with $\mathbf{H}_\mathrm{M}^{-1}$ to account for this coupling.

A broadside beam is measured and is shown in Figure 23a and 23b. The beam pattern in Figure 23b indicates close correspondence with the ideal pattern. A beam directed towards 30° and a null towards −45° is indicated in Figure 23c. Its beam pattern in Figure 23d indicates a null depth of −32 dB. The beam and null directions are swapped in Figure 23f, indicating a null depth of −30 dB in Figure 23f. These 30° and −45° beams are transmitted simultaneously in Figure 23g and 23h using superposition of the two orthogonal beams with > 30 dB isolation. Due to residual crosstalk, the −35 dB EVM requirement for 1024QAM is not met entirely for this multibeam scenario. Smaller 256QAM constellations

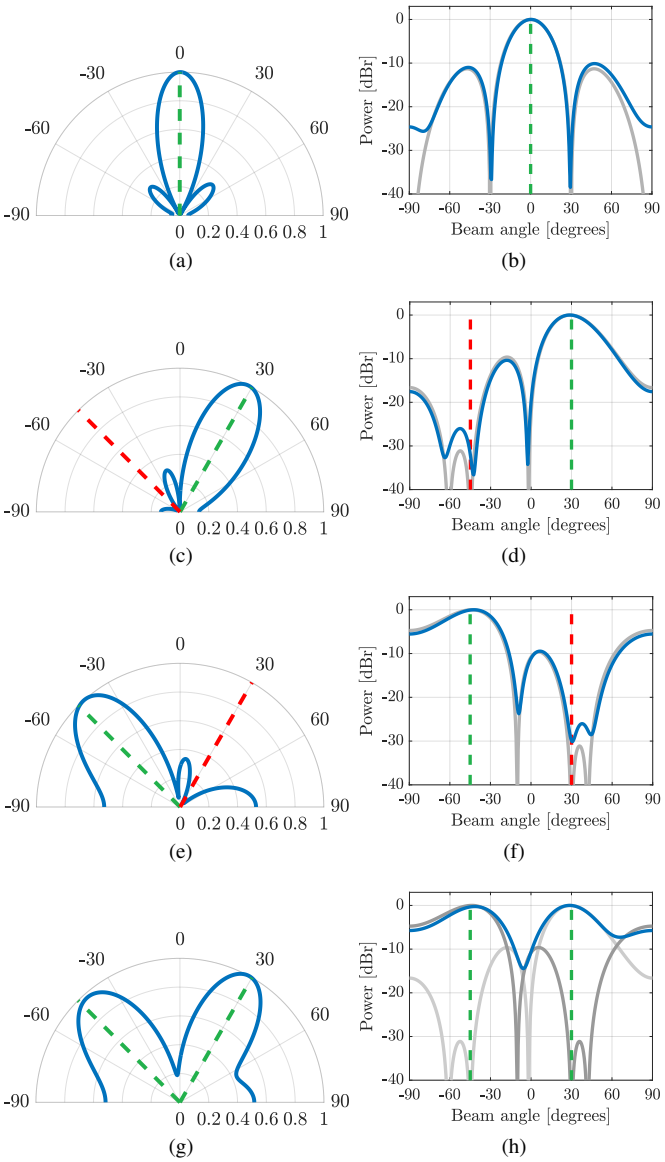


Fig. 23. Patterns for a 3 GHz broadside beam (a, b), 30° beam (c, d), −45° beam (e, f), and a dual-beam scenario (g, h). Measured beam patterns indicated in blue, beam directions in green, notches in red, theoretical patterns in gray.

or increased orthogonality are required. The latter can be achieved e.g. by more accurate characterization of $\mathbf{H}_\mathrm{M}$ to increase the null depths.

When moving to over-the-air experiments, antenna loss, antenna directivity and coupling between the antennas will be introduced. This coupling can be minimized by careful design for low coupling [41]. As long as the remaining coupling does not result in dominant non-linear behavior, this coupling can be considered to be part of the channel matrix $\mathbf{H}_\mathrm{M}$ and can be compensated for in the precoder weights.

A comparison to state-of-the-art digital (MIMO) transmitters is given in Table II. This indicates excellent DPD-less EVM, allowing for single-beam 1024QAM. Combined with the wide RF bandwidth, this results in a high data rate of 1.18

TABLE II
PERFORMANCE OVERVIEW AND COMPARISON TO STATE-OF-THE-ART

Reference	**This work**	[10]	[12]	[13]	[7]	[27]
Architecture	**Quadrature SCPA**	Multiphase SCPA	Bandpass-$\Delta\Sigma$	Current DAC	Quadrature SCPA	Current DAC
Frequency [GHz]	**3.0**	1.75	6.0	5.2	2.2	4.5
No. elements	**4**	4	8	4	1	1
Element P_{avg} [dBm]	**2.9**	18.4	2	14.5	–3[d]	18.2
Element η_{avg} [%]	**3.2**	14.0	3.3	N/A	1.0[d]	41
Modulation	**1024QAM**	64QAM OFDM	16QAM	64QAM	802.11ax 1024QAM	512QAM OFDM
Bandwidth [MHz]	**80**	15	24	40[b]	40[b]	320[b]
ACLR [dB]	**–43.3/–43.3**	–30.5/–30.9	N/A	–30.7/–30.4	–47/–47[c]	–39.7/–39.9
Element EVM [dB]	**–39.4**	–28.6	–29.6	–24.7	–42.2	–29.65
DPD	**No**	No	No	Yes	No	Yes
Technology	**22nm FD-SOI CMOS**	65nm CMOS	28nm CMOS	40nm CMOS	65nm CMOS	40nm CMOS
Supply voltage [V]	**0.9**	1.4/2.8	1.0	1.1/1.2	1.2	1.0
Matching network	**bondwires + external**	on-chip	on-chip	on-chip	on-chip	on-chip
Chip core area [mm^2]	**0.33**	5	0.08	3.12	0.14	1.5

[b] Values for maximum modulation bandwidth listed. [c] Estimated from figure. [d] Increased back-off to trade efficiency for linearity.

Gbps[4]. The 3.2% element efficiency is high for a DPD-less 1024QAM transmitter. The bondwires as inductors reduce the chip area per transmitter element.

VIII. Conclusion

In MIMO systems with low element transmit power and wide signal bandwidth, the DPD power can exceed the PA power. In this case, a high system efficiency can be achieved by using a PA with sufficient linearity, image rejection and ISI performance to meet the required EVM specifications without DPD, even if this comes at the cost of decreased PA DE. SCPAs were shown to be suitable candidates with both high linearity and a reduced number of memory effects. A digital high linearity MIMO transmitter with output conductance linearization was previously proposed in [8], meeting the linearity requirements for 1024QAM. This work adds quadrature imbalance calibration, RF bandwidths up to 160 MHz, a wideband low impedance power supply and MIMO capabilities. This implements a high EVM digital MIMO transmitter which does not require any DPD or digital quadrature compensation.

A four-element MIMO transmitter in 22nm FD-SOI CMOS was demonstrated. A wide passband Chebyshev bandpass filter using bondwires in a QFN package as inductors functions as the matching network, providing a n RF passband of 1.64 GHz to 3.28 GHz. The lack of on-chip inductors decreases chip area, albeit at the cost of required external components. A time-skewed reclocking strategy was proposed to relax the timing requirements for the RF-DAC baseband signals, exploiting the 75% of the carrier period where the digital mixer does not select the respective baseband input.

Quadrature calibration was implemented by adding programmable delay to all clock edges using DTCs. The calibration procedure is simplified to two degrees of freedom by defining and tuning a phase imbalance code and gain imbalance code for optimal IRR. In measurements, this technique improves IRR to >53 dB, allowing for 1024QAM signals without quadrature compensation. Temperature stability of this calibration has been demonstrated by increasing the chip temperature by $53°$C, which had an insignificant effect of < 0.7 dB on EVM.

MIMO specific nonlinear effects are discussed, indicating the highly digital nature makes the SCPA robust to crosstalk between the MIMO signal chains, but nonlinear crosstalk can occur via the power supply. Bonding and PCB design and decoupling were optimized for a wideband low-impedance supply network to mitigate this effect.

The combination of linear constant-conductance drivers, quadrature imbalance calibration and a wideband low-impedance power supply allows for DPD-less 1024QAM OFDM up to 160 MHz signal bandwidth. For 20 MHz 1024QAM signal and a 1.9 GHz carrier, the EVM and ACLR are -43.3 dB and -47.7 dB, respectively, at an average output power of 3.8 dBm and DE of 5.0%. For a 3.0 GHz carrier, the EVM and ACLR are -42.7 dB and -48.1 dB, respectively, at an average output power of 2.9 dBm and DE of 3.2%.

Four-element MIMO experiments demonstrate single and multi-beam scenarios with ≤ -30 dB crosstalk between the beams, resulting in sufficient EVM for single-beam 1024QAM communication.

IX. Acknowledgment

We would like to thank GlobalFoundries for silicon donation. We would also like to thank Gerard Wienk, who has sadly passed away too soon, for his CAD support, and Olaf Zanen for language related reviewing.

References

[1] J. Zanen, E. Klumperink, and B. Nauta, "Power efficiency model for MIMO transmitters including memory polynomial digital predistortion," *IEEE Trans. Circuits Syst. II*, vol. 68, no. 4, pp. 1183–1187, 2021.

[2] M. Hashemi, Y. Shen, M. Mehrpoo, M. S. Alavi, and L. C. N. de Vreede, "An intrinsically linear wideband polar digital power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3312–3328, 2017.

[3] M. Hashemi, L. Zhou, Y. Shen, and L. C. N. de Vreede, "A highly linear wideband polar class-E CMOS digital doherty power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 10, pp. 4232–4245, 2019.

[4] R.-C. Marin, A. Frappé, B. Stefanelli, P. Cathelin, A. Cathelin, and A. Kaiser, "Digital RF transmitter with single-bit $\Delta\Sigma$M-driven switched-capacitor RF DAC and embedded band filter in 28-nm FD-SOI," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 3200–3209, 2019.

[4]With the used transmit filter roll-off factor of 0.35 for the 8×20 Mhz experiments, the symbol rate is 118 MSps at 10 bits per symbol for 1024QAM.

[5] N. Ginzberg, D. Regev, R. Keren, and E. Cohen, "A 65 nm CMOS quadrature balanced switched-capacitor power amplifier for full- and half-duplex wireless operation," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 3008–3020, 2021.

[6] S.-W. Yoo, S.-C. Hung, and S.-M. Yoo, "A multimode multi-efficiency-peak digital power amplifier," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3322–3334, 2020.

[7] S.-W. Yoo, S.-C. Hung, J. S. Walling, D. J. Allstot, and S.-M. Yoo, "A 0.26mm2 DPD-less quadrature digital transmitter with <–40dB EVM over >30dB Pout range in 65nm CMOS," in *2020 IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2020, pp. 184–186.

[8] J. Zanen, E. Klumperink, and B. Nauta, "A predistortion-less digital transmitter with –50-dB ACLR exploiting output conductance linearization," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 162–165, 2021.

[9] "IEEE standard for information technology–telecommunications and information exchange between systems local and metropolitan area networks–specific requirements part 11: Wireless LAN medium access control (MAC) and physical layer (PHY) specifications amendment 1: Enhancements for high-efficiency WLAN," *IEEE Std 802.11ax-2021*, p. 636.

[10] Z. Bai, W. Yuan, A. Azam, and J. S. Walling, "A multiphase interpolating digital power amplifier for TX beamforming in 65nm CMOS," in *2019 IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2019, pp. 78–80.

[11] B. Zheng, L. Jie, J. Bell, Y. He, and M. P. Flynn, "A two-beam eight-element direct digital beamforming RF modulator in 40-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2569–2579, 2019.

[12] B. Zheng, L. Jie, and M. P. Flynn, "A 6-GHz MU-MIMO eight-element direct digital beamforming TX utilizing FIR H-bridge DAC," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 6, pp. 2832–2840, 2021.

[13] H. J. Qian, J. Zhou, B. Yang, and X. Luo, "A 4-element digital modulated polar phased-array transmitter with phase modulation phase-shifting," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 11, pp. 3331–3347, 2021.

[14] S.-M. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, 2011.

[15] H. Jin, D. Kim, and B. Kim, "Efficient digital quadrature transmitter based on IQ cell sharing," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1345–1357, 2017.

[16] J. Zanen, E. Klumperink, and B. Nauta, "Analysis of switched capacitor losses in polar and quadrature switched capacitor PAs," *IEEE Trans. Circuits Syst. II*, vol. 67, no. 10, pp. 1904–1908, 2020.

[17] W. Luo, Y. Yin, L. Xiong, T. Li, and H. Xu, "Nonlinear analytical model for switched-capacitor class-D RF power amplifiers," *IEEE Trans. Circuits Syst. I*, vol. 66, no. 6, pp. 2309–2321, 2019.

[18] S. Trampitsch, M. Kalcher, H. Enzinger, D. Gruber, M. Lunglmayr, and M. Huemer, "A circuit-inspired digital predistortion of supply network effects for capacitive RF-DACs," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 1, pp. 271–283, 2021.

[19] M. Fulde *et al.*, "A digital multimode polar transmitter supporting 40MHz LTE carrier aggregation in 28nm CMOS," in *2017 IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2017, pp. 218–219.

[20] T. C. W. Schenk and E. R. Fledderus, "RF impairments in high-rate wireless systems - understanding the impact of TX/RX-asymmetry," in *2008 3rd International Symposium on Communications, Control and Signal Processing*, 2008, pp. 117–122.

[21] F. Gregorio, J. Cousseau, S. Werner, T. Riihonen, and R. Wichman, "EVM analysis for broadband OFDM direct-conversion transmitters," *IEEE Transactions on Vehicular Technology*, vol. 62, no. 7, pp. 3443–3451, 2013.

[22] A. Cheaito, M. Crussière, J.-F. Hélard, and Y. Louët, "Quantifying the memory effects of power amplifiers: EVM closed-form derivations of multicarrier signals," *IEEE Wireless Communications Letters*, vol. 6, no. 1, pp. 34–37, 2017.

[23] S. C. Cripps, *Advanced Techniques in RF Power Amplifier Design*. Artech House, 2002.

[24] S. Kawai *et al.*, "An 802.11ax 4×4 spectrum-efficient WLAN AP transceiver SoC supporting 1024QAM with frequency-dependent IQ calibration and integrated interference analyzer," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 442–444.

[25] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Artech House, 2006, p. 256.

[26] M. He *et al.*, "20.5 a 40nm dual-band 3-stream 802.11a/b/g/n/ac MIMO WLAN SoC with 1.1Gb/s over-the-air throughput," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 350–351.

[27] M. Beikmirza, Y. Shen, L. C. N. de Vreede, and M. S. Alavi, "A wideband four-way Doherty bits-in RF-out CMOS transmitter," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3768–3783, 2021.

[28] X. Gao, E. A. M. Klumperink, and B. Nauta, "Advantages of shift registers over DLLs for flexible low jitter multiphase clock generation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 3, pp. 244–248, 2008.

[29] M. Mehrpoo, M. Hashemi, Y. Shen, L. C. N. de Vreede, and M. S. Alavi, "A wideband linear ¡inline-formula¿ ¡tex-math notation="latex"¿i/q ¡/tex-math¿¡/inline-formula¿-interleaving ddrm," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1361–1373, 2018.

[30] E. Mensink, *High Speed Global On-Chip Interconnects and Transceivers*. Ph.D. dissertation, University of Twente, Netherlands, Jun. 2007, p. 22.

[31] S. A. Bassam, M. Helaoui, and F. M. Ghannouchi, "Crossover digital predistorter for the compensation of crosstalk and nonlinearity in MIMO transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 5, pp. 1119–1128, 2009.

[32] A. N. Atanasov, M. S. Oude Alink, and F. E. van Vliet, "Reverse intermodulation in multi-tone array transmitters," in *2020 IEEE BiCMOS and Compound Semicond. Integr. Circuits and Technol. Symposium (BCICTS)*, 2020.

[33] M. Kamper, G. Ulbricht, R. Weigel, and G. Fischer, "Comparison of class A and class D RF amplifier operation with focus on reverse intermodulation and efficiency performance," in *2011 6th European Microw. Integrated Circuit Conf.*, 2011, pp. 272–275.

[34] M. C. M. Soer, E. A. M. Klumperink, D.-J. van den Broek, B. Nauta, and F. E. van Vliet, "Beamformer with constant-gm vector modulators and its spatial intermodulation distortion," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 735–746, 2017.

[35] F. H. Raab, "Intermodulation distortion in kahn-technique transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 44, no. 12, pp. 2273–2278, 1996.

[36] F. Svelto and R. Castello, "A bond-wire inductor-MOS varactor VCO tunable from 1.8 to 2.4 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 403–407, 2002.

[37] D. M. Pozar, *Microwave Engineering*, 4th ed. Wiley, 1998, p. 405.

[38] S. C. Cripps, "Chasing Chebyshev [microwave bytes]," *IEEE Microw. Mag.*, vol. 8, no. 6, pp. 34–44, 2007.

[39] A. L. Nazarian, L. F. Tiemeijer, D. L. John, J. A. van Steenwijk, M. de Langen, and R. M. T. Pijper, "A physics-based causal bond-wire model for RF applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 3683–3692, 2012.

[40] A. F. Molisch, *Wireless Communications*, 2nd ed. Wiley, 2011, p. 417.

[41] C. A. Balanis, *Antenna Theory: Analysis and Design*. John Wiley & Sons, Inc., 2005, ch. 8.7, pp. 478–491.

Joep Zanen (Student Member, IEEE) received the B.Sc. and M.Sc. (*cum laude*) degrees in electrical engineering from the University of Twente, Enschede, the Netherlands, in 2015 and 2017, respectively, where he is currently pursuing the Ph.D. degree in predistortion-less transmitter design with the Integrated Circuit Design Group.

In 2022 he joined ItoM Enschede, the Netherlands, where he is working as an analog and mixed signal IC designer. His current research interests are in the area of high-speed mixed-signal IC design.

Eric Klumperink (IEEE Member '98, Senior Member '06, Fellow '20) was born on April 4th, 1960, in Lichtenvoorde, The Netherlands. He received a B.Sc. degree from HTS, Enschede (1982), worked in industry on digital hardware and software, and then joined the University of Twente, Enschede, in 1984, shifting focus to analog CMOS circuit research. This resulted in several publications and his Ph.D. thesis "Transconductance Based CMOS Circuits: Circuit Generation, Classification and Analysis" (1997). In 1998, Eric started as Assistant Professor at the IC-Design Laboratory in Twente and shifted research focus to RF CMOS circuits during a sabbatical in 2001 at Ruhr Universitaet Bochum, Germany. Since 2006, he is an Associate Professor, teaching Analog & RF IC Electronics and guiding PhD and MSc projects related to RF CMOS circuit design with focus on Software Defined Radio, Cognitive Radio and Beamforming. Eric served as an Associate Editor for the IEEE TCAS-II (2006–2007), IEEE TCAS-I (2008–2009) and the IEEE JSSC (2010–2014), and as member of the technical program committees of conferences ISSCC (2011–2016), RFIC Symposium (2011–2021) and ESSCIRC (2019–). He holds 16 patents, authored and co-authored over 200 internationally refereed journal and conference papers, and was recognized as 20+ ISSCC paper contributor over 1954–2013. He is a co-recipient of the ISSCC 2002 and the ISSCC 2009 "Van Vessem Outstanding Paper Award" and served as IEEE SSC Distinguished Lecturer.

Bram Nauta (Fellow, IEEE) was born in Hengelo, The Netherlands, in 1964. He received the M.Sc. degree (cum laude) in electrical engineering and the Ph.D. degree in analog CMOS filters for very high frequencies from the University of Twente, Enschede, The Netherlands, in 1987 and 1991, respectively.

In 1991, he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, The Netherlands. In 1998, he returned to the University of Twente, where he is currently a Distinguished Professor, heading the Integrated Circuit Design Group. Since 2016, he has been the Chair of the Electrical Engineering Department, University of Twente. His current research interests are high-speed analog CMOS circuits, software-defined radio, cognitive radio, and beamforming.

Dr. Nauta is also a member of the Royal Netherlands Academy of Arts and Sciences (KNAW). He was a co-recipient of the International Solid State Circuits Conference (ISSCC) 2002 and 2009 Van Vessem Outstanding Paper Award. In 2014, he received the Simon Stevin Meester Award (500.000e), the largest Dutch national prize for achievements in technical sciences. He was the 2013 Program Chair of the ISSCC. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 1997 to 1999 and the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) from 2001 to 2006. He has served as the Editor-in-Chief of the IEEE JSSC from 2007 to 2010. He served as the President of the IEEE Solid-State Circuits Society from 2018 to 2019. He was on the Technical Program Committee of the Symposium on VLSI Circuits from 2009 to 2013. He is on the Steering Committee and the Program Committee of the European Solid State Circuit Conference (ESSCIRC). He has served as a Distinguished Lecturer of the IEEE.