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Sidewall patterning—a new wafer-scale method for accurate patterning of vertical silicon structures

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Abstract

For the definition of wafer scale micro- and nanostructures, in-plane geometry is usually controlled by optical lithography. However, options for precisely patterning structures in the out-of-plane direction are much more limited. In this paper we present a versatile self-aligned technique that allows for reproducible sub-micrometer resolution local modification along vertical silicon sidewalls. Instead of optical lithography, this method makes smart use of inclined ion beam etching to selectively etch the top parts of structures, and controlled retraction of a conformal layer to define a hard mask in the vertical direction. The top, bottom or middle part of a structure could be selectively exposed, and it was shown that these exposed regions can, for example, be selectively covered with a catalyst, doped, or structured further.

Keywords: microfabrication, nanofabrication, nanotechnology, corner lithography, retraction edge lithography, wafer scale

Supplementary material for this article is available [online](#)

(Some figures may appear in colour only in the online journal)

1. Introduction

Micro and nanofabrication are mostly achieved on flat (single-crystal silicon) substrates using techniques that modify the substrate as a whole. In the out-of-plane dimension (z), most of the structural and material contrast is obtained by various combinations of stacking and removal of films. Control of the in-plane dimensions (x and y) is typically obtained through lithography. By a combination of these two basic tools, complex 3D structures can be obtained, as can be seen for example in the complex 3D metal networks in integrated circuits. However, these are never truly 3D because the height of the structures that can be obtained is limited to a few micrometers because of the film growth rates of nanotechnology-compatible deposition methods. This is partly resolved by bulk

micromachining (etching into the substrate), but here the shape control in the z -direction is limited by the etching mechanism (isotropic, directional, or determined by crystallographic directions). The goal of this paper is to demonstrate routes for accurate out-of-plane ‘lithography’, to obtain the 3D structures as those shown in figure 1.

The ultimate technologies for obtaining similar control over all three dimensions of structures probably come from the field of 3D printing/writing, in which material is deposited or modified only at the exact position where it is desired. Some of these techniques reach the micrometer or even nanometer scale [1–7], especially two-photon polymerization laser writing. Many complex structures can be realized with this technique, as long as every voxel is attached to another voxel or the substrate. The main disadvantage of this

Figure 1. Schematic representation of structures that can be obtained by applying the techniques described in this paper: silicon (gray) micro or nanostructures covered by a conformal material (yellow), where selectively the top part (a), bottom part (b) or a band halfway (c) is opened to expose the underlying silicon. Note that this picture is not to scale—in principle the size and aspect ratio of the structures can be varied, and also the height(s) of the transition between the covered and exposed parts can be changed in a well-controlled way.

technology is the throughput. The technology is inherently slow, since the structures are created in a serial manner, while the more conventional thin-film and lithography-based micro and nanofabrication technologies can produce many structures in parallel on a single wafer or even on multiple wafers simultaneously.

Some interesting wafer scale alternatives can be found in more advanced lithography that uses photoresist as a 3D material instead of only as a 2D film. Grayscale lithography can achieve local gradients in photoresist thickness that can be amplified in the material underneath with a factor F , if a directional etching process is used that has etch rates ϵ_{resist} and $\epsilon_{\text{material}} = F\epsilon_{\text{resist}}$ [7, 8]. Nano imprint lithography (NIL) can also make use of a 3D stamp to create height differences in the resist (multilevel NIL) [7, 9], and the same amplification trick can be used. Laser interference lithography can be used in three dimensions [10], but is limited to periodic structures.

Similar structuring as can be achieved by grayscale lithography can also be achieved by directly controlling the sidewall angle during deep reactive ion etching (by changing the etch parameters as a function of etch time), and this also allows the creation of either positively or negatively tapered sidewalls, or combinations thereof in a single structure [11–16].

A completely different approach is to create structures bottom-up instead of top-down. Vapor-liquid-solid growth and templated electrodeposition can be used to grow wires, and the reactant gases/electrolytes can be changed during the process to obtain changes in material composition along the wires [17–25]. Further processing of such wires after the growth then also allows for changes in the radial direction [26]. Self-assembly is another bottom-up strategy to achieve 3D structures at this small scale [27]. Also, bottom-up grown carbon nanotubes can be further processed to connect [28] or locally modify [29] these nanotubes to create 3D structures.

Some specific 3D structures can sometimes be obtained by applying conventional wafer-scale nanofabrication techniques in unconventional combinations [7, 30–48]. Many of these use the edge or corner of some feature as a starting point for defining

new features ('Edge Lithography' [33] or 'Corner Lithography' [36]) and/or the specific orientation of certain surfaces which results in a contrast in deposition or etching speed.

For patterning regular arrays of wires or pores with micrometer or nanometer dimensions in the vertical direction, a rather straightforward technique exists. The spaces between the wires, or the holes themselves, are filled with polymer (or with a conformally grown layer of some other material) which is subsequently etched back to a certain height to facilitate the different treatment of the top and bottom of these wires or pores [49–58]. However such methods are prone to air trapping and non-uniformity, and usually require adjustment of the polymer deposition procedure for every individual geometry (diameter, pitch, height, etc). With the use of a completely filling conformal layer with good deposition uniformity, the air trapping and non-uniformity can be avoided, but for larger wire spacings or hole diameters prohibitive layer thicknesses are required for complete filling.

Here we report on wafer scale techniques that achieve accurate out of plane patterning, to obtain structures such as those shown in figure 1. This enables high throughput fabrication of complex micro and nanostructures with potential applications in many fields. In order to develop a versatile, accurate and reproducible patterning method for the sidewalls of out of plane silicon structures, (Retraction) Edge Lithography and standard wafer-scale technologies such as chemical vapor deposition, thermal oxidation and selective wet etching (which are intrinsically 3D because of their isotropic/conformal nature) are combined with a newly developed surface orientation dependent etching technique. This technique resembles the sidewall spacer technology used in the integrated circuit industry, except that because an inclined ion beam is used for etching, lower lying horizontal structures can also be retained. The presented techniques give good control over the resulting structures, have good uniformity, are scalable and are quite insensitive to the shape and sidewall roughness of the starting structures of the silicon on which the patterning is applied.

In this paper, in separate sections for each of the structures of figure 1, the fabrication processes and results are discussed, and an example of an application is presented. For all these processes it is crucial that the top surface of microstructures can be opened selectively, and therefore the novel technique that was developed to achieve this is discussed separately in section 3.

2. Modify the top part of a structure

This section describes the technique by which the top part of a silicon micro or nanostructure can be exposed selectively, while keeping the bottom part covered in silicon oxide, as shown in figure 1(a).

2.1. Fabrication

The fabrication procedure is shown schematically in figure 2 and is summarized in the caption of that figure (see SI section 1 for more details (stacks.iop.org/JMM/28/015008/mmedia)). This section elaborates on the materials and

Figure 2. Schematic process outline for opening only the top part of silicon structures (■ silicon substrate, ■ silicon oxide, ■ silicon nitride, ■ polysilicon). (a) Silicon wafer, (b) deep reactive ion etching of patterned wafer to create vertical sidewalls, (c) conformal coverage of all structures with subsequently silicon oxide, silicon nitride, polysilicon and silicon oxide, (d) removal of silicon oxide from the top by inclined ion beam etching (see section 3), (e) isotropic etching of polysilicon to the desired height, (f) isotropic etching of silicon oxide, (g) isotropic etching of silicon nitride, (h) isotropic etching of polysilicon, (i) isotropic etching of silicon oxide and (j) isotropic etching of silicon nitride. See text for a more detailed description.

methods that were chosen for the process. For a detailed discussion of the technique used in step d as shown in figure 2, see section 3.

The combination of silicon oxide, silicon nitride and (poly) silicon was chosen because these materials can be applied conformally by means of low pressure chemical vapor deposition, and because for each material a wet etching solution is available which etches the other two materials much slower, such that each material can be selectively etched without damaging the other materials too much.

The thermally grown silicon oxide layer was chosen as the outer layer because of the high quality of the layer (no pinholes) and its well-known angle dependent etching rate in the ion beam etching system used (see section 3).

In this material system, the etching solution for polysilicon, tetramethylammonium hydroxide (TMAH), has the highest etching rate and the highest selectivity (see SI table 1), and the etch rate is fairly constant even when etching deep down in narrow spaces. Therefore, the etching of polysilicon was chosen for the ‘retraction’ step (step e as shown in figure 2): the achieved height can be predicted by linear extrapolation and the layers that encapsulate this retracting layer remain intact during the retraction. Furthermore, making use of the controlled retraction of a sacrificial layer for defining a mask

edge minimizes the sensitivity of this technique to variations in sidewall angle as are encountered for example on structures with inclined or rough sidewalls.

The two layers below the polysilicon layer are needed to transfer the pattern formed in the polysilicon step by step to the underlying silicon structure. If they were not present, it would not be possible to remove this polysilicon hard mask without damaging the underlying silicon structure.

In principle, the procedure could be very much simplified if only two layers were used: first silicon oxide and then silicon nitride. The silicon nitride could be removed selectively from the top using inclined ion beam etching. Then the silicon oxide could be retracted to the desired height, and as a final step the silicon nitride could be etched selectively. However, the HF-solution that would be used for retracting the silicon oxide has only a limited selectivity especially towards silicon nitride, and the silicon nitride might fail after some retraction time. Also, the etch rate for the silicon oxide in HF-solution is typically not constant when etching in narrow trenches [59].

In principle, the particular materials and methods chosen here are not essential to the approach described in this paper, but the properties described in this section are. Without these, the procedure would not work, or at least not as well and reliably as described here.

Figure 3. SEM images of various silicon structures of which the bottom part is covered with silicon oxide (lighter gray): (a) narrow micropillars, (b) close up of a sidewall at the transition, (c) bar structure surrounded by open space, with cross section indicated in black, where only a band of silicon oxide (lighter) has remained in the middle of the sidewall (d) microholes and (e) wide micropillars. Scale bars: (a) 5, (b) 0.5, (c) 25, (d) 5 and (e) 25 μm .

2.2. Results and discussion

Figures 3(a) and (e) show that the process can be applied to silicon micropillars of various thicknesses and spacings, and that the edge of the silicon oxide can be controlled to be at various heights. Figure 3(d) shows that it can also be applied to microholes. Figure 3(b) shows that the transition is well-defined, even on rough sidewalls. Only for structures with very large open areas around the vertical structures was the lower part of the structures also uncovered (figure 3(c)). This effect is explained in section 3.

The distance of the transition location from the top of the structures was measured from the SEM pictures, and was related to the TMAH etching time (step e as shown in figure 2). Assuming a linear relation, the etch speed for this step was found to be $510 \pm 50 \text{ nm min}^{-1}$ (1σ), based on several structures from wafers etched for various times. On average, there was no significant offset in the linear fit, but for short and long etch durations standard deviations of respectively 1.5 and 1.6 μm between the heights on various structures on the same wafer were found. Since the standard deviation hardly increases with etch time, the spread in values is probably caused by a geometry related startup effect rather than by a variability in the TMAH etching speed.

This process has been applied to achieve spatioselective passivation on a microstructured silicon photocathode for the photoelectrochemical reduction of water to hydrogen [58]. The well-controlled patterning of the passivating oxide layer facilitated the localized electrodeposition of the nickel-molybdenum alloy catalyst, thereby preventing excessive light absorption without compromising the catalytic performance of these

Figure 4. SEM image of silicon micropillars of which only the bottom part and the horizontal surfaces between the pillars was covered in silicon oxide, and subsequently the top was covered with catalyst material by electrodeposition. The scale bar is 5 μm .

devices. An array of such micropillars that have catalyst material deposited on them only at their tops is shown in figure 4.

3. Selective opening of top surfaces

An important step for the processes described in this paper is the selective etching of the top surfaces of structures. In short, this is done by inclined ion beam etching of a rotating sample. In this section, the principles and test results from this technique are described in more detail.

The selective etching of silicon oxide on the top surfaces is based on two principles. Firstly, the silicon structures cast

Figure 5. Plot of the relative etch rates for ion milling of silicon oxide as a function of angle of incidence for a horizontal surface ('top'), a vertical surface ('side') and the ratio of these two ('top:side'). The measurements to which the 'top' curve was fitted are also shown, normalized with the $R(0)$ found from the fitting.

shadows on everything between them: the ion beam does not reach all surfaces between the structures during the full rotation of the substrate. Secondly, the etch (or sputter) rate of silicon oxide depends on the angle of incidence of the ion beam. This dependence can be described by [60]:

$$R(\theta) = \begin{cases} R(0) \cos |\theta| e^{a \sin^2 |\theta|} & |\theta| < 90^\circ \\ 0 & |\theta| \geq 90^\circ \end{cases} \quad (1)$$

where R is the sputter speed, θ the angle of incidence of the ion beam (with respect to normal incidence, the angle with respect to the horizontal plane is $\gamma = 90^\circ - \theta$), $R(0)$ the sputter rate at normal incidence and a a material dependent parameter. Etch rates for horizontal surfaces of thermally grown silicon oxide were measured for the used ion beam etching system (see SI section 1) as a function of angle (circles in figure 5), and equation (1) was found to fit the measured etch speeds best for $R(0) = 7.41 \text{ nm min}^{-1}$ and $a = 1.56$ (solid line in figure 5).

Next, the etching speeds for horizontal and vertical surfaces are calculated as a function of the ion beam incident angle θ and the rotation of the substrate ϕ . The symbols used are visualized in figure 6. The incident angle on horizontal surfaces will always be equal to θ , and is independent of ϕ . Therefore, the etch speed of horizontal surfaces that are never in the shadow of a structure is described by equation (1) and represented by the solid curve in figure 5. The incident angle on vertical surfaces, α , is defined with respect to the plane of the vertical surface, and depends on both θ and ϕ , as:

$$\sin \alpha = \cos \phi \cos \gamma = \cos \phi \sin \theta. \quad (2)$$

Substituting $90^\circ - \alpha$ from equation (2) for θ in equation (1) gives the etch rates for vertical surfaces that are not in the shadow of some other structure:

$$R(\phi, \theta) = \begin{cases} R(0) \sin \theta \cos \phi \cdot e^{a(1 - \sin^2(\theta) \cos^2(\phi))} & |\phi| < 90^\circ \\ 0 & |\phi| \geq 90^\circ \end{cases} \quad (3)$$

Averaging this etch speed over a full rotation of ϕ gives the average etch speed of vertical surfaces as shown by the dashed curve in figure 5. The ratio between the two etch rates is shown in figure 5 by the dash-dotted line.

These graphs can be understood as follows. For small angles, the ion beam is (almost) parallel to vertical surfaces, so they will hardly be etched, while the horizontal surfaces are etched normally, so the ratio approaches infinity as θ approaches 0. This will allow selective etching of horizontal surfaces but because of the (almost) normal incidence there is hardly a shadowing effect anymore. At around 30° the etching angle for vertical surfaces is close to the optimum etching angle for most of the time that it is exposed to the beam, while the etch rate for horizontal surfaces is still very close to that for normal incidence, and therefore the etch speed ratio reaches a minimum. At around 60° the etch rate for horizontal surfaces is quite optimal, while for vertical surfaces the average etch speed is similar for 30° and 60° , so here the ratio reaches a maximum, and horizontal surfaces can be etched with some selectivity. Additionally, since the beam is now significantly tilted, clear shadows will be cast by the structures. Further increasing the angle has little effect on the etch rate of vertical surfaces, while the horizontal surfaces are hardly etched anymore because the beam becomes increasingly parallel to these surfaces. This would allow selective etching of vertical surfaces; however, for most patterns they would be in the shadow of another structure most of the time.

For what seems to be the ideal angle for selective etching from figure 5, 57° , thermally oxidized silicon ridges formed by deep reactive ion etching were subjected to ion beam etching for 30 min, broken, and then imaged by SEM. In this experiment we have chosen to not completely remove the oxide from the top, because in that case there would be no reference surface for determining the etch rate on the top (except when the etching process would have stopped exactly at the silicon oxide-silicon interface, which is difficult to achieve with ion beam etching). Also, ridges from the same wafer that were not etched by an ion beam were broken and imaged.

Figure 7 shows an overlay of a thermally oxidized (90 min, 1000°C , water vapor atmosphere) structure that was subjected to ion beam etching at 57° , and one that was not, both from the same wafer. From the top, on average about 392 nm is removed, while from the sidewall on average only 117 nm was removed. This means the etching ratio between horizontal and vertical surfaces is in this case 3.35, which is higher than the factor of about 2.5 that would be expected from figure 5. That means that the technique works even better than expected. This improvement may be caused by the roughness of the 'vertical' silicon oxide surfaces resulting from the Bosch etching recipe that was used to shape the original silicon structure. Because

Figure 6. Schematic representation of a rotating 3D silicon structure with a conformally grown layer of silicon oxide, which is etched at various angles by the ion beam (red ‘pencils’), depending on the orientation.

Figure 7. Overlay of cross-sectional SEM images of an oxidized silicon structure that was subjected to ion beam etching under 57° and one that was not etched. The scale bar is 500 nm.

of this roughness there is a local variation in sidewall angle, resulting in an etch speed lower than predicted by the model, which assumed a smooth vertical surface.

The minimum aspect ratio for which the shadowing effect works is determined by the chosen ion beam angle. For an angle θ , a structure with height h will cast shadows up to $h \sin \theta$ away, so $h \cdot 0.84$ for $\theta = 57^\circ$. Every lower horizontal surface that is further away from a structure than this distance will be etched with the same speed as the top surfaces. However since some overetch is always needed to be sure of complete silicon oxide removal at all top surfaces, this aspect ratio requirement will in practice be even more stringent, since the bottom surfaces are not always in the shadow, so even the parts of these surfaces that are within this distance have a finite etch speed.

The consequences of this aspect ratio limitation were seen in figure 3(c). Most parts of the large lower-lying horizontal surfaces that surround these structures were never in the shadow of any structure, and therefore in step d as shown in figure 2, the silicon oxide on these surfaces etches with the same speed as the horizontal silicon oxide surfaces on top of the silicon structures. Therefore the silicon oxide is also completely removed from the large lower-lying surfaces in this step. The subsequent retraction of the polysilicon layer underneath the silicon oxide layer will then proceed along the vertical walls from both the top and the bottom, leaving only a band of silicon oxide halfway along the vertical surfaces in the final device, which is shown clearly in figure 3(c).

4. Modify the bottom part of a structure

This section describes the technique by which the bottom part of a silicon micro-/nanostructure can be exposed selectively, while keeping the top part covered in silicon oxide, as shown in figure 1(b).

4.1. Fabrication

The fabrication procedure is shown schematically in figure 8. Steps (a)–(j) are the same as for the process described above for only covering the top part of a structure, except that in step (c), before all the other layers, another 50 nm layer of silicon rich nitride is deposited by LPCVD as described in SI section 1 for step (c) of that process. Also, in step (j) the hot phosphoric acid solution etches both layers of silicon rich nitride: the outer layer is completely removed, and the inner layer is patterned by the silicon oxide hard mask that remains. Details of the further steps after step (j) are given in SI section 2.

The extra silicon nitride layer and the LOCOS step are necessary to invert the pattern that was created in the same way

Figure 8. Schematic process outline for opening only the bottom part of silicon structures (■ silicon substrate, ■ silicon oxide, ■ silicon nitride, ■ polysilicon). (a) Silicon wafer, (b) deep reactive ion etching of patterned wafer to create vertical sidewalls, (c) conformal coverage of all structures with subsequently silicon nitride, silicon oxide, silicon nitride, polysilicon and silicon oxide, (d) removal of silicon oxide from the top, (e) isotropic etching of polysilicon to the desired height, (f) isotropic etching of silicon oxide, (g) isotropic etching of silicon nitride, (h) isotropic etching of polysilicon, (i) isotropic etching of silicon oxide (j) isotropic etching of silicon nitride, (k) isotropic etching of silicon oxide, (l) local oxidation of silicon and (m) isotropic etching of silicon nitride. See text for a more detailed description.

as in the procedure for opening the top part of a structure. Such an inversion requires the transformation of a thin layer of one material into another in a controlled way. This additional requirement further limits the choices of materials and methods with which this technique could be achieved.

A properly patterned silicon nitride layer is already formed in step (g). However the polysilicon layer could not be removed without damaging the silicon structures if the underlying layers and subsequent steps were not used.

To give an example of the applicability of this process, after the final processing step an additional silicon etching step was performed to obtain a new structure.

4.2. Results and discussion

Figure 9 shows some examples of the structures obtained by applying the bottom modification process to silicon structures. Again the procedure can be applied to both holes (figure 9(a)) and pillars (figures 9(c) and (d)) and the transition can be controlled to be at various heights (figures 9(c) and (d)) and is well defined (figure 9(b)). The only differences with the top modification process is that the areas covered by silicon oxide and the uncovered areas are now interchanged. This is also true for the band patterns that are formed on structures surrounded by large open areas, as seen in figure 9(e), which also shows again the roughness tolerance of this technique.

Figure 9. SEM images of silicon structures of which only the top part was covered with silicon oxide (lighter gray): (a) microholes, (b) close up of a sidewall at the point where the silicon oxide starts, micropillars with (c) a small and (d) a large part covered by silicon oxide, and (e) a structure where the silicon (darker gray) is only exposed at the middle of the sidewalls, while everything else is covered in silicon oxide. Scale bars: (a) 5, (b) 0.5, (c) 25, (d) 25 and (e) 25 μm .

An example of a structure resulting from another silicon etching step after the final process step is shown in figure 10. The silicon was completely removed from the lower part of the structure, leaving only the top part: a free standing perforated silicon membrane.

5. Modification at an intermediate height

This section describes the technique by which the middle part of a silicon micro or nanostructure can be exposed selectively, while keeping the bottom and top parts covered in silicon nitride, as shown in figure 1(c).

5.1. Fabrication

The fabrication procedure is shown schematically in figure 11. For more detail, see SI section 3.

In principle, the same ideas are used as for the first two processes, but for the definition of the band another newly developed procedure was added here. The transition point between the top and bottom parts of the structure that was defined in the other processes is used here as a starting point to define a band locally. This procedure is shown in more detail in figure 12. The LOCOS is used to grow a silicon oxide that starts exactly where the silicon nitride stops. Subsequent isotropic thinning of the silicon nitride layer widens this transition point so that a narrow line of the layer underneath (polycrystalline silicon) can be accessed, and isotropically etched/retracted to define the desired band. This technique is comparable to the process reported previously by Berenschot *et al* [42], where a larger feature was developed by etching a polysilicon layer through a nanoscale opening.

Figure 10. SEM image of a free-hanging silicon membrane created by underetching structures of which only the top was covered by silicon oxide (lighter gray). The scale bar is 25 μm .

Another difference is that no oxide layer is used to facilitate the removal of the two polysilicon hard mask layers. Instead, the polysilicon hard mask is only used for partially etching the silicon nitride layer underneath. Because the silicon nitride was not etched completely, the polysilicon hard mask can then be removed without damaging anything underneath the silicon nitride layer. After removal of the polysilicon, the patterning of the silicon nitride is completed by etching until the previously thinned region has completely been etched away, leaving a layer of silicon nitride only in the regions which were previously covered by the polysilicon hard mask.

5.2. Results and discussion

Figures 13(a)–(c) shows structures where the polysilicon retraction shown in step e in figure 11 was performed for 20 min and in step l for 1 min. Indeed a narrow band of silicon nitride was removed near the top of narrow (figure 13(a)) and wide

Figure 11. Schematic process outline for opening only a horizontal band on silicon structures (■ silicon substrate, ■ silicon oxide, ■ silicon nitride, ■ polysilicon). (a) Silicon wafer, (b) deep reactive ion etching of patterned wafer to create vertical sidewalls, (c) conformal coverage of all structures with subsequently silicon nitride, polysilicon, silicon nitride, polysilicon and silicon oxide, (d) removal of silicon oxide from the top, (e) isotropic etching of polysilicon to the desired height, (f) isotropic etching of silicon oxide, (g) timed isotropic etching of silicon nitride, (h) isotropic etching of polysilicon, (i) (see figure 12 for a close up view of steps i-l) isotropic etching of silicon nitride (j) local oxidation of the polysilicon (not the full thickness), (k) timed isotropic etching of less than the full thickness of the silicon nitride, (l) isotropic etching of polysilicon to the desired band width (m) isotropic etching of silicon oxide (n) timed isotropic etching of silicon nitride (o) isotropic etching of polysilicon (p) timed isotropic etching of silicon nitride. See text for a more detailed description.

(figure 13(c)) micropillars and for microholes (figure 13(b)). However, some structures show holes in the silicon nitride on the sidewalls above the band (figures 13(b) and (c)). This effect is even more pronounced when the polysilicon retraction times are increased (figure 13(d)) and for some structures the silicon nitride is completely removed from the upper part of the sidewalls (figure 13(e)). This is probably caused by a failure of the silicon oxide layer formed in step j as shown in figure 11. The rough sidewalls of the structures, resulting from the Bosch etching process by which they were formed, cause strong local curvatures in the conformal layers that are formed on these sidewalls. This local curvature causes stress during the oxidation step, resulting in locally thinner silicon oxide points, especially since low temperature (900 °C) dry oxidation was used. The hot phosphoric acid and TMAH that are used in the subsequent steps also have a finite etch speed

Figure 12. Close-up view of part of the process shown in figure 11 (■ silicon oxide, ■ silicon nitride, ■ polysilicon). (i) After stripping silicon oxide, a silicon nitride hard mask is left on the polysilicon (j) local oxidation of the polysilicon (not the full thickness), (k) isotropic etching of half the thickness of the silicon nitride, (l) isotropic etching of polysilicon.

Figure 13. SEM images of various silicon microstructures from which a narrow band of silicon (darker gray) was uncovered, while the remainder of the structure remained covered in silicon nitride: (a) narrow micropillars, (b) narrow microholes and (c) wide micropillars, all with 20 and 1 min polysilicon retraction for the height and band with definition respectively, and further (d) wide micropillars where 40 and 36 min of retraction was used respectively, and (e) wide microholes where 60 and 6 min of retraction was used. Scale bars: (a) 0.5, (b) 5, (c) 5, (d) 25 and (e) 25 μm .

Figure 14. SEM image of silicon pillars covered by dielectric layers from which a band has been removed. The scale bar is 25 μm .

for silicon oxide, such that pinholes in the silicon oxide layer are formed at these thinner points. The polysilicon retraction step now also retracts the polysilicon with such pinholes as starting points, causing circular defects in the polysilicon, or even complete removal of the polysilicon in these regions for longer etching times.

However, this problem can probably be resolved by growing a thicker silicon oxide. It might also help to reduce the thinning time of the silicon nitride in step k as shown in figure 11, since especially the selectivity of the hot phosphoric acid etchant between silicon nitride and silicon oxide is poor (roughly 10 : 1).

Despite some remaining engineering challenges, the feasibility of this procedure for creating an open band on a sidewall was clearly shown by the results for short TMAH etching times. Again in this case well-defined

Figure 15. SEM image of silicon pillars on which a dielectric diffusion barrier has been used during the doping process. In this way, a confined doped region is obtained at a defined position along the pillar length, as highlighted by the dotted line. This has been visualized by FIB cross sectioning and chemical staining. The scale bar is 500 nm.

transitions were defined for both microholes and micropillars of different sizes.

To show that the band pattern can also be used for functional local modification along the sidewalls of silicon structures, the remaining dielectric pattern was used as a diffusion barrier during a diffusion doping process, as described in SI section 3. A pillar was then cut in half along its axis using focused ion beam milling, and the doped regions were etched using a staining solution. Figure 14 shows the silicon micropillars with the opened bands. Visualization of the doping inside the pillar is shown in figure 15. Although the contrast is weak, a lighter area can be seen on both sides of the pillar, which is the doped region, that was etched faster by the staining solution than the undoped silicon.

6. Conclusion

Versatile, integrated circuit technology compatible wafer-scale processes for patterning sidewalls of silicon structures were presented and successfully demonstrated in this study. The impact angle dependent etch rate of silicon oxide in an ion beam etching system was characterized, and it was shown that this angle dependence can be used for opening horizontal silicon oxide surfaces while leaving vertical surfaces protected. The retraction of polysilicon underneath a dielectric layer was shown to be a reliable, well-controlled and roughness insensitive method for defining a hard mask edge with an offset to an existing edge, without additional optical lithography steps. A smart combination of these techniques can be used to selectively open any desired region along the vertical sidewall of a structure, as long as the open space between such structures is smaller than the height of the structures.

The resolution of these techniques is in the order of magnitude of the layer thicknesses used. Therefore it can, in principle, be scaled down to the nanometer range by using thinner layers. However, at the layer thicknesses used in the present study (50–400 nm) defects have been detected for certain geometries. Therefore, the downscaling of especially the silicon oxide layer thicknesses will need to be accompanied by careful tuning of etching parameters in several of the fabrication steps involved. Furthermore, the retraction of a thinner polysilicon layer by wet chemical etching may lose the linear dependence on etch time as the etch rate may become transport limited.

It has been shown that the locally opened regions can be used for selective deposition, modification or removal of material at an arbitrary height along the vertical sidewall of silicon structures. One very relevant recent application in which we have used part of the methods described here is in the local coverage of silicon pillars with an electrocatalyst for the purpose of solar hydrogen generation [58]. The demonstrated applications are only examples, and these techniques can be considered for application in many other fields. From the references cited in the introduction section, it can be seen that 3D micro and nanostructures are used in a broad range of fields. Some examples are micro and nanoelectronics, scanning probe microscopy, (bio)sensors, MEMS/NEMS, microfluidics, nanostructured surfaces, cell studies, catalysis, photonics, energy conversion and storage, supercapacitors, tissue engineering, filtration, chromatography, healthcare, photovoltaics, computer memory, mixing, acoustics and thermoelectrics. The demonstrated fabrication methods are potentially useful in any of these fields if the parallel fabrication of large amounts of 3D micro and nanostructures is desirable.

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