RF Transconductor Linearization Robust to Process, Voltage and Temperature Variations

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Abstract -- Software defined radio receivers increasingly exploit linear RF V-I conversion, instead of RF voltage gain, to improve interference robustness. Unfortunately, the linearity of CMOS inverters, which are often used to implement V-I conversion, is highly sensitive to Process, Voltage and Temperature variations. This paper proposes a more robust technique based on resistive degeneration. To mitigate 3rd order IM3 distortion induced by the quadratic MOSFET I(V) characteristic, a new linearization technique is proposed which exploits a floating battery by-pass circuit and replica biasing to improve IIP3 in a robust way. This paper explains the concept and analyzes linearity improvement. To demonstrate operation, an LNTA with current domain mixer is implemented in a 45nm CMOS process. Compared to a conventional inverter based LNTA with the same transconductance, it improves IIP3 from 2 dBm to a robust PIIP3 of 8 dBm at the cost of 67% increase in power consumption.

Keywords— CMOS, software-defined radio, receiver, linearity, linearization, IIP3, negative feedback, transconductor, multi-band receiver, reconfigurable receiver, SAW-less receiver, wideband receiver, software defined receiver, cognitive radio receiver, Figure-of-Merit, Process Voltage Temperature (PVT) variations, robust circuit design.

I. INTRODUCTION

The development of low-cost RF front-ends that meet the requirements of both existing and emerging wireless standards (e.g. GSM, UMTS, LTE, LTE-A, etc.) is challenging due to the wide distribution of frequency bands [1]. The presence of strong out-of-band interferers and the absence of tunable high-Q RF band-select filters pose strong linearity requirements on the receiver front-end. Typical commercial front-ends use a bank of dedicated filters to separate the various frequency bands. Such implementations are expensive, as to the bill-of-materials scales linearly with the number of bands addressed. Hence more flexible receivers with less or no dedicated filtering have been developed, that can be used to cover different frequency bands at the same time and are reviewed in [2-4].

Traditional radio receivers exploit an impedance matching low-noise amplifier ("LNA") with voltage gain followed by a voltage driven mixer. Alternatively, a low noise transconductance amplification ("LNTA") can be used followed by a current commutating mixer (see Fig.1). Often, this LNTA also realizes impedance matching, although not always. This latter architecture has gained popularity during the last decade, as it can both achieve very good linearity and low noise, especially when a passive mixer is used. Historically, the fact that 1/f noise of a MOSFETs biased at V_{DS}=0 is zero has been an important reason to choose for a passive mixer, where early designs use a voltage-mode LNA with voltage mode passive mixer [5]. A narrowband LNTA followed by a current-driven mixer was proposed in [6] and favorable 1/f noise and linearity results were reported compared to active mixer solutions with a narrowband LC-based LNA [6]. Later inductor-less wideband designs stress the benefits of RF V-I conversion to improve bandwidth [7] and interference robustness in a multi-band or wideband software radio front-end context [8-10]. To grasp the potential linearity benefits intuitively, it may be instructive to realize that the output voltage swing of a voltage amplifier is hard limited to V_{DD}, while there is *no hard absolute limit* on the output current of a V-I converter (see Fig.1)

if low ohmically loaded. Hence, handling strong interferers in the current domain can be beneficial. Conceptually, the idea is to *avoid voltage swing and voltage gain at RF*. Instead, only V-I conversion is done at RF, and I-V conversion is moved to baseband (see Fig.1), where it can be combined with low-pass filtering to eliminate blckers [7, 10, 11]. Moreover, the low virtual ground node impedance gets upconverted from node D to B in Fig.1, reducing the output voltage swing of the LNTA, which is beneficial to reduce V_{ds}-swing related LNTA nonlinearity [8, 11].

The V-I conversion based receiver concept can also be combined with the impedance matching noise cancellation concept [4, 12]. In [13], input matching is provided by a passive switched resistor mixer path known as the main path as shown in Fig.2. The noise of the matching resistor R_m is cancelled at the output of the receiver by the "Frequency-Translated Noise Cancellation" (FTNC) technique [7, 13]. Compared to the noise cancellation technique described in [12], the cancelling does not occur at RF but at baseband after down-conversion. The upper signal path, known as the auxiliary path (label "aux"), achieves noise cancellation by converting the receiver's input voltage to an RF current, using a transconductor Gm with high ohmic input. This current is down-converted by a current driven passive mixer as shown in Fig.2, I-V converted and subtracted from the main path, where noise cancelling occurs to achieve a low NF. As the main path is very linear (switched resistor mixer) and its distortion is actually also cancelled like its noise by the auxiliary path, the *transconductor now becomes the noise and linearity bottleneck*. To achieve high resilience to out-of-band interference, a high linearity transconductor is wanted.

Many recent receiver front-ends [11, 13-15] use a CMOS inverter as a transconductor due to its high linearity and relatively good "Normalized Signal to Noise Ratio" [16]. However, this linearity is achieved by "complementary derivative superposition" [17], which relies on cancellation of PMOST and NMOST distortion terms. This cancellation critically depends on biasing and is sensitive to Process, Voltage and Temperature (PVT) variations. In this paper, the

linearization technique for transconductors first presented in [18] will be further analyzed. It exploits negative feedback by resistive degeneration, but aims to avoid the problem of IM3 induced by the quadratic MOSFET term in combination with negative feedback. We will show that this is possible by adding a floating battery in a complementary V-I conversion circuit. The linearity benefits and limitations will be analyzed, with special attention to the robustness over PVT variations.

In Section II, the properties of the CMOS inverter as a transconductor are reviewed with focus on linearity limitations induced by PVT variations. In Section III, the effect of using resistive degeneration to improve IIP3 is analyzed. It will be shown that the full advantage of the negative feedback is not obtained due to second-order to third-order conversion of distortion. This discussion leads to the new transconductor circuit proposal which is presented in Section IV. Section V presents its implementation details and the chip used to measure its performance which is presented in Section VI. Section VII finally draws conclusions based on the measurements and theory.

II. CMOS INVERTER AS A TRANSCONDUCTOR

For a CMOS inverter (Fig.3), the transconductance g_m is the sum of the transconductances $g_{m,n}$ and $g_{m,p}$ of the NMOST and PMOST respectively, while reusing the same bias current. Hence both transistors contribute signal current, resulting in low noise figure and good power efficiency (high g_m and g_m/I_d ratio). The low impedance loading at the inverter's output (Fig.1) due to passive mixer's upconversion of virtual ground impedance not only makes it linear but also extends the RF bandwidth [8] by pushing the output pole to a higher frequency.

For low drain voltage swings, the output current variation i_o is mainly defined by the input (gate) voltage perturbation v_i from the bias point, which can be written as a Taylor series expansion:

$$i_o \approx i_o' v_i + i_o'' \frac{v_i^2}{2} + i_o''' \frac{v_i^3}{6};$$

$$i_o = i_{ds,n} + i_{ds,p}\,; i_o' = i_{ds,n}' + i_{ds,p}' = g_{m,n} + g_{m,p}\ , V_{IIP3} = \sqrt{\frac{8g_m}{i_o'''}} \quad (1)$$

Here, $i_{ds,n}, i_{ds,p}, i_o$ are the current of the NMOST, PMOST and output of the inverter, i_o', i_o'' and i_o''' are the derivatives of the output current and V_{IIP3}[§] is the corresponding input referred third order intercept point of the inverter [17]. These are illustrated in simulation results of Fig.3. By properly sizing the transistors, and adjusting the biasing, it is possible to achieve cancellation of the third order derivative. Notice the peaks in the V_{IIP3} (Fig.3) corresponding to the zero crossings in i_o'''. This linearization technique is known as complementary derivative super-position [17]. However, in practice these V_{IIP3} peaks (sweet spots) have a rather limited benefit as they rely on cancellation between derivatives of currents of the P- and N-device, which vary with PVT. Hence, we look for more robust ways to improve linearity. Moreover, sharp peaks only give good linearity for low swing, while higher order distortion products strongly come up with increasing voltage swing. In a realistic 45nm CMOS inverter simulated in Fig.3, the linear region is very small and occurs around $V_{GS,n}$ = 0.5V where g_m is nearly constant and its derivatives i_o'' and i_o''' have zero crossings. In literature [8, 10], IIP3 results above 10dB have been presented. However, IIP3 results over PVT spread are rarely reported. In Appendix-I, it is demonstrated that a CMOS inverter with ideal square-law MOSFETs when properly dimensioned can cancel its second order currents and becomes perfectly linear while the supply, ground and individual transistor currents still carry second order distortion. In practice second order effects likely mobility reduction but also short channel effects play a significant role. These effects are difficult to capture in simple design equations.

[§] V_{IIP3} in Volts is used here for convenience as we talk about a transconductor. For the receiver, we use P_{IIP3} in dBm with either 50Ω for single-ended or 100 Ω for (differential).

III. IMPROVING CMOS TRANSCONDUCTOR LINEARITY - RESISTIVE SOURCE DEGENERATION

Normalized SNR (NSNR) [16] defined as $NSNR\ [dB] = SNR\ [dB] + 10\log\left(\frac{\mathrm{IM3_N}}{\mathrm{IM3}}.\frac{\mathrm{BW}}{\mathrm{BW_N}}\frac{\mathrm{P_N}}{\mathrm{P_{dis}}}\right)$ is a figure-of-merit which tries to do a fair comparison of transconductors in-dependent of width scaling. Resistive degeneration is a well-known linearization technique which exploits negative feedback. A resistively degenerated MOST as shown in Fig.4a, can potentially achieve high (NSNR) when compared to other alternatives [16]. However, for low loop gain, the square-law term of a MOSFET can be problematic as it indirectly generates third-order distortion [17, 19]. To understand this intuitively, for simplicity of explanation, assume that MOS transistors are ideal square law devices. Now, if a source degeneration resistor is added as in Fig.4a, due to the quadratic drain current the source voltage $v_{S,n}$ will contain a quadratic term. The MOSFET will mix this quadratic term with a linear term on the gate (v_{IN}) to *generate third order distortion which would not exist without resistive degeneration.*

To analyze intermodulation distortion in the transconductor of Fig.4a, the gate is excited by two test-tones at frequencies f_1 and f_2 (Fig.4b). Due to the MOSFET's second order distortion, the source voltage $v_{S,n}$ has second order distortion components at frequencies f_2-f_1 and $2f_1$, $2f_2$ and f_1+f_2. The square law MOSFET term mixes these tones on the source with tones on the gate, which also results in *third* order distortion components in $i_{dsDeg,n}$ at frequencies $2f_1$-f_2 and $2f_2$-f_1. A similar effect happens in the degenerated PMOST and when the two outputs currents are added, the degenerated CMOS inverter can have more third order distortion than a CMOS inverter under the same biasing conditions. This may be a key reason for the rather rare use of degeneration in MOS based LNTAs, where the available loop gain is limited at RF [17, 19].

IV. IMPROVED LNTA

The distortion mechanism can be visualized easily in the time domain if a single tone input

voltage v_{IN} is applied to the gate node of a degenerated inverter as in Fig.5a. The voltages $v_{S,n}$ and $v_{S,p}$ at the sources of the NMOST and PMOST have fundamental terms that are in phase, while their second order harmonics are out-of phase to each other. As shown in Appendix-I, these fundamental and second order terms in $v_{S,n}$ and $v_{S,p}$ can be made equal by choosing appropriate aspect ratios of the MOSFETs. Since these quadratic MOSFET current terms that flow through the degeneration resistors (dashed-red) largely cause the third order distortion problem, we can provide another current path for these terms to avoid this distortion. This is the goal of the added "by-pass" battery V_{by} shown in Fig.5b. As the quadratic term (dashed-red) is short-circuited, so that it flows in a loop with V_{by} and the MOSFETs, it *does not generate a quadratic current in the resistors, nor does it flow to the output*. In this new LNTA topology, the individual transistors do have second order distortion currents but their source voltages will ideally have no second order distortion and hence the third order distortion generation mechanism mentioned earlier is eliminated. In practice complementary P/N mismatches will introduce residual quadratic terms again, but significantly smaller, as is analyzed in Appendix-I. Fig.5c shows suppression of third-order distortion under two-tone test in frequency domain. Fig.6a shows simulation results in terms of histograms of P_{IIP3} obtained from 50 Monte-Carlo trial runs (around nominal conditions) of the input referred P_{IIP3} of a plain CMOS inverter (Inv), and the degenerated inverter with an ideal floating battery bypass (Lin) as in Fig.6c. It can be inferred that the new concept not only reduces the spread in the P_{IIP3} but also increases the minimum $P_{IIP3,}$ thus providing a better guaranteed performance across process variations.

Fig.6b and Fig.6c show the simulated input referred P_{IIP3} of inverter (Inv) and the new transconductor (Lin) w.r.t supply voltage variation ΔV_{DD} and temperature. The plots shows that there is cancellation of distortion in all cases which can be inferred from the peaks. However, the minimum P_{IIP3}s of the inverter (4dBm for ΔV_{DD} sweep and 7dBm for temperature sweep) is much worse than that of the new transconductor (18dBm for both ΔV_{DD} and temperature

sweeps). These simulations clearly demonstrate that the robustness of the linearization technique to PVT variations.

The square-law terms in the MOSTs of the proposed LNTA will not always cancel perfectly. The advantage in V_{IIP3} for the Linearized transconductor with floating battery (index "Lin"), compared to a regular degenerated MOST (index "Deg") derived in Appendix-I is given below:

$$\frac{V_{IIP3Lin}}{V_{IIP3Deg}} \approx 20 \log \left| \frac{\sqrt{2(\beta_n^2+\beta_p^2)}}{(\beta_n-\beta_p)} \right| \text{dB} \qquad \text{(A-8)}$$

If we design for $\beta_n = \beta_p$ and assume a (rather pessimistic) worst case spread of β_n compared to β_p of 20%, we find still achieve 20dB improvement in IIP3 provided that the second to third order distortion conversion is the dominant third-order distortion mechanism. As real MOSTs, particularly in nanometer technologies are far from square-law, there are other mechanisms like mobility reduction and sub-threshold and short-channel effects. Some approximate expression for IIP3s are presented systematically in [16], but for nanometer technologies such simple modeling doesn't render a good fit to simulated results. We decided to keep the math simple and intuitive to achieve insight, and resort to simulations (BSIM4.4) for more subtle modelling.

Any floating battery implementation will suffer from a finite non-zero series impedance. The improvement in V_{IIP3} when the series impedance of the battery Z_{by} is non-zero is derived in Appendix-I using ideal-square law approximation as:

$$\frac{V_{IIP3,LinZ}}{V_{IIP3,Deg}} \approx 10 \log \left| \frac{\left(1+\frac{gm}{2}(R||\frac{Z_{by}}{2})\right)(2R+Z_{by})}{\left(1+\frac{gm}{2}R\right)Z_{by}} \right| \text{dB} \qquad \text{(A-10)}$$

Both (A-8) and (A-10) were validated by using behavioural simulations with square-law models.

To study the effect of β–mismatch between the MOSTs, the relative widths of the PMOST and NMOST were changed to create an effective β mismatch and the resulting effect on the P_{IIP3} for various degeneration factors. The P_{IIP3} results are plotted in Fig.7a are simulated

P_{IIP3}s of the resistively degenerated inverters with (continuous/Lin) and without (dotted/Deg) floating battery respectively. The dashed lines are the values predicted by (A-8). The predicted P_{IIP3} is so high that other effects start limiting P_{IIP3}. For the blue curve (low degeneration case), the second to third order distortion which should increase with residual beta mismatch (A-7) most likely cancels the already existing expansive third-order distortion term for both positive and negative mismatch. This is because the co-efficient of the second to third order distortion term is always compressive (negative) (A-7) irrespective of the sign of the second-order distortion co-efficient. The improvement in P_{IIP3} is more than 6dB in all cases and the P_{IIP3} of the proposed transconductor is quite insensitive to beta mismatch.

Fig.7b shows the simulated P_{IIP3} of the resistively degenerated inverter with (continuous/LinZ) and without (dotted/Deg) floating battery and the P_{IIP3} predicted (by A-10) of LinZ (dashed/A-10) when the series battery resistance (R_{by}) is increased as a percentage of the degeneration resistance R. Again, the actual P_{IIP3} is less than predicted by the square-law model (A-10) as other effects dominate. P_{IIP3} in this case gradually degrades when R_{by} is increased, as predicted by (A-10). For cases of low degeneration (blue), the P_{IIP3} degrades more rapidly as the linearity relies on bypassing of second-order currents through the floating battery.

V. Chip Implementation Details

Implementing a broadband high quality floating battery (V_{by}) is challenging. However, requirements can be relaxed as a low impedance path is mainly important at low frequencies (f_2-f_1) and at twice the LO frequencies ($2f_1$, f_1+f_2, $2f_2$). At low frequencies, we can achieve a low impedance path by using a floating voltage regulator, i.e. a "By-pass Amp." as in Fig.8a. At high frequencies, the capacitive path C_{by} provides a low impedance by-pass path for the double frequency terms. The regulator is implemented by a PMOS transistor (Mp) that is driven by an error amplifier (OTA). The error amplifier is an NMOS input single stage cascoded differential

amplifier as shown in Fig.8b. The feed-forward capacitors C_{ff} stabilize the negative feedback loop by cancelling the phase shift caused by the pole created by $R_{LS1p/n}$ and input capacitance of the OTA due to transistors MN1 by creating a zero. The resistors $R_{LS1p/n}$ and $R_{LS2p/n}$ are used to derive a scaled version of the supply voltage to be used as the floating battery voltage. $R_{LS2p/n}$ are made variable by adding triode MOSTs is series. MPt and MNt (Fig.8d) are also triode MOSTs. Together they are used to regulate the bias current of the inverter to counteract PVT variations on the bias current.The bias voltages VBiasP and VBiasN are derived by using replica biasing.

The inverter itself shown in Fig.8c is made width-programmable for gain, linearity and input capacitance. It is possible to switch on sections of the inverter to increase g_m to compensate for the reduction in gain due to resistive degeneration. The un-utilized inverter sections are isolated using switches (Sen) at the gate to reduce parasitic input capacitance. MP_{LN} and MN_{LN} shown in Fig.8d are used to set the LNTA in a low noise mode (without degeneration) for use in the absence of blockers.

In the the proposed LNTA any noise current generated by the By-pass Amp. (Fig.8a) that flows through Mp will circulate through the NMOST and PMOST of the inverter provided that they have the same transconductance and will not reach the output. Thus this LNTA is suitable for linear and low noise applications.

To simulate the effect of the floating battery impedance, two-tones were applied at the differential LNTA's (Fig.8d) input using SpectreRF periodic analysis. The first tone of magnitude 0.3Vrms (differential) is fixed at frequency f_1=2GHz. The second tone which is a periodic small-signal tone has its frequency f_2 swept from 1GHz to 3GHz. The periodic voltage transfer from the LNTA's input at frequency f_2 to the voltage across the By-pass Amp. at the difference frequencies $|f_2-f_1|$ from 0 to 1GHz and the sum frequencies f_1+f_2 are shown in Fig.9b. Fig.9c shows the simulated periodic small-signal output current transfer of the LNTA from its input to output at fundamental frequency f_2 (continuous) and the third order frequency $2f_1-f_2$

(dashed). The voltage developed across "floating battery" which is the same as the difference in source voltages $v_{S,n}$-$v_{S,p}$ (Fig.8) of the NMOST and PMOST indicates the non-zero magnitude of "floating battery" impedance. The second-order to third-order distortion conversion effect can be understood by following for example the two input points $f_2 = f_1$±700MHz which are indicated by red and blue respectively in Fig.9. The battery voltage at the difference frequencies ($|f_2$-$f_1|$ Fig.9b), increases with frequency due to reduction of loop-gain of the regulator loop and reaches a maximum around 700MHz and decreases due the capacitance C_{by} (Fig.8a) taking over. Correspondingly, the third order distortion (Fig.9c) has a bump with its maximum ±700MHz from 2GHz. There is a degradation of around 1.5dB in the P_{IIP3} due to the finite loop gain. At the sum frequencies (f_1+f_2), the battery voltage (Fig.9b) decreases with frequency due to capacitive impedance continuously reducing. The third-order distortion (Fig.9c)) is correspondingly tilted . The distance between the fundamental (f_1) at and IM3 term is 30dB giving a simulated input-referred P_{IIP3} of 15dBm (input power at f_1 is 0dBm).

VI. MEASUREMENTS

To verify the improvement of IIP3 due to the by-pass circuit, an experimental chip was designed with only the crucial RF components that define RF-linearity. The parts indicated in the dotted box of Fig.11a are implemented on chip. We implemented a fully differential version of the LNTA in a 45nm CMOS process. The mixers in Fig.11a are driven by 4-phase non-overlapping LO signals which are generated from an on-chip divide-by-2 circuit with 1.1V supply. The divider inputs are differential and are driven by an off-chip generated 2-times LO signal (2xLO). Four current-mode logic buffer stages improve the differential nature of 2xLO. The LNTA itself uses a 1.5V supply. Thick oxide devices were used in appropriate locations to avoid reliability problems. The active chip area (Fig.11b) is approx. 0.09 mm^2. External baseband OPAMPs were used in this research work to purely study the LNTA's linearity. All measurements were done

with a fully differential setup. The LNTA of Fig.8d can be programmed in the following two modes:

1)Degeneration OFF ("LNF"/Low Noise Figure) and 2)Degeneration ON ("Lin"/Linear Mode).

The bypass capacitor C_{by} is connected in both modes as using a series switch would degrade its high frequency Q factor. The by-pass amplifier is also kept on in "LNF" mode but at low bias. To test the beneficial effect of the by-pass in the new LNTA topology of Fig.8d, we measured IIP3 and compression of the LNTA. For the IIP3 test, we used two test tones at offsets of 0.5 and 0.7MHz from the LO frequency (f_{LO}) with swept input powers of the two test tones. For fair comparison, the transconductance the two modes was programmed to be nearly equal. Fig.10a shows the results for f_{LO} of 2GHz. We see that the P_{IIP3} improves from 2 dBm to 8 dBm. Although the absolute achieved IIP3s are less than expected from simulations, we clearly see a significant benefit in linearity of about 5 to 6dB. To see how the linearity improvement depends on frequency, we measured P_{IIP3} versus f_{LO} from 0.75 to 3GHz as shown in Fig.10b. For higher frequencies linearity improves, because the bypass capacitor is more effective there as was previously discussed.

In order to verify the LNTA topology's robustness to large signal non-linearity, a one-tone compression test was done by sweeping the power of a test tone at 500kHz from f_{LO} = 2GHz for both the modes. Compression points of -7 and -2dBm for both modes were found respectively. This demonstrates that the linearity improvement is robust for large input signals.

We also tested the combination of the AUX path at f_{LO} = 2GHz (Fig.11a) with the highly linear (P_{IIP3}~20dBm) MAIN path containing only the matching resistor and the main mixer to verify the 3dB improvement assuming a very linear main path. Indeed 8+3=11dBm was found. This shows that under noise cancellation conditions [7, 13], the LNTA dominates the distortion performance.

The measured P_{IIP3} (8dBm) value was lower than the simulated value (15dBm Fig.9). Upon investigation on the layout, we discovered excess series resistance between the LNTA output and the mixer degrading the virtual ground impedance (Fig.1) and thus limiting the achievable P_{IIP3}. When this series resistance is added in the simulation netlist, we obtain an P_{IIP3} of 10.5dBm which is close to the measurements.

To analyze the noise performance of the LNTA, we obtained the input referred noise voltage of the LNTA by referring the output noise of the LNTA path to its input via its gain. The noise excess factor (NEF) [16] of the LNTA with mixer was calculated for various LO frequencies. The results in Fig.12 show that the noise performance is only slightly degraded when using the new technique. This is because the noise of the By-pass Amp. in Fig.8d does not affect the output current of the LNTA, provided that the transconductance of the NMOS and PMOS is almost the same.

To get an impression of the robustness of the linearity improvement, the chip was heated with a hot-air blower at 150^{o}C in the "Lin" mode. The P_{IIP3} degrades only slightly by 0.55dB. The LNTA consumes 8.7 and 14.5mA in the "LNF/Low Noise" and "Lin/Linear" modes respectively.

VII. CONCLUSIONS

A circuit technique to linearize an LNTA in a robust way is proposed and analyzed. The circuit exploits resistive degeneration combined with a floating battery to address the problem of second-to-third order distortion conversion due to negative feedback with insufficient loop-gain. Although the performance is less than predicted by simulations due to layout parasitics, experimental results confirm a robust improvement of both P_{IIP3} and the large signal compression.

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APPENDIX – I

The CMOS inverter's (Fig.3) output current's (i_{Inv}) relation to the gate-source voltage of the NMOST ($v_{GS,n}$) using the square law approximation is :

$$i_{Inv} = i_{DS,n} + i_{DS,p};\ i_{DS,n} \approx \frac{\beta_n}{2}(v_{GSn} - V_{Tn})^2;\ i_{DS,p} \approx -\frac{\beta_p}{2}\left(V_{DD} - v_{GSn} - V_{Tp}\right)^2 \qquad \text{(A-1)}$$

Where, $\beta_n = \mu_n C_{OX}\frac{W_n}{L_n}$; $\beta_p = \mu_p C_{OX}\frac{W_p}{L_p}$ and $V_{Tn/p}$, C_{OX}, μ_n/μ_p, and $\frac{W_n}{L_n}$ /$\frac{W_p}{L_p}$ are the corresponding positive valued threshold voltages, oxide capacitance per unit area, carrier mobilities, and aspect($\frac{W}{L}$) ratios of the NMOST and PMOST respectively. Under quiescent bias condition ($v_{GS,n} = V_{GS,n}$) achieved by say self-biasing with $V_{GS,n} = V_{DS,n}$, the PMOST and NMOST carry the same current ($I_{Inv} = 0$). The output current perturbation i_{inv} is given by:

$$i_{inv} = g_m v_{gs,n} + \frac{\beta_n - \beta_p}{2} v_{gs,n}^2 \qquad \text{(A-2)}$$

The second order terms can be cancelled [20] by setting the appropriate aspect ratios such that $\beta_n = \beta_p$. Then we get a linear relation $i_{inv} = g_m v_{gs,n}$.

However, the current perturbation on the supply is $-i_{dsp}$, where i_{dsp} is given by:

$$i_{ds,p} = i_{DS,p} - I_{DS,p} = g_{m,p} v_{gs,n} - \frac{\beta_p}{2} v_{gs,n}^2 \qquad \text{(A-3)}$$

Thus, the supply (and similarly the ground) has fundamental and second-order terms while the output current remains linear.

Now, the second-order to third-order distortion conversion in a degenerated MOST will be derived using simple square-law model. The drain current perturbation $i_{ds,n}$ the NMOS about its quiescent $I_{DS,n}$ is given by.

$$i_{ds,n} = i_{DS,n} - I_{DS,n} = g_{m,n} v_{gs,n} + \frac{\beta_n}{2} v_{gs,n}^2 \tag{A-4}$$

When resistively degenerated, the MOST can be seen as an amplifier whose output drain current is fed back as a source voltage using the resistor R (Fig.4a). Using formulae in [17, 19] and setting the loop gain to $g_{m,n}R$ and the feedback factor to R, the output current perturbations $i_{Deg,n}$ and $i_{Deg,p}$ of the degenerated NMOST and PMOST are respectively given by:

$$\begin{aligned} i_{Deg,n} &\approx \frac{g_{m,n}}{1 + g_{m,n}R} v_{in} + \frac{\beta_n}{2\left(1 + g_{m,n}R\right)^3} v_{in}^2 - \frac{\beta_n^2 R}{2\left(1 + g_{m,n}R\right)^5} v_{in}^3 \\ i_{Deg,p} &\approx \frac{g_{m,p}}{1 + g_{m,p}R} v_{in} - \frac{\beta_p}{2\left(1 + g_{m,p}R\right)^3} v_{in}^2 - \frac{\beta_p^2 R}{2\left(1 + g_{m,p}R\right)^5} v_{in}^3 \end{aligned} \tag{A-5}$$

Using (A-5) and the approximation $g_{mn} \approx g_{mp} \approx \frac{g_m}{2}$ which simplifies the equations and gives insight into the imperfect cancellation effects, the perturbations in the output current i_{Deg} of the degenerated inverter (without floating battery) is given by:

$$i_{Deg} = i_{Deg,n} + i_{Deg,p} \approx \frac{g_m}{1 + \frac{g_m R}{2}} v_{in} + \frac{\beta_n - \beta_p}{2\left(1 + \frac{g_m R}{2}\right)^3} v_{in}^2 - \frac{(\beta_n^2 + \beta_p^2) R}{2\left(1 + \frac{g_m R}{2}\right)^5} v_{in}^3 \tag{A-6}$$

In the degenerated inverter with floating battery, the inverter (Fig.A-1a), can be treated as a transconductance amplifier with I-V relation given by (A-2) while the feedback factor is $R/2$ as the two degeneration resistors are in parallel for signal perturbations. Using formulae in [17, 19], the output current i_{Lin} of the degenerated inverter (with floating battery) with ($g_{m,n} \approx g_{m,p} \approx \frac{g_m}{2}$) is given by:

$$i_{Lin} \approx \frac{g_m}{1 + \frac{g_m R}{2}} v_{in} + \frac{\beta_n - \beta_p}{2\left(1 + \frac{g_m R}{2}\right)^3} v_{in}^2 - \frac{\left(\beta_n - \beta_p\right)^2 R}{4\left(1 + \frac{g_m R}{2}\right)^5} v_{in}^3 \tag{A-7}$$

Comparing (A-6) and (A-7), the IIP3 advantage when the second-order to third-order distortion conversion is the dominant source of third order distortion is given by (see (1)):

$$\frac{V_{IIP3,Lin}}{V_{IIP3,Deg}} \approx 20 \log \left| \frac{\sqrt{2(\beta_n^2+\beta_p^2)}}{\beta_n-\beta_p} \right| \text{dB} \quad \text{(A-8)}$$

Next, the improvement to IIP3 when the floating battery impedance Z_{by} (Fig.A-1b) is finite w.r.t the case where there is no battery (Fig.5a) will be derived. The analysis is simplified by using the assumption ($g_{m,n} \approx g_{m,p} \approx \frac{g_m}{2}$ and $\beta_n = \beta_p = \beta$) which makes the circuit symmetric about the line XX' in Fig.A-1c. As previously seen (Fig.5a), the node voltages $v_{S,n}$ and $v_{S,p}$ are in-phase for odd-order distortion terms and anti-phase for even-order distortion terms. Thus a current flows through Z_{by} only for even order distortion. This modifies the loop gain and the feed-back factor seen by the even order terms to $\frac{g_m}{2}(R||\frac{Z_{by}}{2})$ and $R||\frac{Z_{by}}{2}$ (see Fig.A-1c)instead of $\frac{g_m}{2}R$ and R in the case of no battery (A-7) respectively. Using formulae in [17, 19], the output current i_{LinZ} of the degenerated inverter with a finite-impedance floating battery is given by :

$$i_{LinZ} \approx \frac{g_m}{1+\frac{g_m R}{2}} v_{in} - \frac{\beta^2 . R . Z_{by}}{\left(1+\frac{g_m R}{2}\right)^4 \left(1+\frac{g_m}{2}(R||\frac{Z_{by}}{2})\right)(2R+Z_{by})} v_{in}^3 \quad \text{(A-9)}$$

Here, Z_{by} is the impedance of the battery at the second order frequency. Comparing (A-6) with (A-9), and using (1), the advantage in IIP3 when the battery impedance is finite is given by:

$$\frac{V_{IIP3,LinZ}}{V_{IIP3,Deg}} \approx 10 \log \left| \frac{\left(1+\frac{g_m}{2}(R||\frac{Z_{by}}{2})\right)(2R+Z_{by})}{\left(1+\frac{g_m}{2}R\right)Z_{by}} \right| \text{dB} \quad \text{(A-10)}$$

REFERENCES

[1] *3GPP TS 36.104: Evolved Universal Terrestrial Radio Access (E-UTRA); Base Station (BS) radio transmission and reception*. Available: http://www.3gpp.org

[2] A. A. Abidi, "The Path to the Software-Defined Radio Receiver," *Solid-State Circuits, IEEE Journal of,* vol. 42, pp. 954-966, 2007.

[3] H. Darabi, A. Mirzaei, and M. Mikhemar, "Highly Integrated and Tunable RF Front Ends for Reconfigurable Multiband Transceivers: A Tutorial," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 58, pp. 2038-2050, 2011.

[4] E. A. M. Klumperink and B. Nauta, "Software defined radio receivers exploiting noise cancelling: A tutorial review," *Communications Magazine, IEEE,* vol. 52, pp. 111-117, 2014.

[5] W. Redman-White and D. M. W. Leenaerts, "1/f noise in passive CMOS mixers for low and zero IF integrated receivers," in *Solid-State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27th European*, 2001, pp. 41-44.

[6] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello, "A 15 mW, 70 kHz 1/f corner direct conversion CMOS receiver," in *Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003*, 2003, pp. 459-462.

[7] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "The Blixer, a Wideband Balun-LNA-I/Q-Mixer Topology," *Solid-State Circuits, IEEE Journal of,* vol. 43, pp. 2706-2715, 2008.

[8] Z. Ru, N. A. Moseley, E. Klumperink, and B. Nauta, "Digitally Enhanced Software-Defined Radio Receiver Robust to Out-of-Band Interference," *Solid-State Circuits, IEEE Journal of,* vol. 44, pp. 3359-3375, 2009.

[9] D. Kaczman, M. Shah, M. Alam, M. Rachedine, D. Cashen, H. Lu, *et al.*, "A Single-Chip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-less CMOS Receiver With DigRF 3G Interface and +90 dBm IIP2," *Solid-State Circuits, IEEE Journal of,* vol. 44, pp. 718-739, 2009.

[10] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, A. Mirzaei, M. Mikhemar, *et al.*, "A Blocker-Tolerant, Noise-Cancelling Receiver Suitable for Wideband Wireless Applications," *Solid-State Circuits, IEEE Journal of,* vol. 47, pp. 2943-2963, 2012.

[11] Z. Ru, E. Klumperink, G. Wienk, and B. Nauta, "A software-defined radio receiver architecture robust to out-of-band interference," in *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, 2009, pp. 230-231,231a.

[12] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *Solid-State Circuits, IEEE Journal of,* vol. 39, pp. 275-282, 2004.

[13] D. Murphy, A. Hafez, A. Mirzaei, M. Mikhemar, H. Darabi, M. F. Chang, *et al.*, "A blocker-tolerant wideband noise-cancelling receiver with a 2dB noise figure," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, 2012, pp. 74-76.

[14] H. Xin and H. Kundur, "A compact SAW-less multiband WCDMA/GPS receiver front-end with translational loop for input matching," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, 2011, pp. 372-374.

[15] J. Borremans, B. van Liempd, E. Martens, C. Sungwoo, and J. Craninckx, "A 0.9V low-power 0.4-6GHz linear SDR receiver in 28nm CMOS," in *VLSI Circuits (VLSIC), 2013 Symposium on*, 2013, pp. C146-C147.

[16] E. A. M. Klumperink and B. Nauta, "Systematic comparison of HF CMOS transconductors," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on,* vol. 50, pp. 728-741, 2003.
[17] Z. Heng and E. Sanchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 58, pp. 22-36, 2011.
[18] H. K. Subramaniyan, E. A. M. Klumperink, B. Nauta, S. Venkatesh, and A. Kiaei, "RF transconductor linearization technique robust to process, voltage and temperature variations," in *Solid-State Circuits Conference (A-SSCC), 2014 IEEE Asian*, 2014, pp. 333-336.
[19] W. Sansen, "Distortion in elementary transistor circuits," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on,* vol. 46, pp. 315-325, 1999.
[20] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *Solid-State Circuits, IEEE Journal of,* vol. 27, pp. 142-153, 1992.

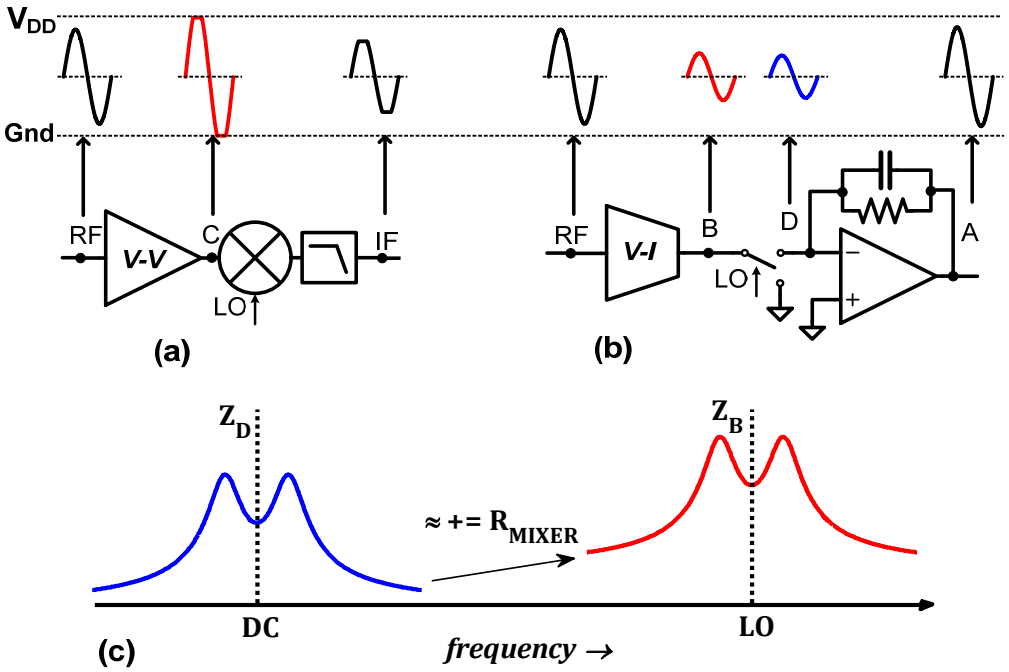


Fig.1 RF-Front-ends employing (a) Voltage gain (V-V) (e.g. LNA) followed by high-input impedance mixer (e.g. active mixer) and (b) V-I conversion followed by passive mixer driving output current into a virtual ground node D. (c) Impedance conversion via passive mixer switch from node B to D.

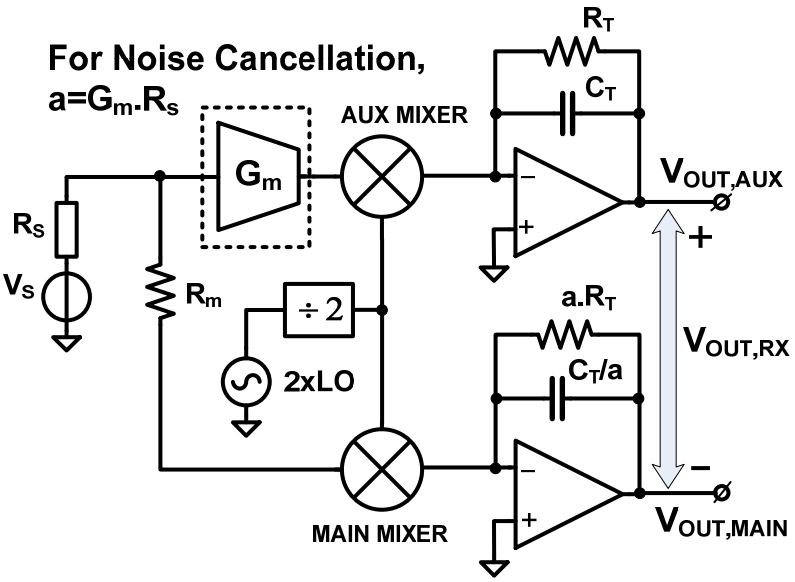


Fig.2: Receiver requiring a high linearity transconductance Amplifier (*dotted box*).

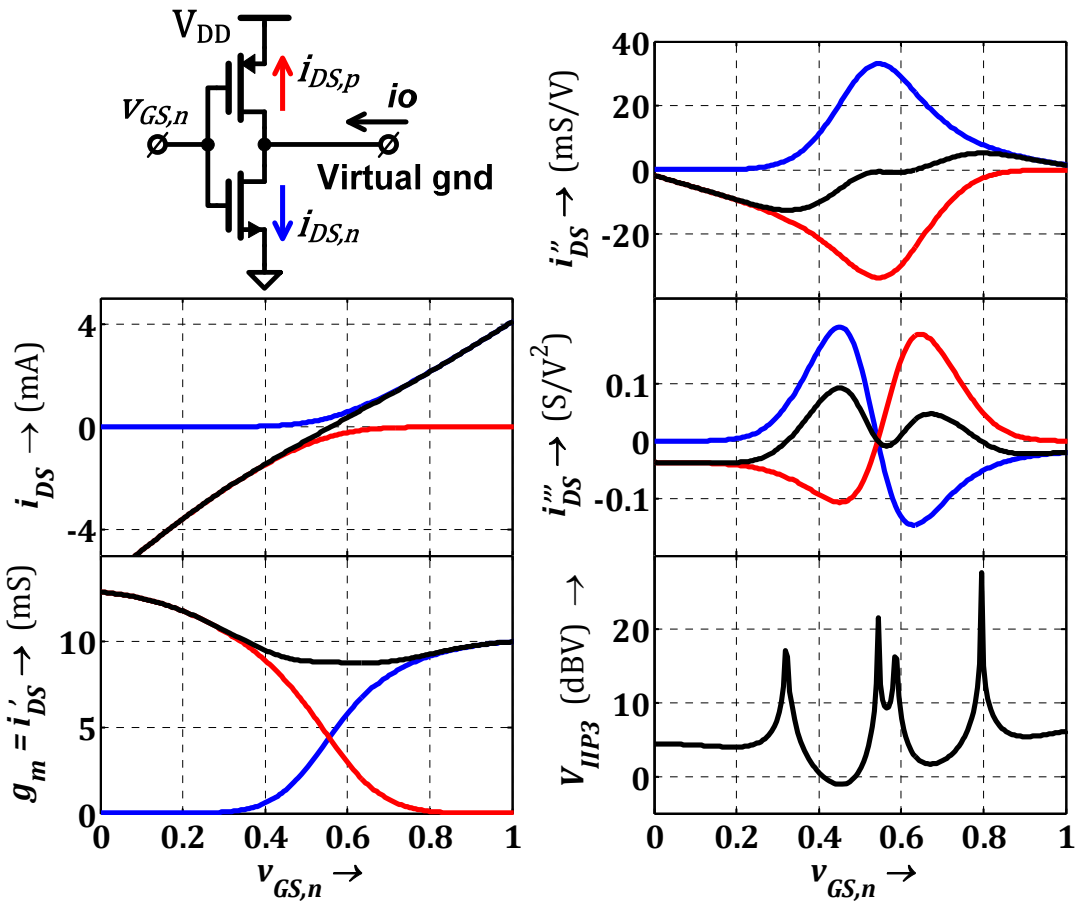


Fig.3 Output (Drain) currents and their derivatives of NMOS (blue), PMOS (red) and CMOS (black) devices in a CMOS inverter.

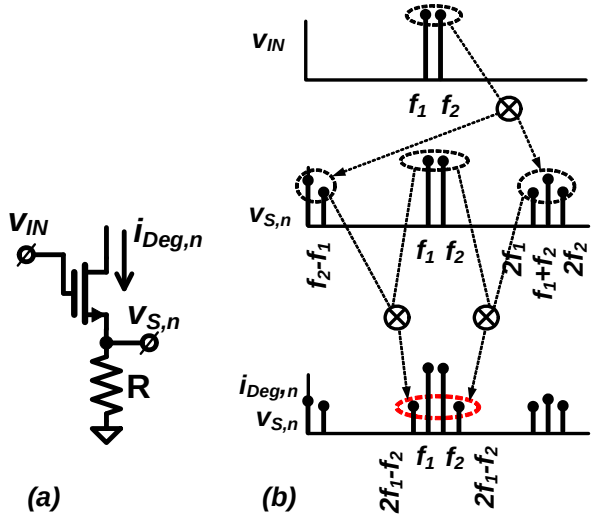


Fig.4 (a) A degenerated NMOS transistor and (b) Generation of third order distortion from second order distortion when excited by two test tones.

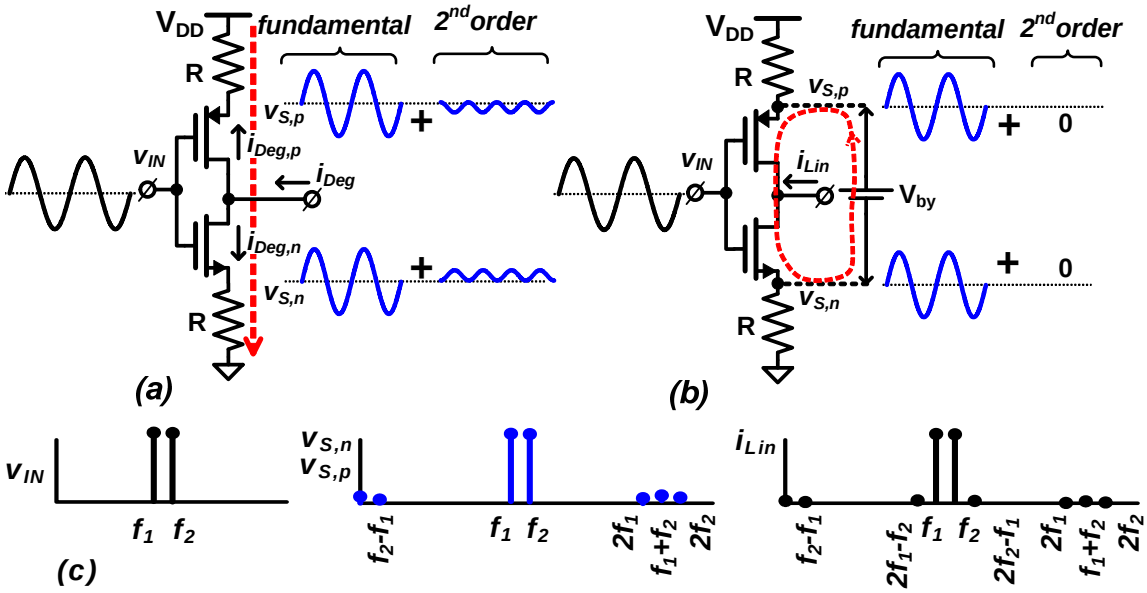


Fig.5 (a) A degenerated inverter excited by a single tone and second order distortion causing the double frequency and DC shifts at the source nodes of the NMOS and PMOS (blue). The resulting second order current (dashed-red) flows from supply to ground through resistors R. and (b) The cancellation of second-order distortion voltages using a floating battery V_{by} leading to circulating second order currents (dashed-red). (c) Mitigation of second-order to third-order distortion conversion by cancellation of the second order distortion at the source nodes of NMOS and PMOS in the circuit with floating battery when the input is excited by two test tones.

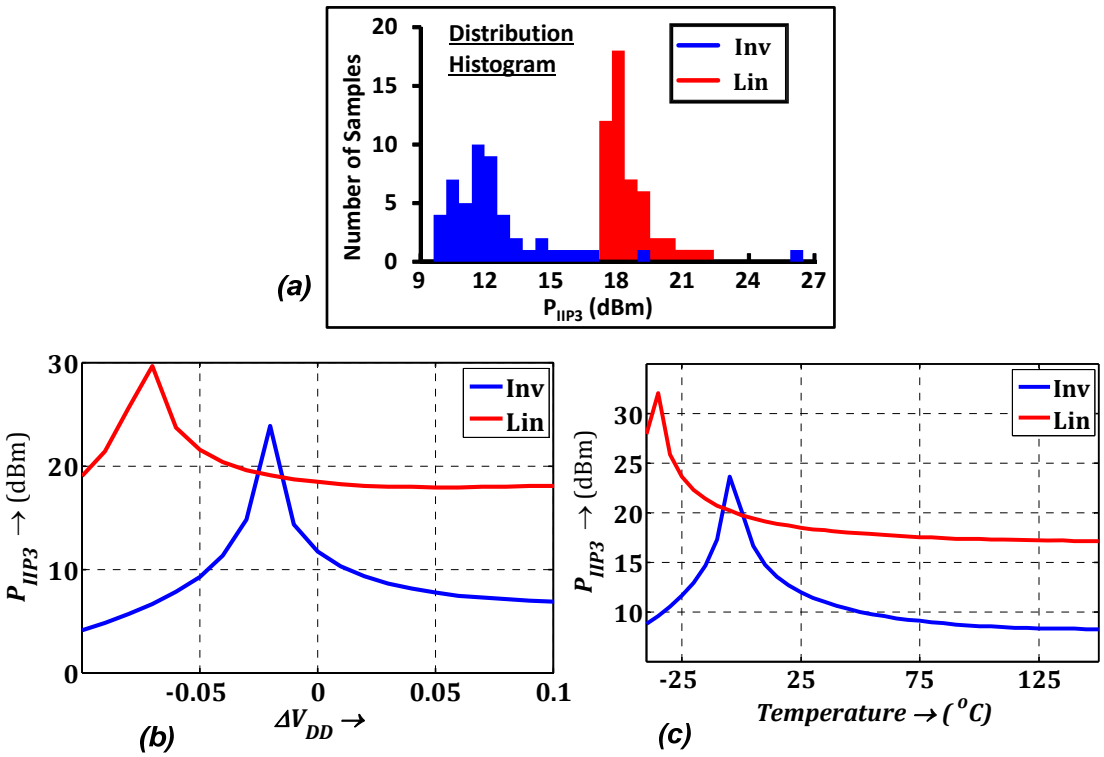


Fig.6 Simulation results of a CMOS inverter (*Inv*/*blue*) and a degenerated CMOS inverter with ideal floating battery bypass (*Lin*/*red*) . (a) Monte-Carlo simulation result of distribution of P_{IIP3} , (b) Variation of P_{IIP3} w.r.t supply voltage variation (ΔV_{DD}) around its nominal value, and (c) Variation of P_{IIP3} w.r.t temperature.

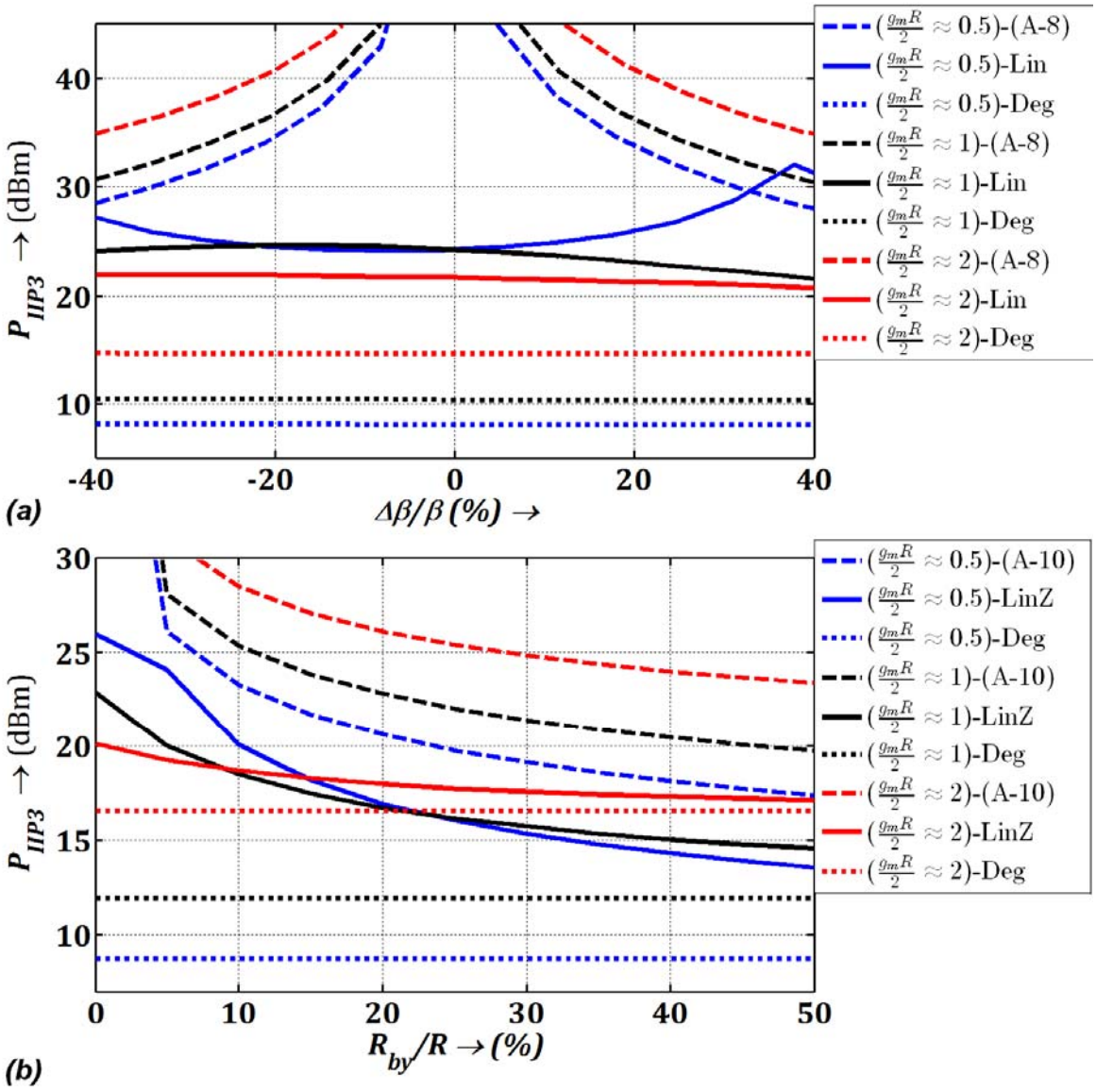


Fig.7 (a) P_{IIP3} when a floating battery is added to a degenerated CMOS inverter as predicted in (A-8) (dotted) as compared to simulations for various degeneration factors ($g_mR/2$=0.5,1,2) (a) vs β mismatch and (b) vs battery series resistance (R_{by}) as a percentage of the degeneration resistor (R).

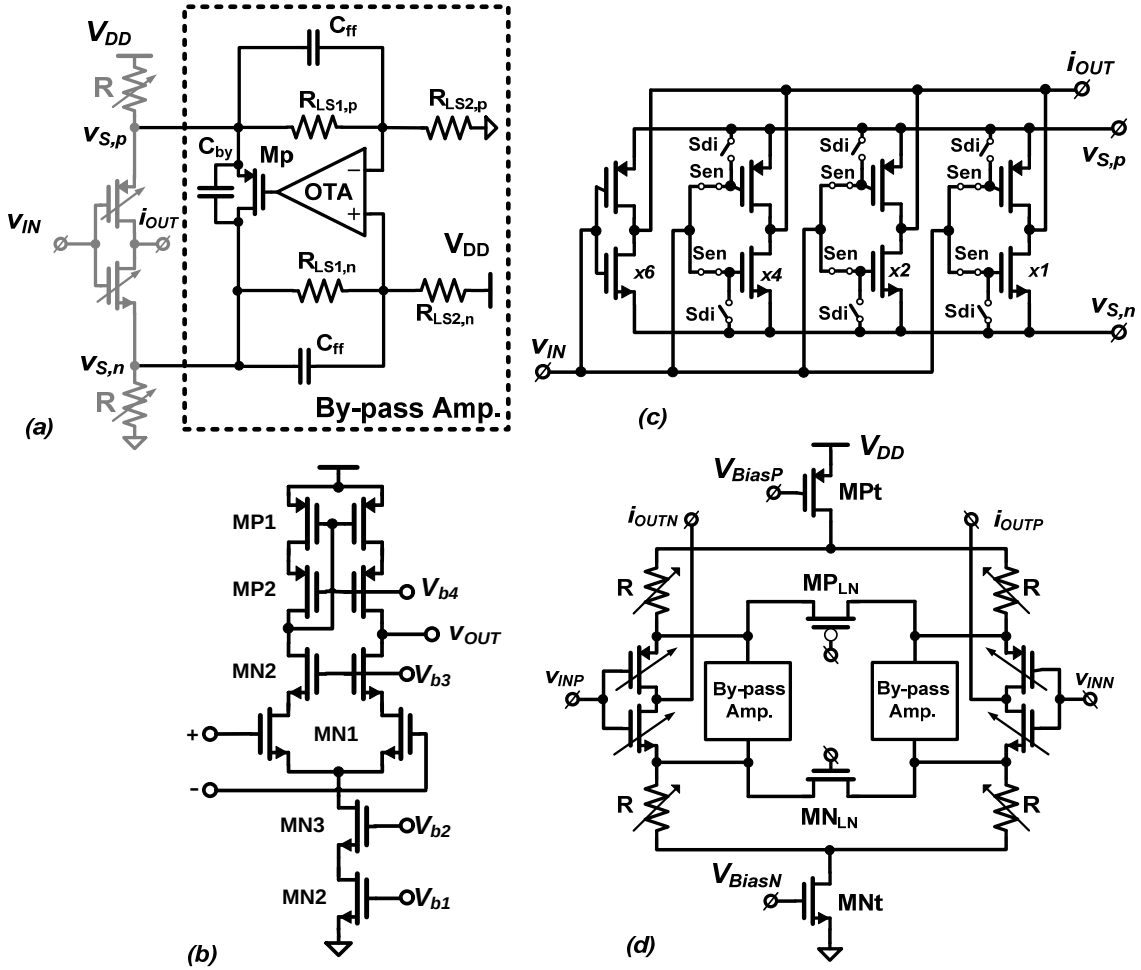


Fig.8 Schematic of (a) The improved transconductor with By-pass amplifier, (b) OTA (error-amplifier), (c) Digitally programmable transconductor, and (d) The fully differential transconductor.

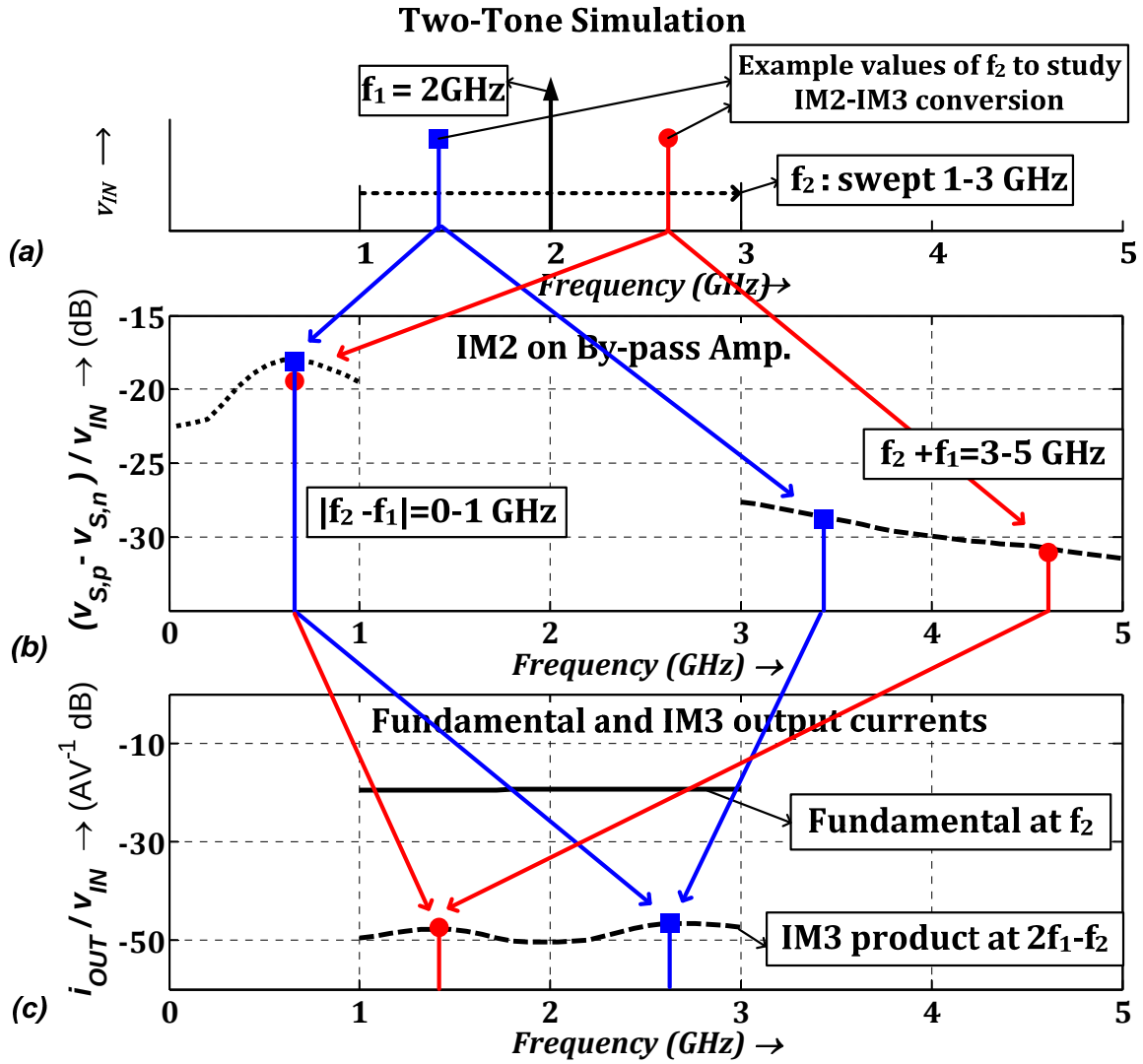


Fig.9: Simulation results of two-tone test: (a) Input test tones: First test tone of amplitude (0 dBm) at fixed frequency (f_1 =2GHz) and the second periodic small-signal test tone is swept from 1 to 3GHz. (b) The periodic voltage transfer (*dotted*) across the "floating battery" impedance Z_{by} at difference frequency ($|f_1-f_2|$ *dotted*) and sum frequencies ((f_1+f_2 *dashed*) from input at frequency f_2, and (c) The periodic output currents transfer from input at frequency f_2 of the transconductor at the fundamental frequency f_2 (*continuous)* and third order distortion frequency ($2f_1-f_2$) (*dashed)*.

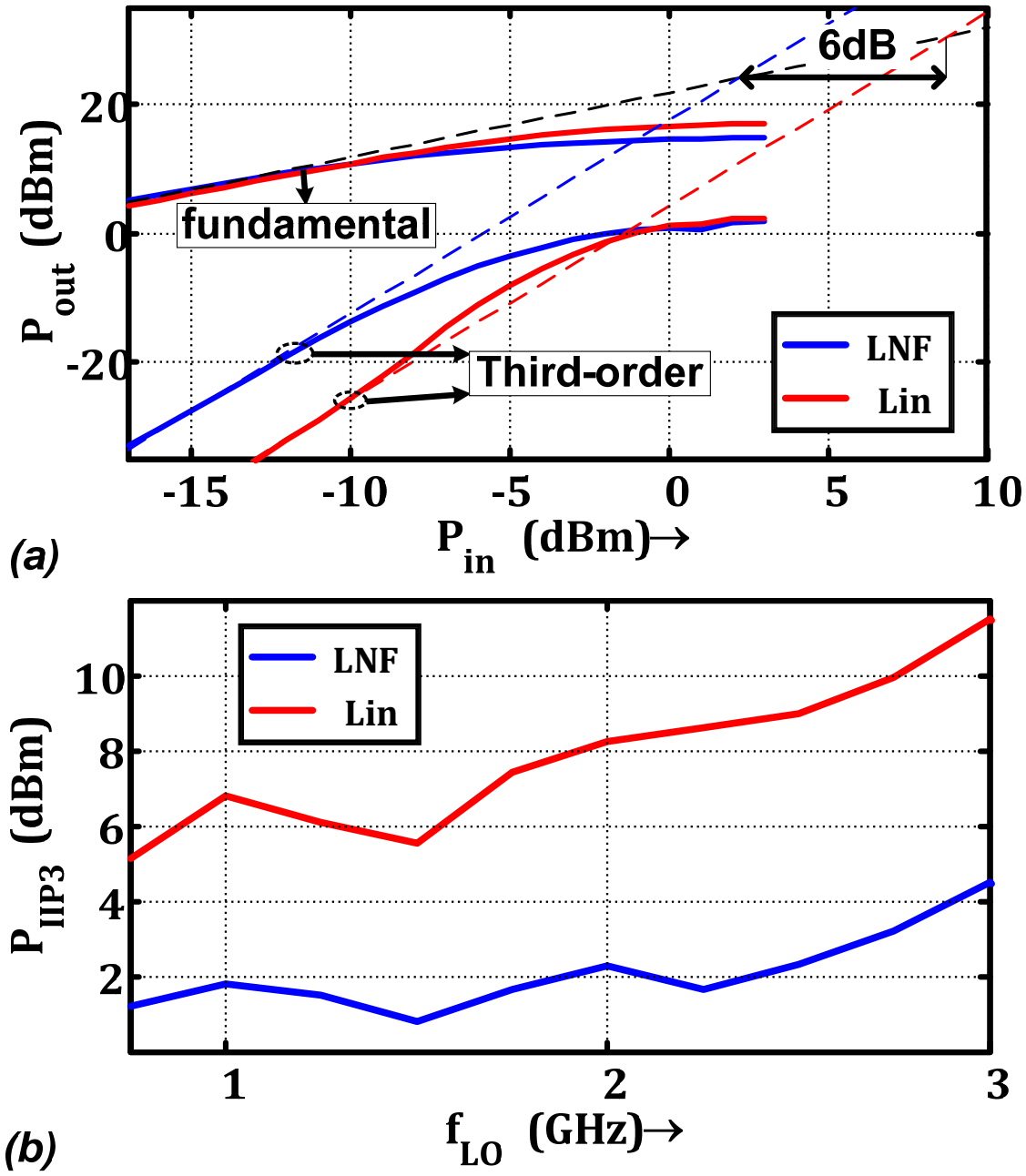
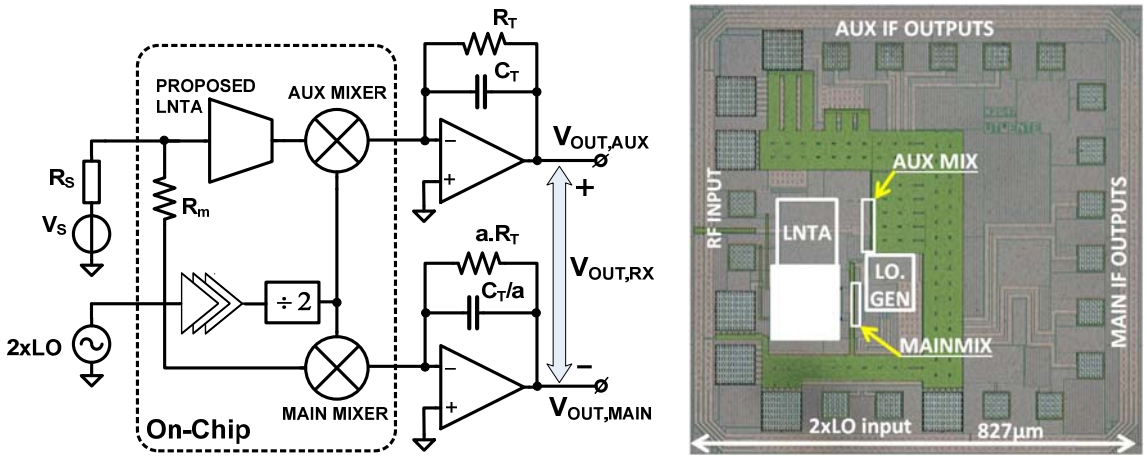


Fig.10: Measurements result of swept P_{IIP3} of the transconductor in the LNF(*blue*) and Lin (*red*) modes : (a) Input power (P_{in}) vs fundamental and third-order distortion output powers at



(a) *(b)*

Fig.11 (a) Block-diagram of the test chip, and (b) Chip Micrograph

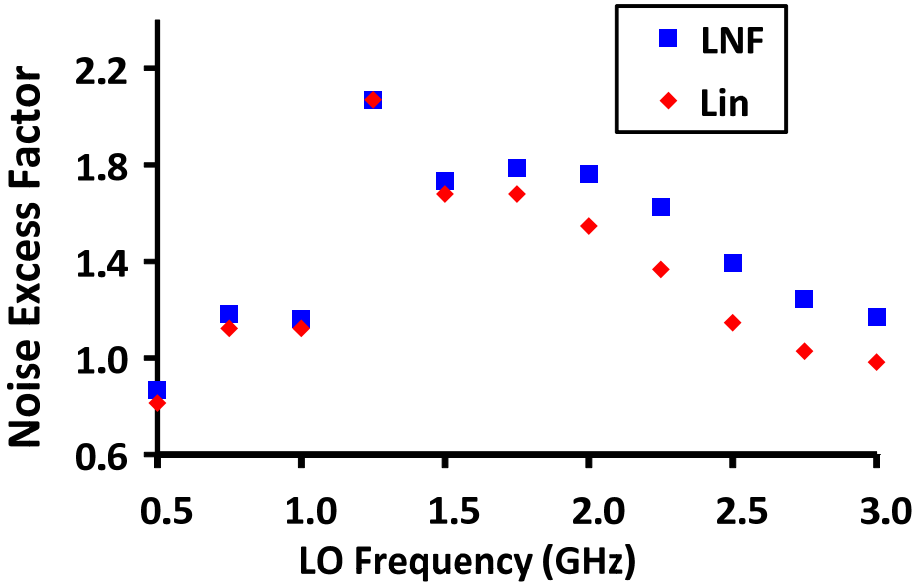


Fig.12 Measured Noise Excess factor of the LNTA in the LNF(blue) and Lin(red) modes.

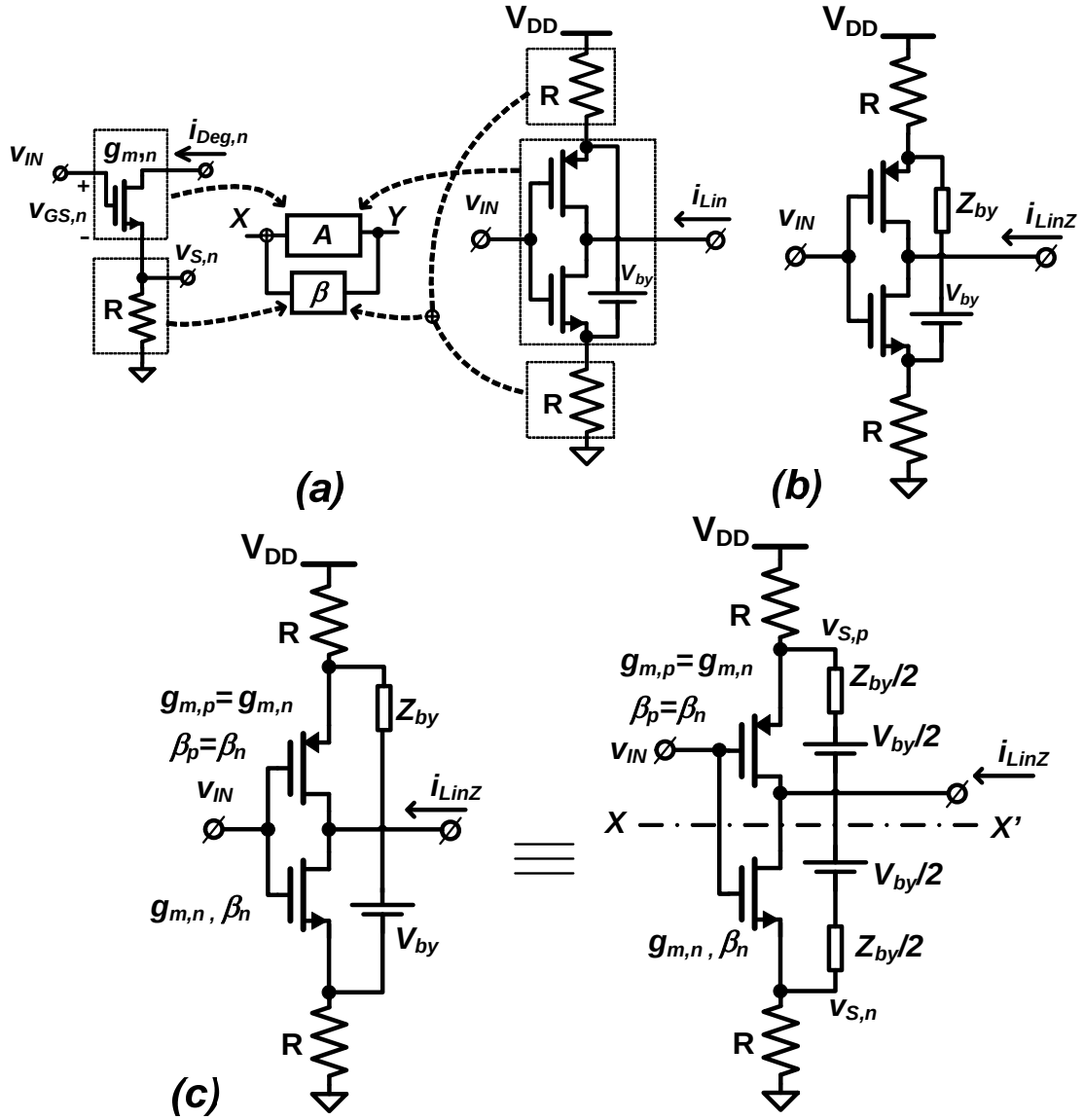


Fig.A-1: (a) Negative feedback blocks in a resistively degenerated NMOST and inverter with "*floating battery*" V_{by}, (b) The degenerated inverter with a floating battery with a finite impedance Z_{by}, (c) Identification of the line of symmetry XX' for simplified analysis in the case where the NMOST and PMOST have same g_m and β