17.3 A 1.2V 10µW NPN-Based Temperature Sensor in 65nm CMOS with an Inaccuracy of ±0.2°C (3σ) from –70°C to 125°C

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This paper describes a temperature sensor realized in a 65nm CMOS process with a batch-calibrated inaccuracy of ±0.5°C (3σ) and a trimmed inaccuracy of ±0.2°C (3σ) from –70°C to 125°C. This represents a 10-fold improvement in accuracy compared to other deep-submicron temperature sensors [1,2], and is comparable with that of state-of-the-art sensors implemented in larger-feature-size processes [3,4]. The sensor draws 8.3µA from a 1.2V supply and occupies an area of 0.1mm^2, which is 45 times less than that of sensors with comparable accuracy [3,4]. These advances are enabled by the use of NPN transistors as sensing elements, the use of dynamic techniques i.e. correlated double sampling (CDS) and dynamic element matching (DEM), and a single room-temperature trim.

The sensor's operating principle is illustrated in Fig. 17.3.1. A bias circuit generates a supply-independent proportional-to-absolute-temperature (PTAT) current I_{bias}, which biases a pair of vertical NPNs at a 4:1 collector current ratio. This results in a voltage ΔV_{be} that is PTAT, and a voltage V_{be} that is complementary to absolute temperature (CTAT). A 1st order ΣΔ ADC integrates $-V_{be}$ when the bitstream bs=1 and integrates $\alpha\Delta V_{be}$ when bs=0, so that the bitstream average $\mu=\alpha\Delta V_{be}/(V_{be}+\alpha\Delta V_{be})$ [3]. With the appropriate choice of a ($\alpha=\alpha_{PTAT}$=18), the denominator will be nearly constant over temperature, and the bitstream average will be a curvature-compensated PTAT function μ_{PTAT} [3]. In this work, however, α=2 has been chosen, since the increased granularity of the charge-balancing process results in less quantization error, for a fixed conversion time. As in [2], a digital back-end is then required to compute a PTAT output $\mu_{PTAT}=\alpha_{PTAT}\mu/[\alpha+(\alpha_{PTAT}-\alpha)\mu]=9\mu/(1+8\mu)$. The digital back-end also converts μ_{PTAT} into degrees centigrade and compensates for any residual systematic non-linearity.

The NPN transistors used in this design consist of an n+ drain diffusion (emitter), a p-well (base) and a deep n-well (collector), all standard features in deep-submicron processes. Unlike the vertical PNPs often used in temperature sensors [1-4], these NPNs can be directly and accurately biased via their collectors (Fig. 17.3.1). The resulting base-emitter voltages are independent of the transistors' current gain β, which is low and approaches unity for parasitic transistors in deep-submicron technologies. This, in turn, significantly relaxes the requirements on the bias circuit in terms of accuracy and required supply voltage.

In the bias circuit (Fig. 17.3.2), transistors Q_a and Q_b are biased by a gain-boosted cascode mirror with a 2:1 current ratio, forcing a PTAT voltage across polysilicon resistor R_E=180kΩ and making the emitter current I_E of Q_b supply-independent. The bias current $I_{bias}=I_E$ of the NPNs is then derived by generating and summing copies of the collector current I_C and the base current I_B of Q_b (via the replica circuit around Q_C). Unlike PNP-based bias circuits [3,4], the circuit in Fig. 17.3.2 does not need low-offset amplifiers. This is because the loop comprising the base-emitter junctions of $Q_{a,b}$ and resistor R_E can be directly realized with NPNs but not with substrate PNPs. However, since their base currents are relatively large (β<5), the use of common-source buffers minimizes the systematic offset of the amplifiers (current-mirror-loaded differential pairs with tail currents of 340nA, for $A_{1,3}$, and 8nA, for A_2). The minimum supply voltage of the bias circuit is determined by the mirror compliance and the BJT saturation voltage V_{CE}~0.3V. This supply voltage is much lower than that in PNP-based bias circuits which must accommodate $V_{be}>>V_{CE}$ [1-4].

In the front-end (Fig. 17.3.3), transistors Q_1 and Q_2 are biased by an array of 5 unit current sources, whose current (50nA) is derived from I_{bias}. The switches driven by en_1 and en_2, make it possible to apply either a PTAT voltage $V_{\Sigma\Delta}=\pm\Delta V_{be}$ or a CTAT $V_{\Sigma\Delta}=\pm V_{be}$ to the sampling capacitor $C_{a1,2}$ (2pF) of a 1st order ΣΔ ADC. To prevent this capacitive load from making the bias loop unstable, diode-connected BJTs $Q_{3,4}$ are used to lower the impedance at the base of $Q_{1,2}$. To generate ΔV_{be}, $Q_{1,2}$ are biased at a 1:4 collector current ratio. A bitstream-controlled DEM scheme is used to swap the current sources in a way that is uncorrelated with the bitstream [3]. Mismatch errors are thus averaged out without introducing in-band intermodulation products, resulting in an accurate 1:4 current ratio and, consequently, an accurate ΔV_{be}. To trim the sensor at room temperature, V_{be} is adjusted: the collector current of Q_1 or Q_2 can be coarsely adjusted via 4 of the current sources, while the 5th is driven by a digital ΣΔ modulator to provide a fine trim [3].

The ΣΔ modulator's integrator is based on a 2-stage Miller-compensated opamp with a minimum gain of 93dB, which is reset at the beginning of each temperature conversion. CDS is used to reduce its offset and 1/f noise. Since the modulator must operate at 1.2V, the voltage swing at the output of the integrator was scaled down by choosing $C_{b1,2}=4C_{a1,2}$. Furthermore, as shown in the timing diagram in Fig. 17.3.4, when bs=1, only one BJT is biased and only one base-emitter voltage $-V_{be}$ is integrated, instead of the $-2V_{be}$ of previous work [3,4]. However, this choice means that when bs=1, a V_{be}-dependent common-mode voltage will also be integrated. To minimize the total integrated common-mode voltage, the sign of the input common-mode voltage is alternated in successive bs=1 cycles, by setting either V_{be1}=0 and $V_{be2}=V_{be}$ in ϕ_1 (period A in Fig. 17.3.4), or $V_{be1}=V_{be}$ in ϕ_2 and V_{be2}=0 (period B). A longer settling time is required when one input of the modulator must switch between, say, V_{be} and 0V, when V_{be} is being integrated, than when one of the inputs must switch between, say, V_{be1} and V_{be2} when ΔV_{be} is being integrated. The length of each sampling phases was appropriately scaled to minimize conversion time.

The 0.1mm^2 temperature sensor (Fig. 17.3.7) was fabricated in a baseline TSMC 65nm CMOS process, and was packaged in a ceramic DIL package. The sensor's performance is summarized in Fig. 17.3.6. Even though all the transistors are thick-oxide high-threshold devices, the sensor draws 8.3µA from a supply of only 1.2V. The off-chip digital back-end decimates the output of the ΣΔ modulator with a sinc^2 filter and compensate for the non-linearity. The conversion rate of the sensor is 2.2Sa/s (6000 bits, T_1=20µs, T_2=50µs) at which it obtains a quantization-noise-limited resolution of 0.03°C. Higher conversion rates can be reached with a 2nd order modulator [3,4]. This only requires the addition of an integrator and will not significantly increase the sensor's area or power dissipation. A set of devices was measured over the temperature range from –70°C to 125°C. After digital compensation for systematic non-linearity, the inaccuracy was ±0.5°C (3σ, 12 devices). This improved to ±0.2°C (3σ, 16 devices) after trimming at 30°C (Fig. 17.3.5). These results demonstrate that accurate low-power low-voltage temperature sensors can still be designed in deep-submicron CMOS processes.

Acknowledgments:
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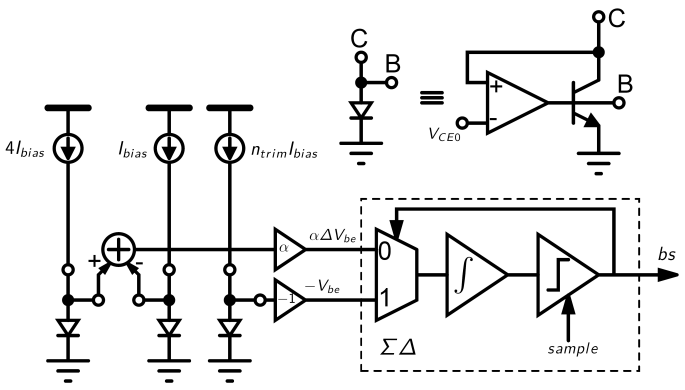

Figure 17.3.1: Principle of operation of the NPN-based temperature sensor.

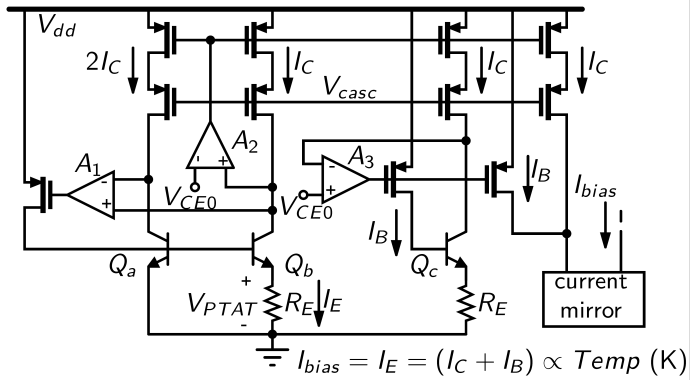

Figure 17.3.2: Simplified circuit diagram of the bias circuit generating I_{PTAT}.

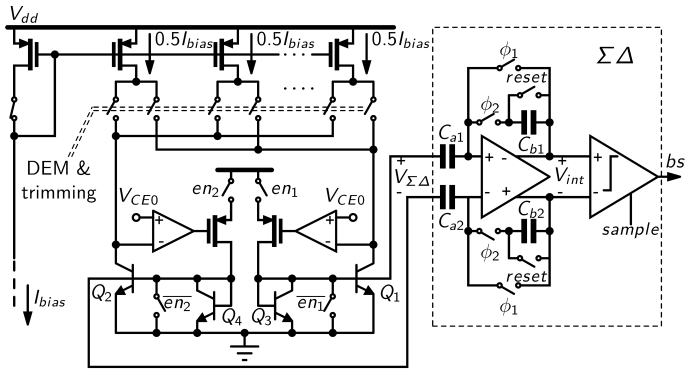

Figure 17.3.3: Simplified circuit diagram of the bipolar front-end circuit and the 1st order ΣΔ modulator; the switches in the current mirrors are implemented with cascode transistors.

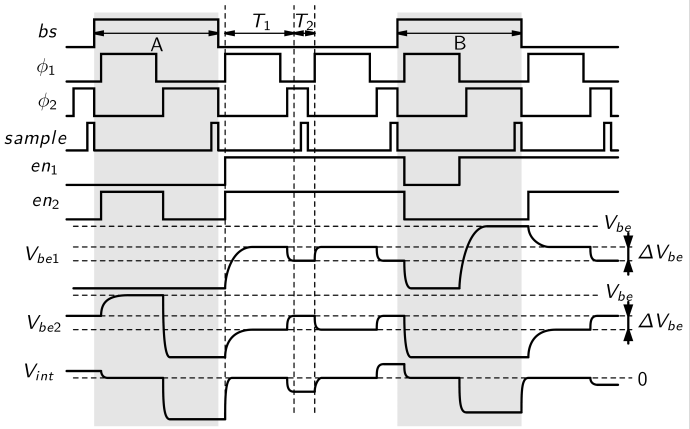

Figure 17.3.4: Timing diagram and waveforms of a fragment of the temperature conversion; periods when *bs*=1 are shown in gray (A and B).

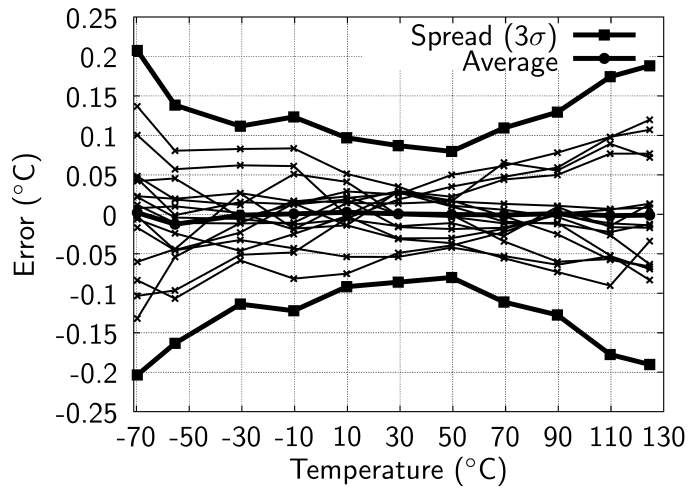

Figure 17.3.5: Measured temperature error (with ±3σ limits) of 16 samples after trimming at 30°C.

Reference	This work	[2]	[4]
Technology	65nm CMOS	32nm CMOS	0.7μm CMOS
Chip area	0.1mm^2	0.02mm^2	4.5mm^2
Supply current	8.3μA	1.5mA	25μA
Supply voltage	1.2 - 1.3V	1.05V	2.5 - 5.5V
Supply sensitivity	0.9/-1.2°C/V	N.A.	0.05°C/V
Output rate	2.2Sa/s	1kSa/s	10Sa/s
Resolution	0.03°C	0.15°C (1σ)	0.025°C (1σ)
Temperature range	-70°C - 125°C	-10°C - 110°C	-55°C - 125°C
Inaccuracy (untrimmed)	0.5°C (3σ)	<5°C	0.25°C (3σ)
Inaccuracy (trimmed)	0.2°C (3σ)	N.A.	0.1°C (3σ)

Figure 17.3.6: Performance summary of this work in comparison with [2] and [4].

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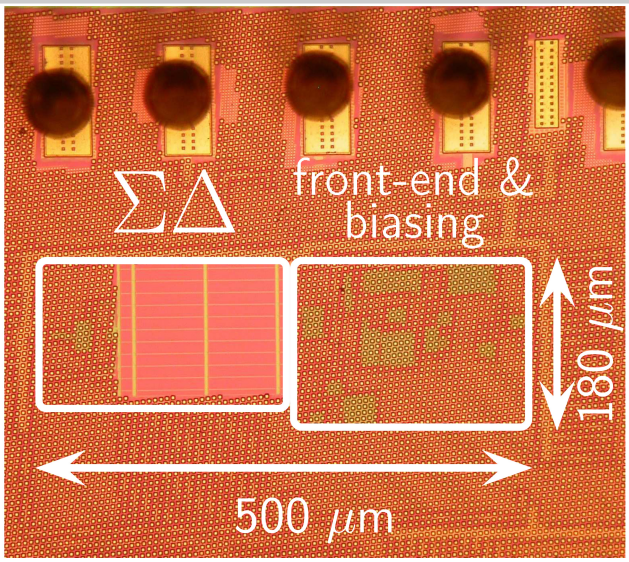

Figure 17.3.7: Chip micrograph.

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