

Effects of Packaging and Process Spread on a Mobility-Based Frequency Reference in 0.16- μm CMOS

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Abstract— In this paper, we explore the robustness of frequency references based on the electron mobility in a MOS transistor by implementing them with both thin-oxide and thick-oxide MOS transistors in a 0.16- μm CMOS process, and by testing samples packaged in both ceramic and plastic packages. The proposed low-voltage low-power circuit requires no off-chip components, making it suitable for applications requiring fully integrated solutions, such as Wireless Sensor Networks. Over the temperature range from $-55\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$, its frequency spread is less than $\pm 1\%$ (3σ) after a one-point trim. Fabricated in a baseline 0.16- μm CMOS process, the 50 kHz frequency reference occupies 0.06 mm^2 and, at room temperature, its consumption with a 1.2-V supply is less than $17\text{ }\mu\text{W}$.

I. INTRODUCTION

The mobility of charge in a MOS transistor has proved to be a good reference for fully integrated oscillators. Mobility-based frequency references with an inaccuracy of only a few percent can be implemented with compact low-power low-voltage circuits [1]. In the presence of cost and size constraints, such references can be used in place of traditional crystal-controlled oscillators (XCOs). For example, in a time reference that synchronizes the nodes of a Wireless Sensor Network (WSN), turning them on only when communication takes place, and thus lowering their power consumption. Although XCOs would provide inaccuracies of only a few ppm, in this application a less accurate but fully integrated reference is preferred since it reduces the cost and size of the node [2].

Charge mobility exhibits a process spread of a few percent and a large temperature dependence (approximately proportional to $T^{-1.8}$, where T is the absolute temperature). For a given process, this dependence is well defined and can thus be compensated for, while the effect of process spread can be removed by a single-point trim at room temperature. Using the I/O thick-oxide transistors of a 65-nm CMOS process, mobility-based frequency references with an inaccuracy of less than 2.7% have been achieved over the temperature range from $-55\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$ for samples in ceramic packages [1]. However, plastic packages are usually preferred in cost-constrained applications such as WSN. The mechanical stress induced by the plastic molding will cause variation in the mobility, and lead to a loss of accuracy [3]–[5]. The choice of process and the specific options used will also cause

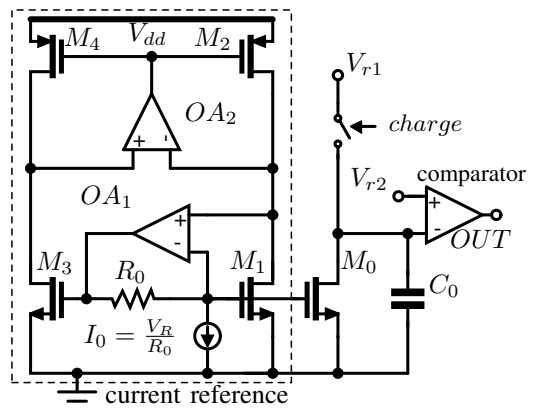


Fig. 1. Simplified schematic of the mobility-referenced oscillator from [1].

variations in the mobility. However, no data is available about the robustness of mobility-based references to process or to plastic packaging.

In this paper, we explore the robustness of mobility-based references by implementing them with both thin-oxide and thick-oxide MOS transistors in a 0.16- μm CMOS process, and by testing samples packaged in both ceramic and plastic packages. Compared to implementation in deep-submicron technology, the use of more mature technology can drastically reduce costs. Moreover, the gate leakage of thin-oxide transistors in deep-submicron technology reduces the accuracy of ultra-low-power circuitry, whereas it is negligible for both the thin and thick-oxide transistors in the chosen 0.16- μm process, thus allowing both options to be explored in the same process. Measurements show that, after a single-point trim, the frequency spread achieved by using thin-oxide transistors is less than $\pm 1\%$ over the military temperature range, a 2.7x improvement on [1]. The circuit is presented in section II; the spread expected after a single-point trim is analyzed in section III; experimental results are shown in section IV and conclusions are drawn in section V.

II. CIRCUIT DESCRIPTION

The operating principle of the mobility-based frequency reference is shown in Fig. 1 [1]. It consists of a low-

voltage current mirror (formed by $M_{2,4}$ and OA_2) with gain $n = \frac{W_4/L_4}{W_2/L_2}$ and the NMOS pair $M_{1,3}$. Opamp OA_1 defines the voltage difference $V_R = R_0 \cdot I_0$ between the gates of M_1 and M_3 . Using the square-law MOS model, the drain current of M_1 can then be written as

$$I_1 = \frac{\mu_n C_{ox} W_1}{2} \frac{V_R^2}{L_1 \left(\sqrt{\frac{n}{m}} - 1\right)^2} \quad (1)$$

where $m = \frac{W_3/L_3}{W_1/L_1}$, C_{ox} is the oxide capacitance per unit area and μ_n is the electron mobility [1].

The drain current of M_1 is mirrored by M_0 and applied to a relaxation oscillator, in which C_0 is periodically charged to V_{r1} and then discharged to V_{r2} . From (1), the oscillation frequency is

$$f_{osc} = k \frac{\mu_n C_{ox} W_1}{2C_0 \left(\sqrt{\frac{n}{m}} - 1\right)^2} \frac{V_R^2}{L_1 V_{r1} - V_{r2}} \quad (2)$$

where $k = \frac{W_0/L_0}{W_1/L_1} = 4$ and C_0 is a MOS capacitance matched to M_1 so that $C_0 \propto C_{ox}$. If V_R , V_{r1} and V_{r2} are temperature-independent reference voltages, then f_{osc} will have the same temperature dependence as μ_n .

The complete schematic of the current reference is shown in Fig. 2. Unlike [1], the current source I_0 is realized on-chip by the bias circuit in the dashed box. This consists of thin-oxide transistors and is supplied by $V_{dd2} = 1.8$ V. With the switches configured as shown in the figure, the opamp forces the voltage V_R across $R_1 = R_2 = 750$ k Ω to generate $I_0 = V_R/R_1$. This current is copied by current mirrors $M_7 - M_8$ and $M_5 - M_6$ and by flowing through R_2 generates a voltage difference between the gates of M_1 and M_3 equal to $R_2 I_0 = \frac{R_2}{R_1} V_R$. The mismatch of the resistors and the current mirrors together with the offset of the opamp introduces errors in V_R and consequently an error Δf in the output frequency. By periodically toggling the position of

the switches and chopping the opamp, this mismatch-induced frequency error can be averaged out.

The start-up circuit and the opamps are shown in the dashed boxes in the figure. Since OA_1 must provide an output quiescent current I_0 , it is biased with $I_{13} = I_0/2$ and is dimensioned such that $\frac{W_{10}}{L_{10}} = \frac{W_9}{L_9}$ and $5 \frac{W_{11}}{L_{11}} = \frac{W_{12}}{L_{12}}$. The MOS capacitor C_{c1} and the fringe metal capacitor C_{c2} are compensation capacitors for the feedback loops involving, respectively, OA_1 and OA_2 .

III. RESIDUAL SPREAD AFTER TRIMMING

By using the precision bias circuit described above, the spread of the reference's output frequency should only be dominated by the spread of mobility. Charge mobility is usually modeled as

$$\mu_n(T) = \mu_0 \left(\frac{T}{T_0}\right)^\alpha \quad (3)$$

where μ_0 is the mobility at room temperature T_0 and α typically varies from -1.2 to -2 [6]. Assuming that the output frequency is proportional to the mobility, the uncompensated and untrimmed frequency is given by

$$f(T) = k \cdot (\mu_0 + \Delta\mu_0) \left(\frac{T}{T_0}\right)^{\alpha + \Delta\alpha} \quad (4)$$

where k is a proportionality constant and $\Delta\mu_0$ and $\Delta\alpha$ are variations due to the process spread. The nominal output frequency is simply

$$f_0(T) = k \cdot \mu_0 \left(\frac{T}{T_0}\right)^\alpha \quad (5)$$

The effect of trimming at temperature T_0 can be modelled by dividing $f(T)$ by the dimensionless factor $f(T_0)/f_0(T_0)$. Similarly the effect of temperature compensation can be modelled

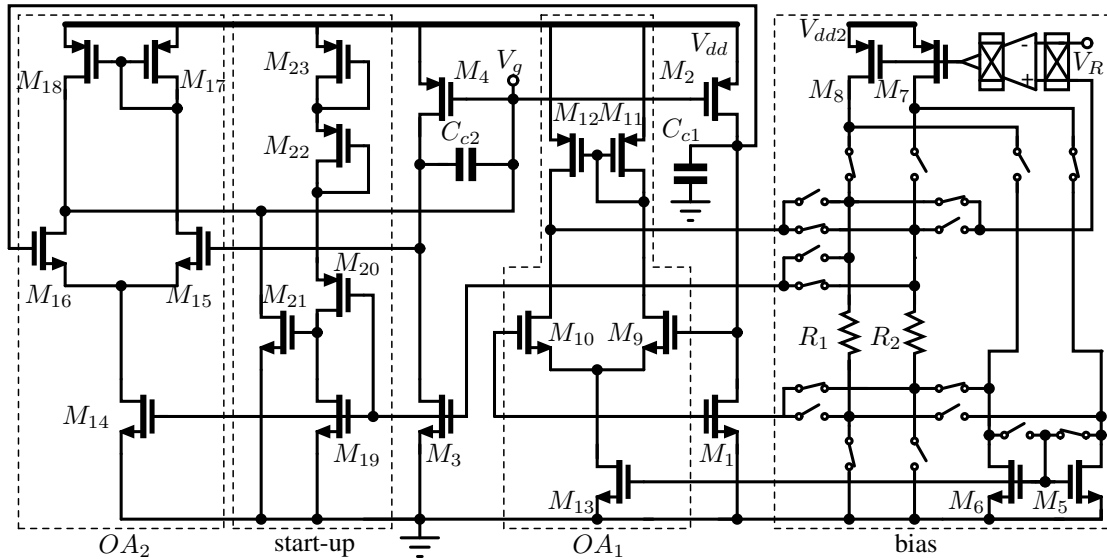


Fig. 2. Complete schematic of the current reference; the cascode transistors in series with $M_5 - M_8$ are omitted for clarity.

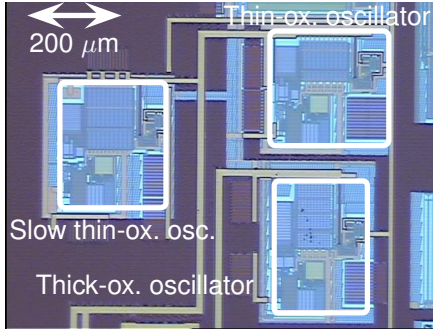


Fig. 3. Die micrograph of the test chip.

by dividing $f(T)$ by $f_0(T)/f_0(T_0)$. The result is a trimmed and temperature-compensated output frequency given by

$$f_{comp}(T) = k \cdot \mu_0 \left(\frac{T}{T_0} \right)^{\Delta\alpha} \quad (6)$$

Since $\Delta\mu_0$ is eliminated by trimming, it is $\Delta\alpha$ that determines the frequency spread. As shown below, the relative error of the compensated frequency should then have a logarithmic dependence on absolute temperature:

$$\frac{f_{comp}(T) - f_0(T_0)}{f_0(T_0)} \approx \frac{\Delta\alpha}{f_0(T_0)} \left. \frac{\partial f_{comp}}{\partial \Delta\alpha} \right|_{\Delta\alpha=0} = \Delta\alpha \log \left(\frac{T}{T_0} \right) \quad (7)$$

IV. EXPERIMENTAL RESULTS

The mobility reference was implemented in a baseline SSMC 0.16- μm CMOS process. In order to test the robustness of the mobility-based reference to process options, two versions were made, one in which the current reference (Fig. 2) and MOS capacitor C_0 in Fig. 1 were implemented with thin-oxide and one in which thick-oxide transistors were used. To minimize the effect of the comparator's non-idealities, the differential oscillator topology of [1] (with two equal capacitors C_0) was adopted for both references instead of the single-ended topology shown in Fig. 1. Since the comparator's delay may limit the reference's accuracy at high output frequencies, a third "slow" thin-oxide reference was implemented with 3x larger oscillator capacitors. The thin-oxide, thick-oxide and slow thin-oxide references each occupy 0.06 mm^2 (Fig. 3) and their current consumption at room temperature is, respectively, $11.8 \mu\text{A}$, $12.4 \mu\text{A}$ and $10.9 \mu\text{A}$ from a 1.2-V supply (V_{dd}) and $2.1 \mu\text{A}$ from a 1.8-V supply (V_{dd2}). All reference voltages (V_{r1} , V_{r2} , V_R) were generated externally. The samples have been packaged both in stress-free ceramic packages and in standard plastic packages without any stress-relieving coating.

The average output frequency of the various frequency references is shown in Fig. 4. At room temperature, the reference current is $I_1 = 200 \text{ nA}$ ($V_R = 0.275 \text{ V}$) for the thin-oxide reference and $I_1 = 200 \text{ nA}$ ($V_R = 0.225 \text{ V}$) for the thick oxide reference. For both references, $C_0 \approx 7 \text{ pF}$, $V_{r1} = 1.2 \text{ V}$ and $V_{r2} = 0.8 \text{ V}$. These reference voltages were used for all the reported measurements. The thin-oxide and

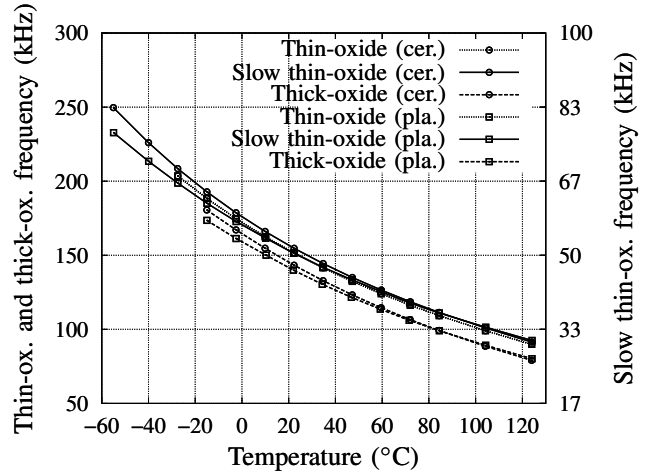


Fig. 4. Output frequency of the frequency references.

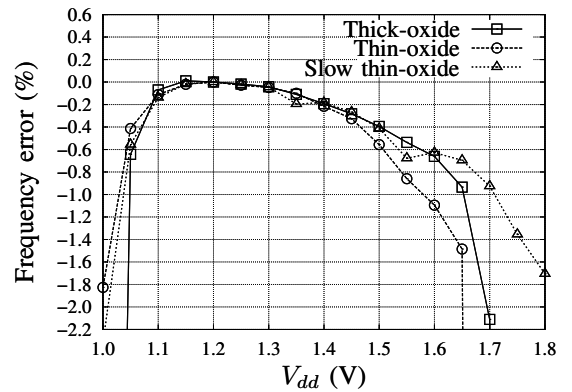


Fig. 5. Frequency error vs. variation of the supply voltage.

thick-oxide references only operate correctly over a limited temperature range, because the comparator's delay becomes significant for frequencies above 200 kHz and because the transistor's threshold voltage approaches the supply voltage at low temperatures. The measurements shows that the parameter α in (5) is approximately equal to -1.7 and -1.9 for the thin-oxide and the thick-oxide references, respectively.

Frequency pushing is illustrated in Fig.5 and is less than 1.3%/V up to 1.5 V. Although the nominal supply voltage is 1.8 V for the thin-oxide transistors and 3.3 V for the thick-oxide ones, the chosen circuit topologies allow functionality down to 1.05 V. The period jitter is $29 \text{ ns}_{\text{rms}}$, $34 \text{ ns}_{\text{rms}}$ and $62 \text{ ns}_{\text{rms}}$ for the thin-oxide, thick-oxide and slow thin-oxide reference, respectively.

Measurements were made on 12 samples in ceramic packages and 12 samples in plastic packages from one batch. Over the military temperature range, the lowest frequency spread of 1% (3σ) was achieved by the "slow" thin-oxide reference in ceramic packaging (Fig. 6). To easily compare the different results, the spread model of (7) has been least-square fitted to the observed 3σ -spread. Good agreement is observed between the model of (7) and the experimental data. The resulting 3σ

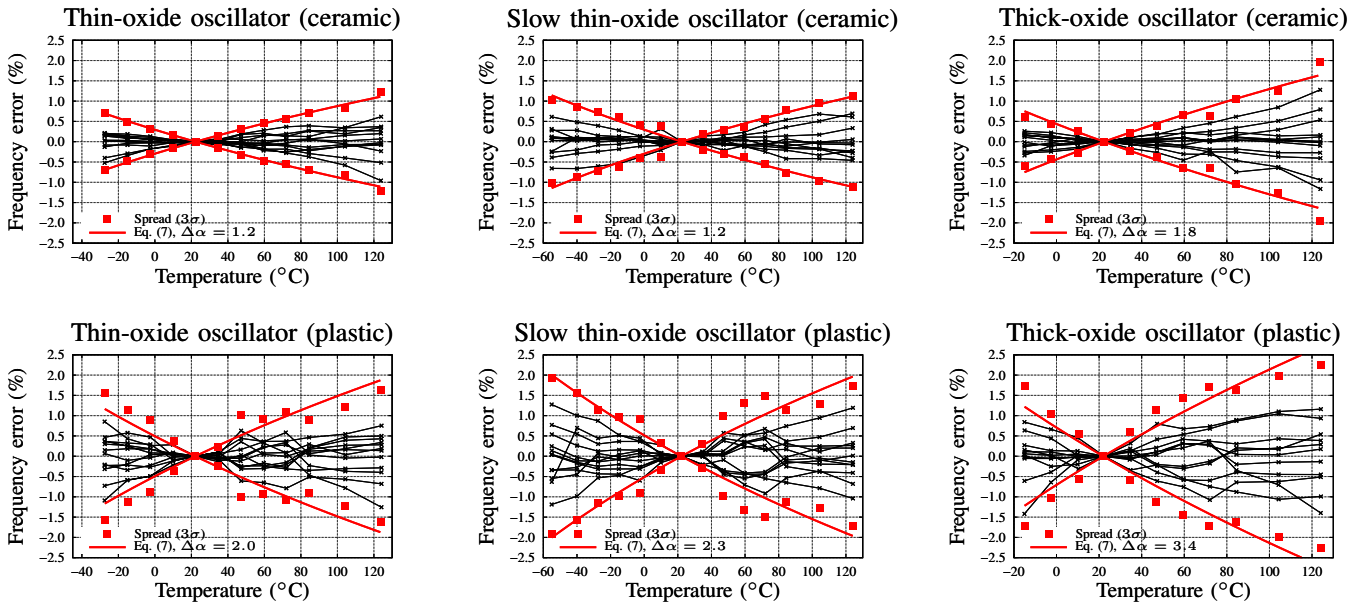


Fig. 6. Frequency error with respect to the average frequency vs. temperature after one-point trimming at room temperature for 12 samples (11 samples tested for the ceramic-packaged slow thin-oxide oscillator).

values for $\Delta\alpha$ are reported in Fig. 6. While similar results were achieved by both thin-oxide references (as expected since they contain the same current reference), the spread of the thick-oxide reference is approximately 50% larger. Even with the limited number of available samples, the use of plastic packaging clearly results in more spread (about 2x more) than the use of ceramic packaging.

The frequency reference's performance is summarized in Table I and compared to other low-power fully integrated CMOS frequency reference for which statistical data was available, i.e. with measurements from more than one sample. Together with the results of [1], this work demonstrates that mobility-based reference can be successfully implemented in different processes, and that, even over a wider temperature range, their accuracy is comparable to the state-of-the-art.

V. CONCLUSIONS

It has been shown that mobility-based frequency references can be implemented in different processes and with different

packaging. In a given process, their accuracy will depend both on the devices used and on the selected packaging. By using thin-oxide transistors and ceramic packaging, inaccuracies as low as 1% over the military temperature range can be achieved. Even when accuracy must be sacrificed for the sake of cost, and thus low-cost plastic packages are used, the resulting inaccuracy can be kept below 2% over the same temperature range. This demonstrates the robustness of the proposed reference and their potential for low-cost application in low-power low-voltage integrated systems.

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON.

Reference	[7]	[1]	This work	
Frequency	6 MHz	150 kHz	50 kHz	140 kHz
Supply	1.2 V	1.2 V	1.2 V	1.2 V
Power	66 μ W	51 μ W	17 μ W	19 μ W
Technology	65 nm	65 nm	0.16 μ m	
Oxide	-	thin	thin	thick
Temp. range (°C)	0~120	-55~125	-55~125	-15~125
Inaccuracy	$\pm 0.9\%$	$\pm 2.7\%$	$\pm 1\%$ (3σ)	$\pm 2\%$ (3σ)
Samples tested over temp.	4	12	11	12