11.6 A 2.4GHz 830pJ/bit Duty-Cycled Wake-Up Receiver with -82dBm Sensitivity for Crystal-Less Wireless Sensor Nodes

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This paper describes a 2.4GHz Wake-up Receiver (WuRx) designed to operate with low-accuracy (<0.5%) frequency references [1], enabling crystal-less and thus low-cost wireless sensor nodes (WSNs). Robustness to frequency error is achieved by combining non-coherent energy detection with a broadband-IF superheterodyne architecture, and by using a pulse-position-modulated (PPM) impulse radio (IR) modulation scheme [2]. The Rx front-end and the LO generator are duty-cycled at pulse level, thereby reducing the power consumption to less than 420μW, which is more than adequate for use in WSNs [2]. PPM-IR also enables the realization of an interferer-robust receiver without the use of bulky off-chip RF filters [3,4]. This 65nm CMOS fully integrated WuRx employs a duty-cycled LO generator and achieves a sensitivity of -82dBm at a data rate of 500kb/s with an energy efficiency of 830pJ/bit.

Figure 11.6.1 shows the frequency plan of the proposed WuRx. The PPM-IR RF input signal has a nominal center frequency of 2.44GHz and is down-converted to IF by a 2.39GHz LO. Since the LO frequency is derived from a frequency reference with an inaccuracy of <0.5%, the actual LO frequency will lie between 2.38GHz and 2.40GHz. The transmitted signal from a similar WSN will also have a 0.5% frequency error and so the IF signal will lie somewhere between 26MHz and 74MHz. Signals in this IF band are amplified and then downconverted to baseband by a full-wave rectifier. The use of a broadband IF amplifier and the non-coherent energy detection of the incoming RF pulses, make it possible to tolerate the IF uncertainty. The extra gain needed for efficient energy detection can be provided at IF with greater power savings and higher sensitivity than RF diode detectors [4,5]. However, heterodyne architectures typically require the generation of a high-frequency LO, dominating their power budget [6]. Alternatively, a periodically calibrated free-running digitally-controlled oscillator (DCO) can be used [3]. However, temperature and supply voltage variations may cause unpredictable frequency drift. Here, the DCO is embedded in a duty-cycled PLL (DCPLL) to overcome these issues [7]. The closed-loop nature of the DCPLL prevents frequency drift, while power efficiency is achieved by burst-mode operation.

Figure 11.6.2 depicts the block diagram of the WuRx comprising an Rx chain and a DCPLL-based LO generator. The differential RF input signal is PPM at 500kb/s with a pulse width of 80ns and a center frequency of 2.44GHz. A finite-state machine (FSM) driven by a 10MHz reference clock (with an inaccuracy of <0.5%) duty cycles the DCO, the mixer and the IF amplifier. The DCO only operates during one reference clock cycle, i.e. 100ns, and is in sleep mode for the next nine, i.e. 900ns. This translates into a 10% duty-cycled DCPLL with the 1MHz pulse repetition rate required to downconvert and detect the pulse positions of the input signal. In the receiver, this duty cycling translates into significant power savings. As in [7], the DCO consists of a current-controlled differential delay line in a closed loop. To minimize its startup time, the DCO is turned on by means of MOS switches, which configure the delay line as a ring oscillator [7]. The output frequency is controlled by means of a 16-bit DAC: 7 bits are used for coarse frequency acquisition and 9 bits for fine tuning. The counter counts the number of rising edges that occur during the 100ns reference cycle, while the phase detector (PD) together with coarse and fine tuning blocks ensures that this number equals the frequency-control word (FCW).

An integrated passive LC resonator at the antenna attenuates out-of-band interferers (Fig. 11.6.2). The DCPLL's 2.39GHz quadrature outputs drive the mixer, which performs the downconversion to IF. Broadband amplification is performed by the IF amplifier, while an IF polyphase filter introduces two notches that suppress interferers at image frequencies. A differential-input full-wave rectifier detects the energy content of the incoming pulses. An off-chip demodulator then

converts the baseband output into a digital bitstream. To save power, the FSM also controls the activity of the mixer and the IF amplifier. Both are enabled 20ns before the DCO to take their own start-up time into account. A preamble precedes each wake-up request packet and is used by an off-chip digital synchronizer and a DLL to estimate and compensate for the time offset between Tx and Rx.

Figure 11.6.3 shows a simplified schematic of the WuRx front-end and IF sections. The input matching network (with an on-chip inductor) realizes the front-end filter and is connected directly to a double-balanced quadrature Gilbert mixer, avoiding the use of an LNA. The IF amplifier comprises two chains of 5 differential-pair gain stages and a passive 2nd-order polyphase filter. Alternate stages are implemented with a split-source topology to minimize their offset voltage. The IF section introduces 3 zeros at DC, two notches at the negative image frequencies and provides 40dB voltage gain in the desired band. Each stage provides 8dB gain and the overall noise performance was optimized by appropriately scaling the current through each stage. To simplify biasing, the mixer and the IF amplifier use resistive loads.

The 0.2 mm² WuRx was fabricated in a baseline 65nm CMOS process (Fig. 11.6.7). The measured front-end conversion gain is 61dB. The normalized gain response is shown in Fig. 11.6.4 along with the measured $|S_{11}|$, which is lower than -15dB in the 2.4GHz ISM band. The RF-referred notches are at 2.3GHz and 2.36GHz, while the IF amplifier notch is visible at the LO frequency of 2.39GHz. This gain response enhances the receiver's interferer tolerance. The DCO's instantaneous frequency has an average value of 2.39GHz within one 100ns cycle of the 10MHz reference (Fig. 11.6.4). Figure 11.6.5 shows the measured BER of the receiver for different data rates and different reference clock accuracies. For a ±0.5% error in the reference frequency and in the frequency of the received RF signal, the sensitivity for 10⁻³ BER is better than -72 dBm at 500Kb/s. Under nominal conditions, the sensitivity reaches -82dBm at 500kb/s and -87dBm at 250kb/s for 10⁻³ BER. When duty cycled, the 2.39 GHz DCO draws 166μA, the mixer, IF amplifier, and envelope detector consume 166μA, while the DCPLL's logic uses 14μA, leading to a total current of 346μA from the 1.2V supply. This corresponds to 830pJ/bit at 500Kb/s. In Fig. 11.6.6, the WuRx's performance is summarized and compared with other work.

This fully integrated WuRx combines PPM-IR modulation with a duty-cycled DCPLL-based broadband architecture. It demonstrates that wakeup receivers can achieve sensitivities as high as -82dBm while only dissipating 830pJ/bit.

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Figure 11.6.1: Method of operation and frequency plan.

Figure 11.6.2: Block diagram of the Wake-up Receiver.

Figure 11.6.3: Simplified schematic of RF front-end and IF section.

Figure 11.6.4: Measured S11 magnitude, normalized conversion gain and DCO's instantaneous frequency.

Figure 11.6.5: Measured BER for different frequency errors and data rates.

	This work	[3]	[5]	[4]
Receiver				
Power Consumption	415uW	52uW	8mW	64uW
Sensitivity@10 ⁻³ BER	-87dBm	-82dBm	-72dBm	-48dBm
Datarate	250kbps	500kbps	100 kbps	16Mbps
Energy efficiency (including LO generation)	830pJ/bit	520 pJ/bit	500pJ/bit	650pJ/bit
Required External components	None	MEMS XTAL for calibration	None	BAW
LO generation				
Techniques used	Duty Cycled PLL	Free running DCO periodically calibrated	Self Mixing RF-Diode	Self Mixing RF-Diode

Figure 11.6.6: Receiver performance and comparison with previous work.

Figure 11.6.7: Chip micrograph.