A 43 GHz 1-V VCO In Standard CMOS With High Output Drive Capability.

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Abstract— **In this paper, we present a 43 GHz VCO in 0.13μm CMOS for use in SONET OC-768 optical networks. The design [1] has a large tune range of 4.2 %, which is sufficient to hold the design center frequency over anticipated process spread and temperature variation. A tuned output buffer is used to provide 1.3 V_{p-p} (single-ended) into a 90 fF capacitive load as is required when the VCO is used in typical clock and data recovery (CDR) circuits. Phase noise is -90 dBc/Hz at a 1 MHz offset from the carrier; this meets SONET jitter specifications. The VCO, including output buffers, consumes 14 mA from a 1 V supply and occupies 0.06 mm^2 of die area.**

Keywords— **SONET, Optical Networks, OC-768, Clock and Data Recovery, VCO, Oscillator, CMOS.**

I. MOTIVATION

At present, circuits for 40 GB/s optical communication networks are commonly made using III-V compounds or in SiGe processes [2]. With the advent of smaller and faster CMOS technology, it has become possible to make such circuits in standard CMOS, leading to lower-cost solutions and opening the way to increased integration. One of the principal functions that is required in optical networks is that of clock and data recovery (CDR). For this, a VCO is a central building block. Several authors have presented 40+ GHz VCO's in CMOS [3], [4], but application of a VCO to a real CDR circuit requires that the tune range be sufficient to cover the anticipated variation in center frequency due to process spread and temperature variation. Additionally, the VCO should be capable of driving a capacitive load with a large voltage swing. As will be shown, these requirements present challenges in terms of phase noise. An architecture with a tuned output buffer is shown to satisfy all requirements simultaneously. The resulting design is low-power (14 mW), low voltage (1V) and occupies a very small die area (0.06 mm^2).

II. SPECIFICATIONS

A. Jitter requirements

In OC-768 optical networks, the specified bitrate is 39.81 GHz. 8% Forward Error Correction (FEC) is commonly used; this makes for a 'raw' bitrate of 43 GHz, which is the design center frequency of this VCO. A single bit-time (commonly referred to as a Unit Interval or UI) at this data rate is 23.2 ps.

ITU requirements [5] specify the maximum allowable jitter whereas for VCO's, the measured quantity is the phase noise spectrum. Conversion between jitter and phase noise is straightforward:

$$\Delta\phi_{RMS}^2 = \int_{band} 2 \cdot L(f)df \qquad (1)$$

where $L(f)$ is the phase noise spectrum, *band* is the offset frequency band of interest and $\Delta\phi_{RMS}$ is the RMS jitter in radians.

ITU requirements state that jitter in a band from 16 MHz to 320 MHz should not be more than 0.1 UI_{p-p}. This requirement does not translate directly to VCO specifications: it dictates the behaviour of the whole CDR subsystem and it is up to the designer of the subsystem to divide the jitter 'budget' in an optimal fashion.

A realistic assumption might be that the VCO should not contribute more than 25% of the allowable CDR jitter at high offset frequencies, to ease the design of the other parts of the CDR circuit. At low offset frequencies, jitter of the VCO is effectively suppressed by the PLL of which the VCO is part.

The phase noise of the VCO can be integrated to lead to an RMS jitter value. For simplicity, a constant slope of the phase noise spectrum is assumed; this slope is chosen so that the resulting jitter estimate is always higher than the actual jitter, thus ensuring achieval of the design goal. If 25 % of the jitter budget is expended on the VCO and L(1 MHz) is lower than -87 dBc/Hz then the VCO is suitable for use in a SONET OC-768 CDR system.

B. *Output drive requirements*

To usefully drive digital logic, the VCO should be capable of driving a large capacitive load with a large voltage swing. The exact requirement will of course depend on the CDR circuit being driven, and in this respect VCO design cannot be considered in isolation. Preliminary investigation reveals that a realistic, useful output is if 90fF (representing the input capacitance of two 36/0.13 n-channel MOSFETs) can be driven by the VCO with more than 0.6 V_{p-p} (single-ended) over all anticipated temperature variations and process spread. These drive requirements mandate the use of a buffer stage between VCO and the load.

For the most common full-rate CDR architectures, two active clock flanks are required per UI. This means that at 43 GB/s, we need a 43 GHz differential clock source or a 21.5 GHz quadrature clock source. Additional constraints such as power and area will decide which of these two is chosen. A 43 GHz differential clock is promising for its small die area and relative simplicity; quadrature generation is not required. Half-rate CDR systems (see, for example [7]) halve the clock frequency requirement at the expense of slower locking performance.

III. Oscillator Architecture & Design

A. *Architecture*

The high center frequency, fixed frequency application and low phase noise requirements point to an LC-type oscillator. At 40 GHz a benefit is that the required inductors are small so this oft-cited disadvantage of integrated LC-oscillators does not apply. Many fully integrated LC oscillators at lower frequencies have been presented, and much design effort has been put into the design of a high-Q inductor. For a given power consumption, low phase noise dictates the use of a high-Q tank. For the LC-tank,

$$\frac{1}{Q_{tank}} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{2}$$

Where Q_{tank}, Q_L and Q_C are the quality factors of the tank and the inductor and capacitor that make up the tank, respectively. When Q_L is much lower than Q_C as is commonly the case for integrated LC-tanks at frequencies up to a few GHz, improving Q_L directly leads to a higher tank Q and hence to lower phase noise at given power [8]. With the advent of modern CMOS processes, with copper metallization and 7 or 8 metal layers (increasing the separation between the inductor and the lossy substrate), Q_C at 40 GHz is significantly lower than Q_L and improving the latter is no longer necessary. Rather, design effort needs to be put into making Q_C as high as possible.

For the parallel combination of several C_n's each with a Q_n, making up a single C, the following holds for Q_C of the parallel combination:

$$\frac{1}{Q_C} = \sum_n \frac{1}{Q_n \cdot (\frac{C}{C_n})} \tag{3}$$

This means that to maximize Q_C, the relative size of the low-Q capacitors must be minimized. Unfortunately, parasitics have a low Q and they comprise a significant portion of the tank C at 40 GHz. This also clarifies why driving the gate of the load MOSFET directly with the VCO core is not a practical proposition. The input capacitance of a MOSFET is lossy (low Q) due to the gate series resistance, and driving the load directly with the VCO tank would unacceptably lower tank Q. Secondly, this would make the load C a significant part of the tank C, and would mean that any variation in load (for example by varying wiring capacitance) would change the center frequency of the VCO.

B. *Design*

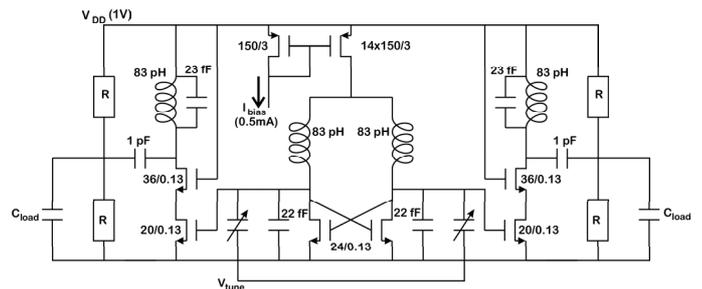The circuit diagram of the oscillator is shown in fig. 1.

Fig. 1. VCO with tuned output buffer

The central part of the tuned oscillator is the LC-tank. Since the oscillation frequency, ω_0,($= 1/\sqrt{LC}$) dictates the product of L and C, the only design freedom is in choosing the tank impedance Z_0:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{4}$$

Constraints such as startup gain and required amplitude of the oscillation voltage commonly dictate the choice of Z_0 [9], but here we have a more pressing requirement, namely to maximize tank Q. We expect Q_C to be low at 40 GHz and hence want to maximize it. Since a significant part of the tank C consists of parasitics (these have a low Q and sum to approximately 100 fF), the only way to increase the Q of the tank C is by adding as much as possible

high-Q MIM[1] capacitance, in accordance with eq. 3. The resulting tank capacitance of 150 fF has a Q of approximately 10. The tank impedance is thus made as low as possible, within, of course, other constraints such as startup conditions, power consumption, and tune range. For this design, Z_0 is 25 Ω.

The other important component of the tank is the inductor. The availability of copper metallization and operation at 40 GHz means it is not necessary to tie several metal layers together for a low series resistance. Hence, a single turn of metal on the top metal layer is used. Preliminary simulations quickly affirm the initial idea that inductor Q is very high at 40 GHz. This means extensive measures to maximize inductor Q are not required. It also allows us to change the shape of the inductor to suit layout requirements rather than using the common round or octagonal shapes that maximize Q. A long and thin rectangular shape is chosen because it allows very compact layout of the VCO (core and output buffer) and because it is easily scaled to other inductance values. The trace width is 5 μm; the inductor measures 15 x 100 μm. The inductor is simulated by electromagnetic simulation using IES[3] [6], and an equivalent circuit model is developed. It has an inductance of 93 pH and a Q of 35 at 40 GHz.

The VCO gain cell is equipped with NMOS transistors only since these have a higher f_t than PMOS transistors. The transistors used have a fingered structure with fingers of 2 μm width each. Tuning is done with a PMOS varactor that has two fingers of 0.4 x 2.4 μm each. The tune voltage range is continuous from 0 to 1 V. The oscillator is biased with a current source from the positive supply, this for better immunity to supply voltage variations, and to allow direct coupling to the output buffer stage.

The output buffer consists of an n-channel transistor with a tuned drain load for which the inductor layout is re-used. The tuned load enables us to achieve a peak-to-peak output voltage swing of 1.3 V (single-ended; typ.) into 90 fF, which is larger than the 1 V supply voltage. Both the in-phase and the antiphase output of the VCO achieve this swing. Since the peak output voltage of the buffer is higher than the supply voltage, a cascode transistor is included to prevent any detrimental effects on reliability. In this way, the only device junction subjected to more than the 1 V supply voltage is the drain-bulk junction of the cascode transistor. This does not pose reliability problems.

The output of the buffer is capacitively coupled to the load, and the DC level at the output is placed at half the supply voltage using a high impedant resistive divider. The

load still needs to be absorbed into the output buffer tank to bring it to resonance at the correct frequency, but this is no longer very critical, as the only thing influenced is the output amplitude, not the center frequency or the phase noise.

A startup gain of two is chosen to ensure reliable startup of the VCO. A lower startup gain may reduce parasitics, thereby improving Q_C and hence Q_{tank}, thus improving phase noise performance, but for the prototype robust startup behaviour was deemed preferable.

IV. EXPERIMENTAL RESULTS

For testing purposes, a special version of the VCO was made to drive 50 Ω[2]. It was processed in a 0.13 μm standard CMOS process with 1 poly and 8 metal layers. Metallization is copper, and the top metal layer is extra thick (3μm). The interconnect dielectric is 'low-k'; ϵ_r=3. The process features a MIM-capacitance between M7 and M8 that has a capacitance of approximately 1 fF/μm^2 and a low series resistance.

To drive 50 Ω, the VCO core is not changed, so representative measurements of the phase noise are possible. Output voltage is lower, and the purpose of the tuned output buffer is somewhat defeated when driving a low-impedant load. Nevertheless, this test version exhibits performance in excellent agreement with simulations, lending credence to the expectation that the original version will perform according to simulation results as well.

The VCO is tested by wafer probing. To reduce capacitive coupling to the substrate, the output bondpads consist of only the top three metal layers. The output is measured using an Agilent 8565 EC spectrum analyser. At 40 GHz, a double terminated line is preferred for connecting the VCO to the analyser, so a 50Ω resistor is included on the chip. This means that the output buffer sees 25Ω. The output power as a function of center frequency is shown in fig. 2. Simulated output power for this version is -15.5 dBm. Cable and connector loss are measured as 4.5 dB at 40 GHz, and probe/bondpad loss is estimated at 1 dB. Measured output power is therefore approximately 3 dB below simulated output power.

The tuning characteristic is shown in fig 3. Though the C-V curve of the varactor is nonlinear, the large voltage swing in the VCO core tends to linearize the tuning characteristic [10] and the resulting tuning curve is quite linear.

The noise sidebands are measured with the the spectrum analyser and observed in detail with the aid of a specialized program. The phase noise spectrum has a -30 dB/dec

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[1] MIM (Metal-Insulator-Metal) capacitance consists of a thin dielectric between metal layers 7 and 8 that has high Q and is well suited to RF applications.

[2] At the time of design, ITU specs were still for 7% FEC so the design center frequency of this version is 42.6 GHz rather than 43 GHz.
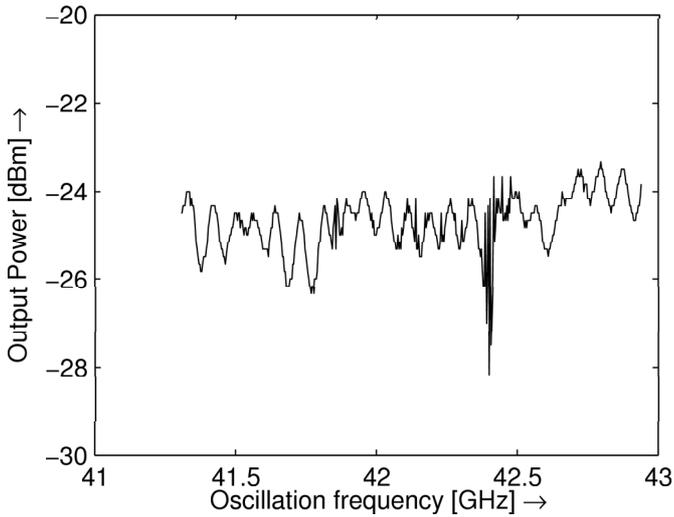
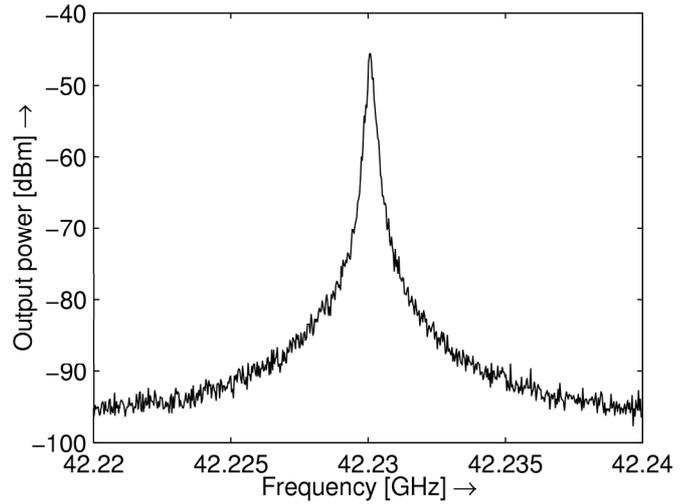Fig. 2. Output Power of the VCO

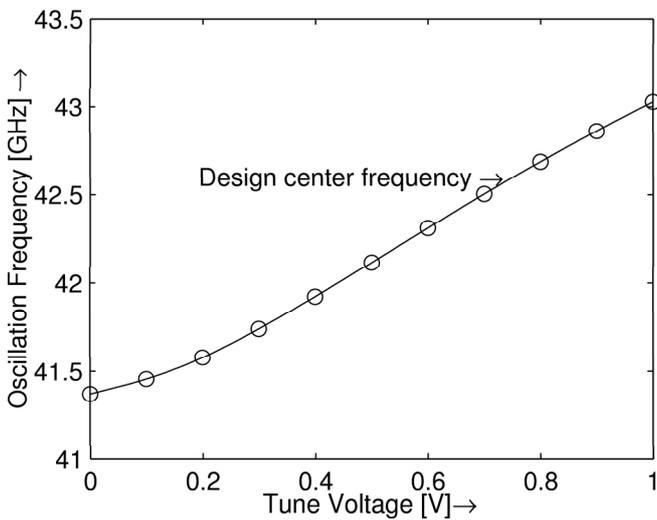
Fig. 4. Output spectrum of VCO (RBW=10 kHz)
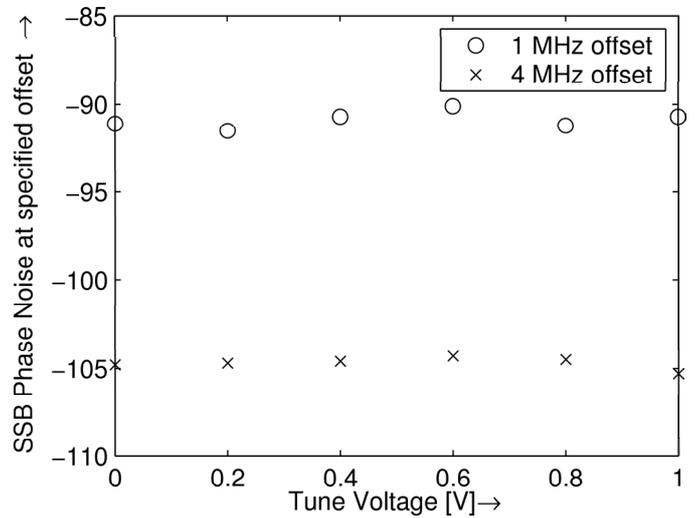

Fig. 3. Tune Range

Fig. 5. Phase noise performance

characteristic for offset frequencies up to 2 MHz, and a -20 dB/dec characteristic for larger offset frequencies. Figure 4 shows the oscillator output as observed on the spectrum analyer. This is measured with a very small resolution bandwidth so carrier power is not the same as in fig 2. Figure 5 shows the measured phase noise at a 1 MHz offset (in the -30 dB/dec range) and at a 4 MHz offset (in the -20 dB/dec range). As can be seen, the phase noise is essentially constant over the tune range. This is in close agreement with simulations.

A die photograph is shown in fig. 6. The distinctive inductor shape is clearly visible; twice at the top (the VCO core) and twice below that (the tuned output buffer).
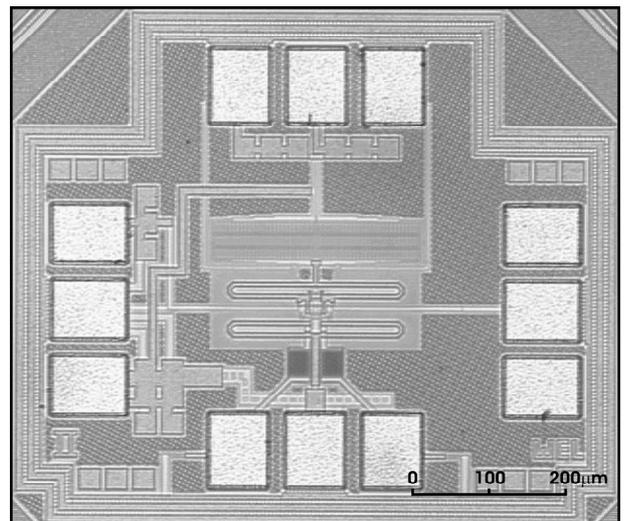

Fig. 6. Die Photo

V. Summary and conclusions

A 43 GHz LC-VCO in 0.13 μm standard CMOS is presented. The 43 GHz center frequency along with the properties of modern standard CMOS processes mean tank loss is determined predominantly by the the tank capacitance rather than the the tank inductance. Hence, rigorous maximization of inductor Q is not required and design effort is focused on maximizing capacitor Q. The VCO has a large tune range of 4.2%, and has both in-phase and antiphase outputs that each have a peak-to-peak output voltage swing larger than the supply voltage. The output voltage (1.3 V_{p-p} typ. in a 90 fF load) makes the VCO capable of driving high speed digital logic. Phase noise is -90 dBc/Hz at a 1 MHz offset; supply current is 14 mA from a 1 V supply, of which 7 mA is drawn by the VCO core. The VCO occupies 220 x 270 μm of die area. The low phase noise, large tuning range and high output drive capability make the VCO suitable for CDR circuits in OC-768 optical networks.

VI. Acknowledgements

VII. References

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