A High Voltage Swing 1.9 GHz PA in Standard CMOS

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Abstract—**A circuit technique for RF power amplifiers that reliably handle voltage peaks well above the nominal supply voltage is presented. To achieve this high-voltage tolerance the circuit implements switched-cascode transistors that yield reliable operation for voltages up to 7V at RF frequencies in a 2.5V CMOS process.**

Advantages of this include the possibility to use higher-ohmic load resistors. The impact of load resistances with higher ohmic values is two-fold. Firstly the demands on matching networks are loosened which translates into a higher efficiency for the matching network. Secondly the signal currents are lower which decreases the impact of any series resistance.

A design of a 1.9 GHz power amplifier using the switched cascode approach was made. Simulations on the extracted layout of a single ended side showed 21 dBm of output power at a 25 ohm load with 21 % PAE. A layout improvement was estimated to result in 22 dBm at 30 % PAE.

Keywords— **high voltage swing, power amplifier, switched cascode, CMOS RF**

I. Introduction

In the last few years there is an increasing demand for RF power amplifiers in CMOS; the main driving forces being the low cost aspect of CMOS and the possibility to integration of a whole RF transceiver in a single chip. For the integration of RF power amplifiers in standard CMOS some additional problems arise due to the low voltage handling capability of standard CMOS circuits. This paper, which is the result of a MSc assignment done at the University of Twente in cooperation with National Semiconductor, discusses some supply voltage related problems and presents a circuit solution. In the last section of this paper the simulated performance of the designed 1.9 GHz power amplifier, in a NSC 0.25 μm CMOS process, are summarized.

II. Supply Voltage Related CMOS Problems

The trend in CMOS to scale down the feature size of devices has a serious impact on the way to obtain high power levels for e.g. RF power amplifiers. To ensure sufficient lifetime of scaled-down transistors their nominal supply voltage as well as the maximum tolerable voltage across the transistors' terminals are decreased in proportion to the minimum feature size.

Two main reliability issues dictate the maximum tolerable voltages: hot carrier degradation and oxide breakdown. Hot carrier degradation depends among others on the length and biasing conditions of the device and mainly limits the drain source voltage that can be handled reliably. Gate oxide breaks down after some time if it is exposed to fields strengths over roughly 5.5MV/cm; corresponding to operation at voltages somewhat higher than the supply voltage. To form no reliability risk, the voltage difference across the transistors terminals should be limited to levels below roughly 2.75 V, the maximum supply voltage.

III. Output Power

The output power that can be delivered to a 50 Ω load is limited by the voltage swing that can be achieved within the reliability limitations. The peak voltage allowed at the drain of a common source PA is therefore equal to the maximum supply voltage of the used 0.25 μm CMOS technology: 2.75 V. This directly limits the ideal voltage swing to 2.75 Vpp and therefore the power that can be delivered to a fixed 50 Ω load. A few options are available to increase the output power.

A. Usage of a differential circuit.

In a differential circuit configuration the output signal equals the difference of both drain voltages, driven in anti-phase. This results in an ideal peak-peak signal that is two times as large as compared to the single ended case. If a 100 Ω differential load is used the output power has increased with a factor two. Because the DC power also increases with a factor two, the drain efficiency stays the same.

B. Use an impedance transformation network.

A common approach in PA design is to use a matching network between the PA output and the antenna load. This transformation network usually consists of passive components and transforms the 50 Ω antenna load to a lower value. With this lower load impedance, seen by the PA, the output power can be larger for the same power supply voltage.

Ideally the output power of the matching network equals the input power, but in practice it is lower due to the finite Q's of the passive components in the matching network. A small load impedance will result in higher currents if the voltage swing is kept constant. A disadvantage of this larger current is the fact that the transistor needs to be larger to sustain that current which in turn results in larger output capacitances. Another disadvantage is that the losses in the transformation network increases, causing a lower matching network efficiency.

C. Increase the output swing / supply voltage.

Another way of obtaining more output power is to increase the voltage swing that can be safely handled at the drain of a device. With circuits that can handle peak voltages above the nominal CMOS supply voltage, higher voltage swings in combination with a higher supply voltage can be used, thereby significantly increasing the maximum output power

There are three approaches that can be followed to handle voltages higher than the nominal supply voltage, while maintaining sufficient lifetime. Technological solutions use extra process steps and masks that deliver a high-voltage tolerant transistor at the cost of a more expensive process. Extended drain devices can be created in standard CMOS without the need for extra process steps but require special models and layout rules to be created [2]. Circuit solutions on the other hand limit the voltages across all transistor terminals to such values that sufficient lifetime is ensured and can be used within a standard CMOS process. This last option is used in this paper.

IV. "High" Voltage Circuits.

The general way to implement a high voltage circuit is to use one cascode transistor with an appropriate bias voltage. This bias voltage should be chosen such that the drain – source voltages of the transistors never exceeds the 2.75 V of the maximum supply voltage, which can be difficult to assure during a transient.

A dynamic bias voltage can be used to protect the cascode transistor if the output voltage of the amplifier comes above the nominal supply voltage. If at that moment the gate voltage of the transistor is increased, the output (drain) voltage may become higher before any transistor degradation or wear occurs. Timing of this dynamic bias voltage is difficult at RF frequencies: high stress would occur if the moment at which the gate voltage is raised, is delayed. Besides this, often a feedback loop is used and it can be difficult to prevent oscillations at RF frequencies. Using a fixed or dynamic bias voltage and a cascode configuration it is possible to handle voltages up to roughly 2 times the nominal supply voltage.

For higher output voltages a circuit solution can be used that implements switched cascode transistors. These switched casdode transistors are switched to either the supply voltage or to the output, as a diode, to limit the voltage [1]. With these extra transistors it is possible to handle output voltages higher than 2 times VDD while keeping the voltage across the transistor terminals below or equal to VDD.

V. SWITCHED CASCODE PRINCIPLE.

The implementation of the switched cascode approach in a general RF power amplifier configuration, results in the circuit as depicted in Figure 1. It uses two supply voltages: VDDnom which is equal to the standard CMOS supply voltage and VDDh which is a higher voltage, needed to allow a higher voltage swing at the output. BFL and BFC are a big fat choke and capacitor used for biasing and decoupling.

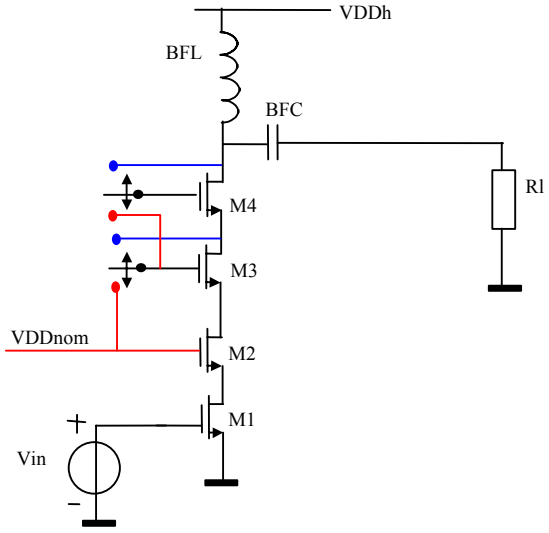

Figure 1 Switched cascode implementation in a PA.

M1 is the input common source transistor of the power amplifier and M2 is a standard cascode transistor. The mosfets M3 and M4 are switched cascode transistors that implement the high voltage protection. The gate of these transistors is switched by the symbolic switches to either VDDnom at low output voltages or to the drain, as a MOS diode, at high output voltages, that way decreasing the voltage to the point below with a gate source voltage.

The two extreme situations occur if the output voltage is very high or very low. In the situation where the output voltage is very high the two switched cascode transistors are connected like a diode and decrease the voltage that appears at the drain of M2 with two times Vgs, that way working like a high voltage protection. If the output is very low the gates of the two switched transistors are connected to VDDnom and M4 and M3 are in the (deep) triode region, limiting the voltage across them.

A simple implementation of the symbolic gate switches uses two pmos devices; Figure 2 shows the implementation for the situation with one switched cascode transistor.

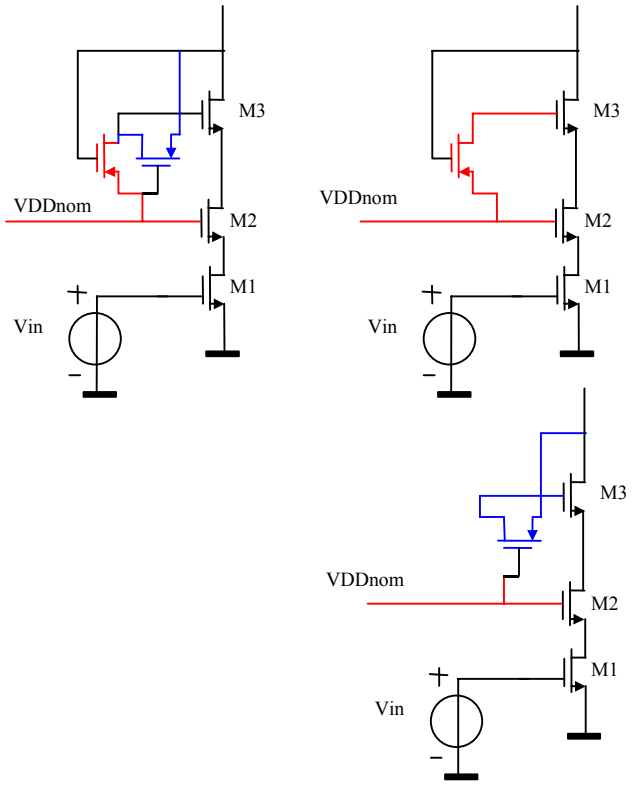

Figure 2 Switch implementation.

The switching moments depend on the level of the output voltage. If the drain of the switched cascode transistor is a Vth below VDDnom, the leftmost pmos transistor will conduct, shown in the upper right picture. The switch is in the down position with the gate of the switched cascode transistor connected to VDDnom or to the gate of the transistor below, in the case with two or more switched transistors. In this situation the cascode transistor is in the triode region since its drain voltage is a threshold below its gate voltage. If the drain voltage of the switched cascode transistor is a threshold above the gate voltage or VDDnom, the rightmost pmos transistor will conduct, resulting in the situation in the lower right picture. In this situation the switch switches to the up position where the gate is connected to the drain, via the pmos transistor. Now M3 is in the saturation region and acts like a MOS diode, thereby limiting the voltages across the transistors.

VI. PA DESIGN.

A 1.9 GHz class F power amplifier design using two switched cascode transistors was made in a 0.25 µm CMOS process. A class F PA has the advantage that for a given maximum output voltage peak, it delivers in theory the highest amount of output power.

A. The single ended output stage.

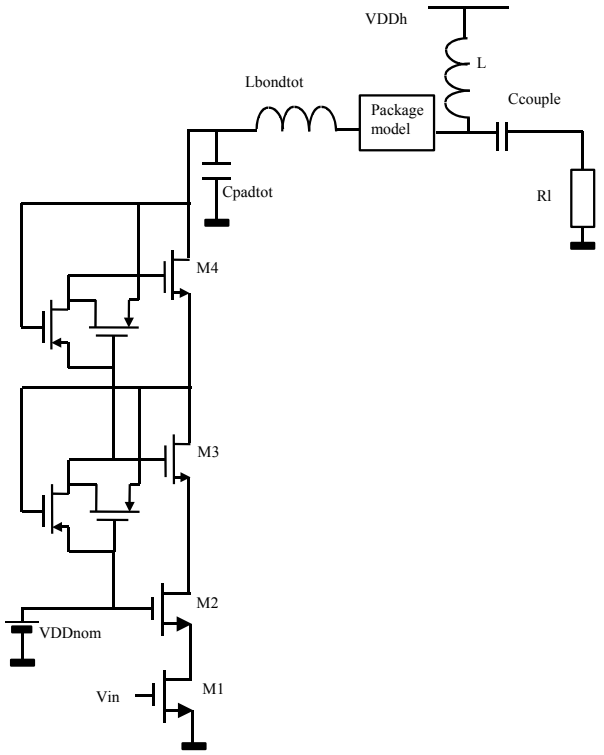

Figure 3 Single ended PA output stage.

Figure 3 shows the single ended PA output stage that uses 1900 µm wide transistors to get the desired amount of output power in a single ended 25 Ω load. This relatively high load value, due to the increased voltage swing, is precisely half of the differential input impedance of a balun. The output network that was used in simulations consists of the total pad capacitance, a bondwire and package model and an off chip inductor and couple capacitor. The value of the pad capacitors, bond wire inductance and resistance result from a parallel connection of 8, which is needed to minimize the total series impedance. The 3.9 nH inductor has a Q of 50 and the 40 pF capacitor was assumed to have a Q of 300. Simulations showed this configuration could safely withstand voltage peaks of 2.8 times the nominal supply voltage at the drain of M4. Furthermore without layout parasites the single ended output power was close to 24 dBm at 40 % PAE

A fully extracted layout was simulated and showed the single ended PA could deliver 21 dBm of output power at a PAE of 21 %. An improved layout, with lower gate resistance, was estimated to be able to deliver 22 dBm at 30 % PAE. Note that all PAE values include the matching network loss.

The third and fifth harmonic at –22 and –31 dBc of the output stage are to high to fulfill the DECT specification, although simulations did not include the filtering of a narrowband balun.

The chip area of the differential layout, without driver, bond pads or ESD diodes, is 0.09 mm^2.

B. Differential driver stage.

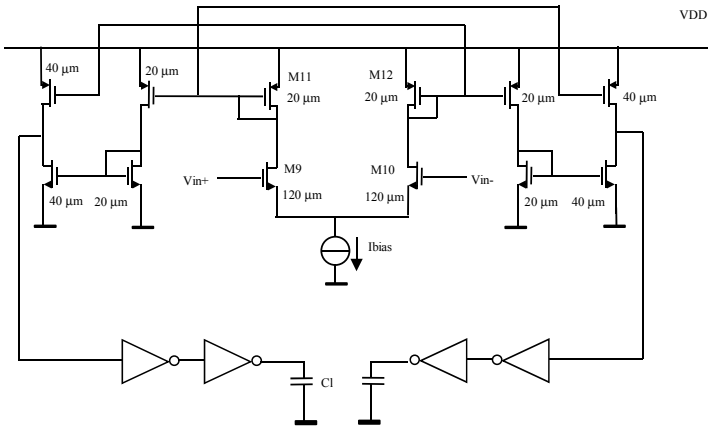

Figure 4 Differential driver stage.

Figure 4 shows a differential driver stage that uses no on chip or bondwire inductors. The input stage of the driver is a differential pair, M9 and M10, biased with a current source. The load of the differential pair consists of the two diode-connected transistors M11 and M12. Transistors M11 and M12 are part of a current mirror structure that copies the output current of the differential pair to the last transistors that form a small output stage. After this stage two more invertor stages are needed to give the output signal a final swing between VDDnom and ground across a 4 pF load. The driver accounts for a 6% efficiency drop due to the extra current consumption.

VII. CONCLUSIONS

The designed power amplifier can handle voltages higher than the nominal 2.5 V supply voltage of a 0.25 µm CMOS process: with the shown approach with two switched stacked transistors, it can reliably withstand up to 2.8 times the nominal VDD at RF frequencies.

The advantage of this configuration is the high value of the load resistor with respect to other reported CMOS power amplifiers. This loosens the demands for the required matching network, which in turn results in a higher efficiency for the matching network. Furthermore the high value of the load resistor reduces the absolute current values in and outside the circuit, making the impact of series resistance less severe.

The layouted output stage shows values for the output power and PAE that have decreased almost a factor 2 to 122 mW and 21 % with respect to the situation with no layout parasites. This decrease is mainly caused by the effect of the gate resistance that is added due to the length of the gate poly. Fully optimizing the layout would increase the power and efficiency to around 175 mW and 30 %.

The third and fifth harmonic of the output stage are too high to fulfill DECT specifications without additional filtering; the simulations however did not include the filtering of the used narrowband balun.

	This PA	**Nokia [3]**	**Stanford university [4]**	**University of California [5]**
Technology	0.25 µm CMOS	0.35 µm CMOS	0.25 µm CMOS	0.35 µm CMOS
Frequency [GHz]	1.9	1.8	1.4	1.98
Output power	0.25 W	1 W	0.3 W	1 W
PAE [%]	21	45	47	48
Size [mm^2]	0.09 (without driver)	1.9	2.4	0.6
Reliability	++	-	+	-

Table 1 PA comparison.

Comparison with other reported CMOS amplifiers is difficult because the exact conditions under which the published amplifier were measured are not clear. For example the losses of the matching network can be quite significant but even their presence is unclear.

The presented amplifier, which does not use inductances to boost efficiency, has a lower efficiency than published state-of-the-art PA's. However the area consumption, related to output power, is better than that of published amplifiers. However a fair comparison, or benchmarking, cannot be done in the absence of any reliability data and matching efficiency figures.

VIII. REFERENCES

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