A 65-nm CMOS Temperature-Compensated Mobility-Based Frequency Reference for Wireless Sensor Networks

Fabio Sebastiano*, Lucien Breems*, Kofi Makinwa† Salvatore Drago*, Domine Leenaerts* and Bram Nauta‡
*NXP Semiconductors, Eindhoven, The Netherlands, Email: fabio.sebastiano@nxp.com
†Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands
‡IC Design Group, CTIT Research Institute, University of Twente, Enschede, The Netherlands

***Abstract*— For the first time, a temperature-compensated CMOS frequency reference based on the electron mobility in a MOS transistor is presented. Over the temperature range from -55 °C to 125 °C, its frequency spread is less than ±0.5% after a two-point trim and less than ±2.7% after a one-point trim. These results make it suitable for use in Wireless Sensor Network nodes. Fabricated in a baseline 65-nm CMOS process, the 150 kHz frequency reference occupies 0.2 mm^2 and draws 42.6 μA from a 1.2-V supply at room temperature.**

I. Introduction

Wireless Sensor Networks (WSN) are based on small, cheap and energy efficient nodes. Since the largest fraction of the energy used in each node is spent listening to the channel, synchronous networks are employed to reduce such idle listening time [1]. In that case, the receiver predicts the timeslot that the transmitter will use and turns itself off when no incoming signal is expected. The duty-cycle of the receiver can be lower if the timeslot can be predicted with a smaller error, i.e. if a more accurate time reference is available. Accuracies of a few ppm can be achieved by crystal-controlled oscillators (XCOs), but since such external components should be avoided to reduce the cost and size of the nodes, accuracy must be given up for the sake of integration.

The tradeoff between integration and time/frequency accuracy is also present in the RF front-end. While commercial communication systems require high frequency accuracy, radios for WSN can be optimized to relax such specifications and so frequency accuracies in the order of only a few percent are needed [1] [2]. Thus, it is interesting to investigate which level of accuracy can be reached without external components, with the constraint to operate at the low voltage and power levels typical of WSN supplies.

Recently, much work has been devoted to implementing fully integrated frequency references in standard microelectronic technologies. *LC* oscillators [3] can provide accuracy and phase noise performances comparable to XCOs; however, their power consumption can hardly be reduced below 100 μW due to the limited Q of integrated inductors and the possible need for high-speed frequency dividers. Fully integrated frequency references based on ring oscillators [4] and silicon thermal diffusivity [5] are quite accurate, but dissipate several milliwatts of power. *RC* oscillators can achieve inaccuracies less than 1% while consuming less than 200 μW [6], [7], but their accuracy relies on the availability of on-chip resistors with low or, at least, accurately defined temperature coefficients.

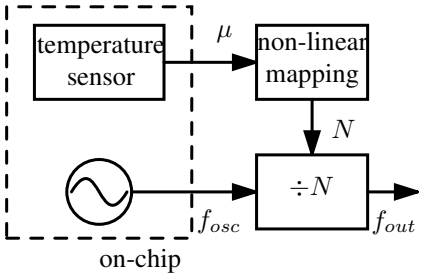


Fig. 1. Block diagram of the frequency reference.

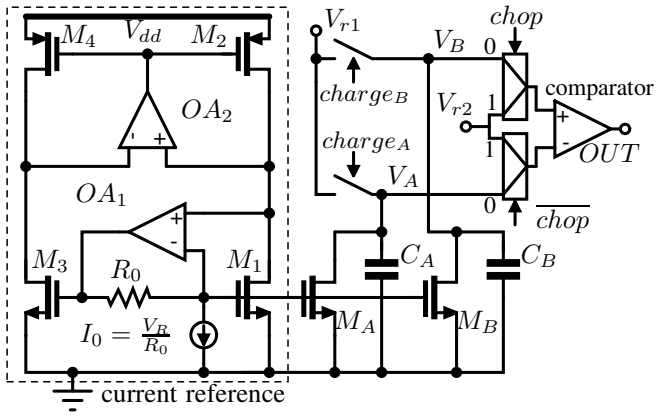
As an alternative, the mobility of charge in a MOS transistor can be employed as a reference. It exhibits low process spread and, although its temperature dependence is large (approximately proportional to $T^{-1.6}$, where T is the absolute temperature), it is well defined for a given process and thus can be compensated for. The effect of process spread can then be removed by a one or two temperature calibration.

In this paper, we explore the level of accuracy that can be achieved by a fully integrated temperature-compensated oscillator that is referenced to electron mobility. The proposed frequency reference comprises a current-controlled relaxation oscillator, in which the current is proportional to the mobility, and a bandgap-based temperature sensor for temperature compensation. Experimental validation of this approach will be provided, demonstrating that, after a two-point calibration, a frequency spread of less than ±0.5% can be achieved over the military temperature range. The circuit is presented in section II; experimental results are shown in section III and conclusions are drawn in section IV.

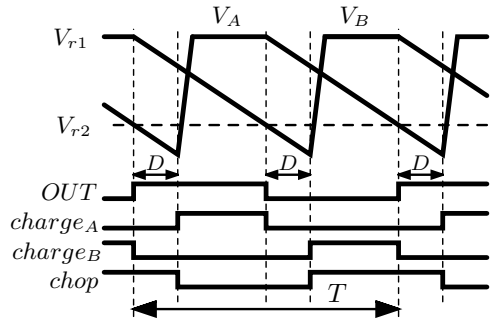
II. Temperature-Compensated Mobility-Based Reference

A. System Architecture

The proposed frequency reference consists of a mobility-referenced oscillator, a band-gap temperature sensor (TS)



(a)



(b)

Fig. 2. Mobility-referenced oscillator (a) and its waveforms (b).

and an external frequency divider (Fig. 1). The mobility-referenced oscillator generates a frequency f_{osc} proportional to the electron mobility μ_n in an NMOS transistor. Via a predetermined compensation curve, the digital output of the TS is mapped to a division factor N in such a way that the output frequency f_{out} remains constant over temperature.

B. Mobility-based oscillator

A simplified schematic of the mobility-based frequency reference is shown in Fig. 2(a) [8]. It consists of a low-voltage current mirror (formed by $M_{2,4}$ and OA_2) with gain $n = \frac{W_4/L_4}{W_2/L_2}$ and the NMOS pair $M_{1,3}$. The voltage difference between the gates of M_1 and M_3 is kept equal to V_R by the the combination of the current source I_0, R_0 and OA_1. Using the square-law MOS model, the drain current of M_1 can be written as

$$I_1 = \frac{\mu_n C_{ox}}{2} \frac{W_1}{L_1} \frac{V_R^2}{\left(\sqrt{\frac{n}{m}} - 1\right)^2} \tag{1}$$

where $m = \frac{W_3/L_3}{W_1/L_1}$, C_{ox} is the oxide capacitance per unit area and μ_n is the electron mobility [8]. The current source I_0 is implemented by mirroring the current flowing in a resistor matched to R_0 and whose voltage drop is equal to the reference voltage V_R (not shown in the schematic).

The drain current of M_1 is mirrored by M_A and M_B with a gain of four and used to alternatively discharge C_A and C_B after they have been precharged to V_{r1}. When the voltage on the discharging capacitor drops below V_{r2}, the output of the comparator switches and the linear discharge of the other capacitor starts. The recharge is delayed by a short interval D, ensuring that the comparator's non-idealities do not affect the slope of the discharge at the V_{r2}-crossing. Note that D is not critical, as it does not influence the period T. Using (1), the oscillation frequency is

$$f_{osc} = \frac{\mu_n C_{ox}}{4C(\sqrt{\frac{n}{m}} - 1)^2} \frac{W_1}{L_1} \frac{V_R^2}{V_{r1} - V_{r2}} \tag{2}$$

where $C = C_A = C_B \propto C_{ox}$. If V_R, V_{r1} and V_{r2}, are reference voltages then f_{osc} has the same temperature dependence as μ_n.

The two multiplexers at the input of the comparator, driven by the signal *chop* shown in Fig. 2(b), are used to mitigate the effect of comparator offset.

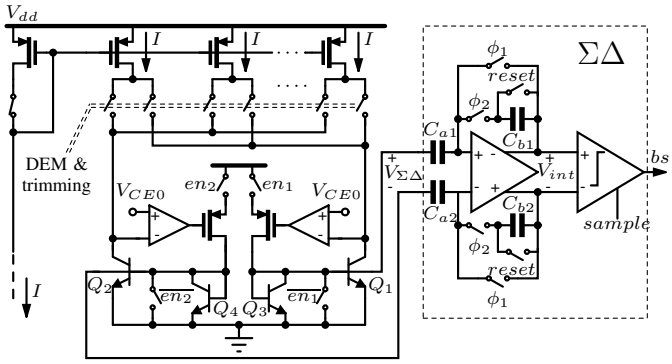


Fig. 3. Simplified schematic of the band-gap temperature sensor.

C. Temperature Sensor

The band-gap based TS is shown in Fig. 3 [9]. When $en_{1,2}$ are both high, the vertical NPN $Q_{1,2}$ are biased by the PMOS current sources array at a 1:4 collector current ratio to produce a PTAT difference between their base emitter voltages $V_{\Sigma\Delta} = \Delta V_{be}$. When en_1 (en_2) is high and en_2 (en_1) is low, Q_1 (Q_2) is biased by a fixed current and the base-emitter junction of Q_2 (Q_1) is shorted to produce $V_{\Sigma\Delta} = +V_{be}$ ($V_{\Sigma\Delta} = -V_{be}$). The feedback loops comprising the amplifiers and the common-source buffers compensate the base current of $Q_{1,2}$, so that neither ΔV_{be} nor V_{be} depends on the bipolar current gain. Moreover, the two loops increase the output impedance at the the collectors of $Q_{1,2}$, by fixing the collector voltages equal to the reference voltage V_{CE0}. To prevent the capacitive load of the analogue-to-digital converter from making the loops unstable, diode-connected $Q_{3,4}$ are added to lower the impedance at the base of $Q_{1,2}$.

A 1st-order $\Sigma\Delta$ analog-to-digital converter is used to produce an output bitstream bs whose average μ represents the TS output. The switched-capacitor integrator in the $\Sigma\Delta$ integrates $2 \cdot \Delta V_{be}$ when $bs = 0$ and $-V_{be}$ when $bs = 1$. Since the negative feedback forces the average integrated voltage to be

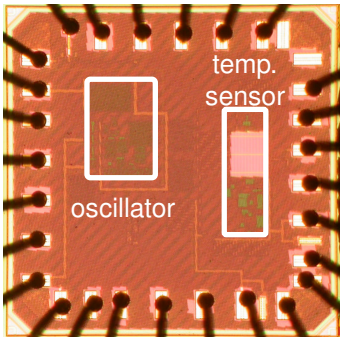


Fig. 4. Die micrograph of the test chip.

zero, the bitstream average is

$$\mu = \langle bs \rangle = \frac{2 \cdot \Delta V_{be}}{V_{be} + 2 \cdot \Delta V_{be}} \tag{3}$$

Although μ is a non-linear function of temperature, the biasing of the NPNs has been chosen [9] such that a function that is proportional-to-absolute-temperature (PTAT) can be obtained by applying the transformation

$$\mu_{PTAT}(\mu) = \frac{9 \cdot \mu}{1 + 8 \cdot \mu} \tag{4}$$

D. Temperature compensation

For flexibility, the temperature compensation scheme was implemented off-line in Matlab. However, it can be practically implemented without incurring much hardware complexity. For example, to determine fixed time intervals, the divide-by-N shown in Fig. 1 can be replaced by a simple counter. After an initial reset, the end of the time interval is denoted by the instant when the counter's output is equal to $M_{cyc} \propto N$, where M_{cyc} can be adjusted in a temperature-dependent manner. For time intervals in the order of $T_{meas} = 100$ ms as required for WSN synchronization [1], $M_{cyc} = T_{meas} \cdot f_{osc} \approx 15 \cdot 10^3$ at room temperature, which is equivalent to more than 13 bits of temperature compensating resolution.

For a single-point trim, the oscillation frequency of each sample at the trim temperature $f_{osc}(T_{trim})$ is measured. A seventh-order polynomial $P_7(\cdot)$, whose coefficients are fixed for all the samples, is then obtained via a batch calibration. The divider factor N is computed as

$$N = \frac{f_{osc}(T_{trim})}{f_{nom}} P_7(\mu) \tag{5}$$

where $f_{nom} = 150$ kHz is the nominal frequency of oscillation, i.e. the desired output frequency.

For two-point trim, the following procedure is adopted. The oscillator frequency f_{osc} and the on-chip TS decimated output μ are measured at two different temperatures, $T_{trim,1}$ and $T_{trim,2}$. Those data are used to interpolate the frequency using the interpolant

$$f_{osc} = A \cdot \mu_{PTAT}^{B} \tag{6}$$

where μ_{PTAT} is computed from the TS output using (4) and A and B are the trim parameters for each sample. A fourth-order polynomial $Q_4(\cdot)$ is obtained from batch calibration so

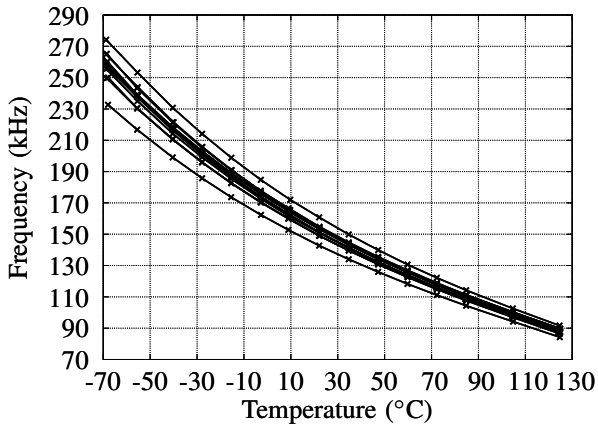


Fig. 5. Uncompensated oscillator output frequency (f_{osc}).

that the divider factor N computed for each sample is

$$N = \frac{1}{f_{nom}} A \cdot \{\mu_{PTAT}\,[Q_4(\mu)]\}^{B} \tag{7}$$

The polynomial[1] $Q_4(\cdot)$ is required to compensate for the fact that the power-law interpolant in (6) only approximately describes the temperature dependence of the electron mobility, especially over a wide temperature range.

III. Experimental Results

The frequency reference was fabricated in a standard 65-nm CMOS process (Fig. 4). The circuit occupies 0.2 mm^2 (0.1 mm^2 for the oscillator and 0.1 mm^2 for the TS) and uses only 2.5-V I/O thick oxide MOS devices. For flexibility, some control logic, the temperature sensor's sinc^2 decimation filter and the reference voltages $V_R = 0.25$ V, $V_{r1} = 1.6$ V and $V_{r2} = 1.2$ V were implemented off-chip. The reference draws 42.6 μA (34.3 μA for the oscillator and 8.3 μA for the TS) from a 1.2-V supply at room temperature. The supply sensitivity is 1.2%/V.

Measurements on 12 samples from one batch were performed over the temperature range from -70 °C to +125 °C using a temperature-controlled oven. The temperature of the samples was measured using a Pt100 platinum thermometer and compared to the temperature reading of the on-chip TS. The TS shows a spread on μ_{PTAT} of 0.5°C (3σ) over the range from -70 °C to +125 °C.

Fig. 5 shows the uncompensated output frequency of the oscillator. At room temperature, its maximum deviation from the average is ±6%. First, the samples were trimmed at $T_{trim} = 22$ °C and compensated with an external Pt100 and an ideal temperature compensation curve. In those conditions, the maximum error is ±2.6% over the military range from -55 °C to 125 °C. Then, the compensation polynomial $P_7(\cdot)$ (see section II-D) was extracted from batch calibration of the 12 devices. After a single-point trim at $T_{trim} = 22$ °C, the

[1]Note that the order of the polynomials $P_7(\cdot)$ and $Q_4(\cdot)$ is the minimum required for the error due to the non-linearity of the compensation to be negligible compared to the spread among the samples.

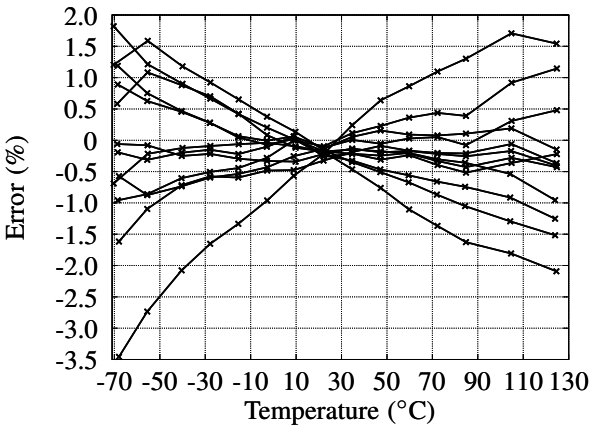


Fig. 6. Frequency error of the reference after single-point trim.

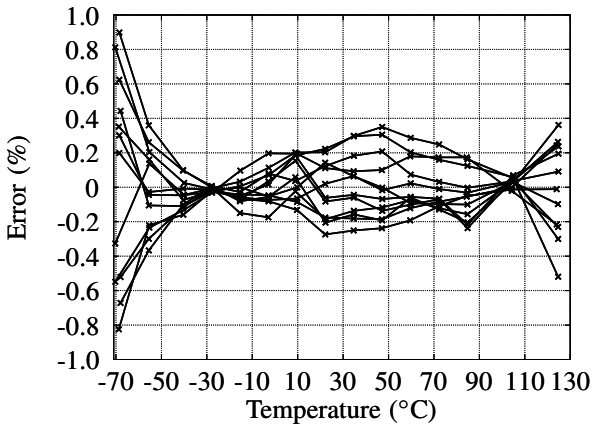


Fig. 7. Frequency error of the reference after two-point trim.

error when compensating with the on-chip TS is less than $\pm 2.7\%$ (Fig. 6). Finally, a two-point trim at $T_{trim,1} = -27$ °C and $T_{trim,2} = 105$ °C was employed and the error improved to $\pm 0.5\%$ using another compensating polynomial $Q_4(\cdot)$ (see section II-D) extracted from a batch calibration of the 12 devices (Fig. 7). For the adopted compensation schemes, the resolution of the integer divider factor N in Fig. 1 has been limited to 13 bits. Since this resolution can be easily reached in a practical implementation, as discussed in section II-D, the feasibility of the proposed compensation scheme is proved.

The frequency reference's performance is summarized in Table I and compared to other low-power fully integrated CMOS frequency reference. The proposed frequency reference achieves accuracy comparable to the state-of-the-art over a wider temperature range and for significantly more samples.

IV. Conclusions

A fully integrated temperature-compensated frequency reference based on electron mobility has been presented. Its inaccuracy is less than $\pm 2.7\%$ after single-point trim and less than $\pm 0.5\%$ after two-point trim over the military temperature range. This demonstrates that frequency references with inaccuracies less than 1% over a wide temperature range can be realized with MOS transistors, even in nanometer CMOS. Those references are accurate enough for WSN applications, while working at low-voltage and low-power, as required for the use in autonomous sensor nodes.

TABLE I

Performance summary and comparison.

Reference	[6]	[7]	[10]	This work	
Frequency	6 MHz	10 MHz	30 MHz	150 kHz	
Supply	1.2 V	1.2 V	3.3 V	1.2 V	
Power	66 μW	80 μW	180 μW	51 μW	
Technology	65 nm	0.18 μm	0.35 μm	65 nm	
Temp. range (°C)	0∼120	-20∼100	-20∼100	-55∼125	
Inaccuracy	$\pm$0.9%	$\pm$0.4%	$\pm$0.7%	$\pm$0.5%	$\pm$2.7%
Calibration	single	N.A.[a]	N.A.[a]	double	single
Samples tested over temp.	4	1	1	12	

[a]No calibration applied on a single sample.

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