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Optimized Stage Ratio of Tapered CMOS Inverters for Minimum Power and Mismatch Jitter Product

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Abstract

In this paper, an optimum stage ratio (tapering factor) for a tapered CMOS inverter chain is derived to minimize the product of power dissipation and jitter variance due to device mismatch. Analysis shows that this optimum stage ratio (2.4) is lower than that of minimum delay (3.6) and minimum power-delay (6.35) product. This analysis is verified by simulation results using standard 180nm as well as 90nm CMOS technology. Knowledge of the optimum stage ratio helps to design low power low mismatch jitter buffers for multi phase clock generation circuits that can drive large load capacitances.

Index Terms—tapering factor, stage ratio, CMOS inverter, mismatch jitter, multiphase clock, low power, figure of merit.

1. Introduction

Multiphase clocks are required in several applications such as time interleaved Analog to Digital Converters (ADCs) [1], polyphase multipath radio circuits [2] and image reject wireless receivers [3]. In all of these applications, phase error of the multiphase clocks severely degrades the performance by generating spurious tones in time interleaved ADCs [4], reducing the harmonic rejection in polyphase multipath radios [5] and limiting the image rejection and thus increasing bit error rate in the image reject receivers [3].

The phase error originates from the mismatch among the phase-generating blocks which are the delay element of a Delay Locked Loop (DLL) based multiphase clock generator and latches or flip-flops in a shift register based multiphase clock generator [6]. Given a good layout design and power supply, the delay variations in these blocks are primarily caused by the device mismatch among different blocks. We term this timing variation as "mismatch jitter" similar to [6]. For one phase clock, mismatch jitter is fixed after fabrication and thus only contributes to clock output skew. However, in case of multiple phases (for differential clock also), the mismatch jitter causes phase error. The noise (thermal noise, flicker noise etc.) generated timing error also causes phase error but its value much lower than error generated by mismatch jitter for MOS circuits. This is because the error current (or voltage) due to noise is much less than that of device mismatch [7]. It is also confirmed by simulations in [6] and [8]. Although static mismatch jitter can be reduced by digital calibration techniques but it adds considerable cost and complexity which increases with number of phases. Therefore, optimum circuit design by just component sizing is often preferred. Another performance parameter is the power consumption as we target for a portable application.

The phase generated form a multiphase clock generator is often needed to drive a large amount of capacitance. Depending on the fan-out, it is required to be decided whether to use extra buffer to drive the load. And if yes how many buffers should be used. In general, for the single ended and large swing clocks CMOS inverters and for low swing differential clocks, MOS Current Mode Logic (MCML) buffers are used. Mismatch jitter analysis along with power to optimize the MCML buffers has been reported [6][9]. However, mismatch jitter analysis on CMOS inverter is not done much.

To solve the number of buffer problem, traditionally a tapered chain of inverter analysis has been adopted to find the optimum stage ratio for minimum delay [10-11] and minimum power delay product [12]. We follow similar procedure only with a different optimization target. Mismatch analysis on a tapered buffer chain has been done by [13], however

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optimum stage ratio combining mismatch jitter and power consumption is not reported yet. In this paper, we aim to derive the optimum stage ratio for minimum power and mismatch jitter product by a simple analysis for a chain of inverters driving a given load capacitance.

The paper is organized as follows. Section II introduces a Figure of Merit (FoM) for power and mismatch jitter. Section III and Section IV estimates the mismatch jitter of an inverter and a tapered inverter chain respectively. In Section V the power consumption of the inverter chain is modeled. Section VI derives the optimum stage ratio from the FoM expression. Simulation results are presented in Section VII, while Section VII concludes this paper.

2. Figure of Merit: Power and mismatch jitter

The clock buffers need to size such that it gives both low power as well as low mismatch jitter. Via admittance level scaling [14], we know that both noise and mismatch jitter can always be reduced at the cost of increasing the power consumption. In order to take this tradeoff into account, jitter variance is normalized to power, similar to [6]. Thus a FoM is defined to combine the mismatch jitter and power in the following way:

$$FoM = \sigma_{t_p}{}^2 . P_d \tag{1}$$

where P_d is the power consumption and σ_{tp}^2 is the mismatch jitter variance. In simple word, a better FoM circuit will introduce less mismatch jitter for a given power budget and vice-versa.

3. Mismatch jitter of an inverter

The propagation delay of an inverter with a LOW to HIGH step input can be estimated as [15]:

$$t_{pHL} = \frac{C_L . V_{DD}}{K_n . (V_{DD} - V_{Tn})^{\alpha}} \tag{2}$$

where C_L is the total load capacitance, V_{DD} is the supply voltage, K_n is the transconductance parameter and V_{Tn} is the threshold voltage of an nMOS transistor. The α-power law model [16] with α<2 instead of the square-law model (α=2) is more appropriate for short channel devices which experience significant mobility reduction due to high electrical fields.

In (2) it is assumed that the average nMOS current is equal to the initial current during switching. The actual current will start degrading when the inverter output goes below (V_{DD} - V_{Tn}). This degradation will not be severe if (V_{DD} - V_{Tn}) is not much higher than the toggle point $V_{DD}/2$. Since new technologies use lower V_{DD} and for simplicity, we neglect this degradation. Another assumption used in (2) is that the input is considered as an ideal step. This assumption simplifies the math and can still give reasonable accurate results as discussed in [15].

In a very similar manner we can find the inverter delay for a HIGH to LOW input transition as:

$$t_{pLH} = \frac{C_L . V_{DD}}{K_p . (V_{DD} - V_{Tp})^{\alpha}} \tag{3}$$

The nominal inverter delay is the average of (2) and (3) and represented as:

$$t_{pINV} = \frac{1}{2}\left[\frac{C_L . V_{DD}}{K_n . (V_{DD} - V_{Tn})^{\alpha}} + \frac{C_L . V_{DD}}{K_p . (V_{DD} - V_{Tp})^{\alpha}} \right] \tag{4}$$

When an inverter is un-loaded, C_L is equal to its intrinsic capacitance C_{int} (mainly its drain-bulk capacitance). We call the delay of the un-loaded inverter the intrinsic delay $t_{p\_int.}$ It is independent of the fan-out and sizing of the gate and is purely determined by the technology and layout. It can be represented similar to (4) just by replacing C_L with C_{int} as:

$$t_{p\_\mathrm{int}} = \frac{1}{2}\left[\frac{C_{\mathrm{int}} . V_{DD}}{K_n . (V_{DD} - V_{Tn})^{\alpha}} + \frac{C_{\mathrm{int}} . V_{DD}}{K_p . (V_{DD} - V_{Tp})^{\alpha}} \right] \tag{5}$$

In an inverter chain, an inverter is loaded by the next inverter. If C_{ext} is the "extrinsic" (load) capacitance, i.e. mainly the gate capacitance from the next inverter stage, such that $C_L = C_{int} + C_{ext}$, (4) can be written as:

$$t_{pINV} = \frac{C_{\mathrm{int}} + C_{ext}}{2}\left[\frac{V_{DD}}{K_n . (V_{DD} - V_{Tn})^{\alpha}} + \frac{V_{DD}}{K_p . (V_{DD} - V_{Tp})^{\alpha}} \right] \tag{6}$$

and

$$t_{pINV} = t_{p\_\mathrm{int}} [1 + \frac{C_{ext}}{\gamma C_g}] \tag{7}$$

where C_g is the gate capacitance of the driving inverter, and γ is the ratio between the drain and gate capacitance of any inverter in the chain with a value between 0 to 1 and close to 1 for most sub-micron process [17,pp. 253].

The delay of any inverter can now be related to its fan-out r using $C_{ext} = rC_g$, as:

$$t_{pINV} = t_{p\_\mathrm{int}} (1 + \frac{r}{\gamma}) \tag{8}$$

Due to mismatch in the parameters such as K_n, K_p, V_{Tn}, V_{Tp} and C_L, there will be uncertainties in the amount of inverter delay which we call the "mismatch

jitter". The mismatch jitter variance of an inverter can be found from (4) via partial derivatives as:

$$\sigma^2_{t_{pINV}} = \frac{t_{pINV}^{\ 2}}{4}\left[\begin{array}{l} 2\dfrac{\sigma_{C_L}^{\ 2}}{C_L^{\ 2}} + \dfrac{\sigma_{K_n}^{\ 2}}{K_n^{\ 2}} + \dfrac{\alpha^2\sigma_{V_{Tn}}^{\ 2}}{(V_{DD}-V_{Tn})^2} + \\ \dfrac{\sigma_{K_p}^{\ 2}}{K_p^{\ 2}} + \dfrac{\alpha^2\sigma_{V_{Tp}}^{\ 2}}{(V_{DD}-V_{Tp})^2} \end{array}\right] \quad (9)$$

where $\sigma_{V_{Tn}}^{\ 2}, \sigma_{V_{Tp}}^{\ 2}\sigma_{C_L}^{\ 2}, \sigma_{K_n}^{\ 2}, \sigma_{K_p}^{\ 2}$ are the variances of V_{Tn}, V_{Tp}, K_n, K_p, and C_L variations respectively. The nominal HIGH to LOW and LOW to HIGH delay are assumed to be equal here by choosing proper nMOS and pMOS widths.

In a very similar manner mismatch jitter of a un-loaded inverter can be represented by partial derivative of (5) as:

$$\sigma^2_{t_{p\_\mathrm{int}}} = \frac{t_{p\_\mathrm{int}}^{\ 2}}{4}\left[\begin{array}{l} 2\dfrac{\sigma_{C_{\mathrm{int}}}^{\ 2}}{C_{\mathrm{int}}^{\ 2}} + \dfrac{\sigma_{K_n}^{\ 2}}{K_n^{\ 2}} + \dfrac{\alpha^2\sigma_{V_{Tn}}^{\ 2}}{(V_{DD}-V_{Tn})^2} + \\ \dfrac{\sigma_{K_p}^{\ 2}}{K_p^{\ 2}} + \dfrac{\alpha^2\sigma_{V_{Tp}}^{\ 2}}{(V_{DD}-V_{Tp})^2} \end{array}\right] \quad (10)$$

The only difference between the bracket-ed parts in (9) and (10) is the capacitance variations. Compared with variations in V_T and K, capacitance variations are usually small, as observed in [6]. With this assumption, (9) and (10) can be related using (8) as:

$$\sigma_{t_{pINV}}^{\ 2} = \sigma_{t_{p\_\mathrm{int}}}^{\ 2}\left(1+\frac{r}{\gamma}\right)^2 \quad (11)$$

4. Mismatch jitter of a inverter chain

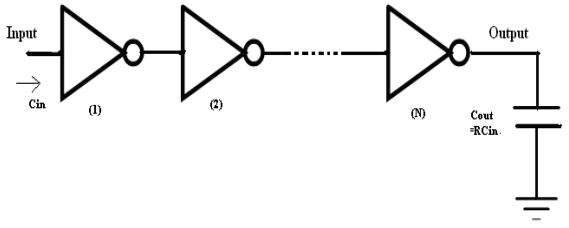

Figure 1: A chain of *N* inverters with fixed input and output capacitance

Let us now consider the circuit shown in Fig. 1, where C_{in} and C_{out} are the input and output capacitance fixed by a specific application. For example C_{in} will be the input capacitance of the first inverter which is defined by the acceptable load of the circuit driving the first inverter, and C_{out} by the load capacitance or the input capacitance of the block to be driven. Typically a chain of tapered inverters is used when there is a large difference between C_{in} and C_{out}. The ratio $R = C_{out} / C_{in}$ is the overall fan-out for the chain of N inverters with each inverter having a fan-out of r. For a given R, our aim is to find the optimum value of r which gives the minimum *FoM*.

Although the amount of delay is equal for all the stages in an inverter chain, the mismatch jitter variance will differ because of the different sizes. If we compare the 1st and the 2nd stage, the inverter area as well as load capacitance are sized up by a factor of r for the 2nd stage. According to mismatch theory [18][19], the mismatch variance of the 2nd stage will be r times smaller than that of the 1st stage also exploited during admittance level scaling [14]:

$$\sigma_{t_{pINV\_2}}^{\ 2} = \frac{\sigma_{t_{pINV\_1}}^{\ 2}}{r} \quad (12)$$

Similarly, for N^{th} inverter in the inverter chain, the mismatch jitter variance can be related to the first stage as:

$$\sigma^2_{t_{pINV\_N}} = \frac{\sigma^2_{t_{pINV\_1}}}{r^{N-1}} \quad (13)$$

The total mismatch jitter variance of the inverter chain is the sum of the independent jitter variance terms of each stage. Thus,

$$\sigma_{t_{pINV\_total}}^{\ 2} = \sigma_{t_{pINV\_1}}^{\ 2} + \sigma_{t_{pINV\_2}}^{\ 2} + .. + \sigma_{t_{pINV\_N}}^{\ 2} \quad (14)$$

From (11), (13) and (14) we get the total mismatch jitter: The first stage intrinsic mismatch jitter is independent of r and thus can be considered as a constant here.

$$\sigma_{t_{pINV\_total}}^{\ 2} = \sigma_{t_{p\_\mathrm{int}\_1}}^{\ 2}\left(1+\frac{r}{\gamma}\right)^2 \frac{1}{r^{N-1}}\left[\frac{(r^N-1)}{(r-1)}\right] \quad (15)$$

5. Power consumption of the inverter chain as a function of fan-out

The main source of power consumption of an inverter is the dynamic switching power. Another source of power consumption is the "cross-bar" circuit power consumption which may be a considerable component if the output capacitance is low compared to the input capacitance [20]. In the present scenario,

the output capacitance of each inverter is larger than its input capacitance. Therefore, the short circuit power consumption can be ignored.

Recognizing that the load capacitance of any stage is scaled up by r (for a fan-out of r) from the previous stage, the load capacitance of any stage can be represented by the input capacitance C_{in}. The first stage power consumption is $f_{in}V_{DD}^2C_{in}r$ because its load is $r.C_{in}$. The total dynamic power of the inverter chain can be represented as,

$$P_d = f_{in}.V_{DD}^2.(r.C_{in} + r^2.C_{in} + ... + r^N C_{in}) \quad (16)$$

Where, f_{in} is the input clock frequency. With some manipulation (16) can be rewritten as:

$$P_d = f_{in}.V_{DD}^2.C_{in}\frac{r(r^N - 1)}{(r-1)} \quad (17)$$

6. Optimum inverter stage ratio for minimum FoM

The inverter chain mismatch jitter and power consumption can be used to get the FoM of the inverter chain. From (1), (15) and (17) and replacing r^N by R we get,

$$FoM = \sigma_{t_{p0\_1}}^2 f_{in}.V_{DD}^2.C_{in}.\frac{r^2}{R}\frac{(R-1)^2}{(r-1)^2}\left(1+\frac{r}{\gamma}\right)^2 \quad (18)$$

After differentiating (18) with respect to r and using the condition for minima we get an equation of r. After some simplification, the equation can be written as,

$$r^2 - 2r - \gamma = 0$$

If we ignore the negative solution of r we get,

$$r = 1 + \sqrt{1+\gamma} \quad (19)$$

Therefore, r=2 for γ=0 and r=2.414 for γ=1

As γ is generally close to 1 [17], the optimum value of the stage ratio is close to 2.4. This is smaller than the optimum stage ratio for minimum delay. Table 1 shows the stage ratios for minimum delay [11], minimum power delay product [12] and the minimum FoM which is power and mismatch jitter product for different γ values. Though γ is close to 1, a wider range from 0-3 is chosen as in [12], to show its effect on the optimum stage ratio. It is clear that the optimum stage ratio for minimum power and mismatch jitter product is significantly less than that of minimum power-delay product.

Sizing base on the power-mismatch jitter product approach takes more power but it have much better FoM. From (18) we can say that compared to the power-delay product approach, it is less than 2 times. That means it introduces less mismatch jitter and thus relaxed the phase errors specifications for other blocks. In other word this approach reduces the mismatch jitter for a given power budget.

TABLE 1: Optimum stage ratio for minimum delay, power*delay and power*mismatch jitter

γ	Minimum Delay	Minimum Power*delay	Minimum power * mismatch jitter (FoM)
0	2.718	4.25	2
0.2	2.91	4.69	2.1
0.5	3.19	5.34	2.22
0.8	3.43	5.95	2.34
1	3.6	6.35	2.4
2	4.25	8.28	2.7
3	4.97	10.11	3

7. Simulation results

In order to verify the analytical results, simulations have been carried out in UMC 90nm technology on a long tapered inverter chain for different stage ratios, while keeping the input and output capacitance fixed. We have chosen overall fan-out, R=250. The choice is made such a way so that we get the required stage ratios maintaining integer number of stages. To get more resolution in the stage ratio, R can be increased to the square of this value. The stage ratio was chosen equal to 2, 2.2, 2.5, 3, 4 and 6.3 to realize an overall fan-out of 250 with a number of stages equal to 8, 7, 6, 5, 4 and 3 respectively. The first inverter has Wn=1μm and Wp=2.5μm, and C_{out} is set by an inverter of size Wn=250μm and Wp=625μm and the length of all the transistors are equal to the minimum length allowed for that technology. The pMOS to nMOS ratio is 2.5 because that gives equal rise and fall delay.

In Fig. 2 the delay of the inverter chain is plotted as a function of the stage ratio. Minimum delay is found for a stage ratio of 4, which is the closest compared to the value given in [11,17] as 3.6. Mismatch jitter is evaluated by Monte Carlo simulations using 100 iterations. Histogram plots were used to find the sigma value of the mismatch jitter. Fig. 3 shows the resulting mismatch jitter, power dissipation and *FoM* for different stage ratios. The lowest (best) *FoM* is found for a stage ratio of 2.5, which is close to the theoretically derived value. To allow for easy relative comparison to the minimum value, all the values in the plots are normalized to their corresponding value at 2.5 stage ratio. When stage ratio is larger than 2.5, the power dissipation decreases but the mismatch jitter increases.

To verify that mismatch jitter dominates over noise jitter as found in [7], we simulated the variance of noise jitter using spectre pnoise analysis. This variance was found to be about 5-6 times smaller than due to mismatch in 90nm and 20-30 times smaller in case of 180nm CMOS technology. This validates our assumption that the mismatch jitter dominates the phase error.

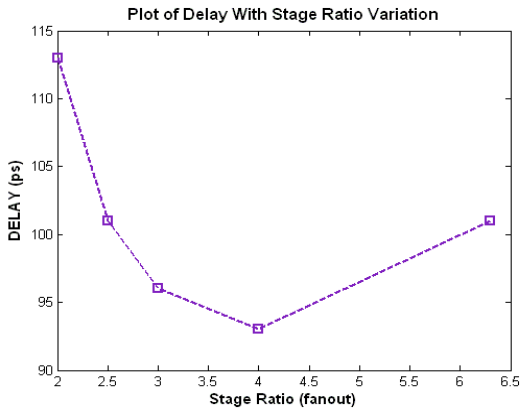

Figure 2: Delay versus inverter stage ratio in 90nm CMOS

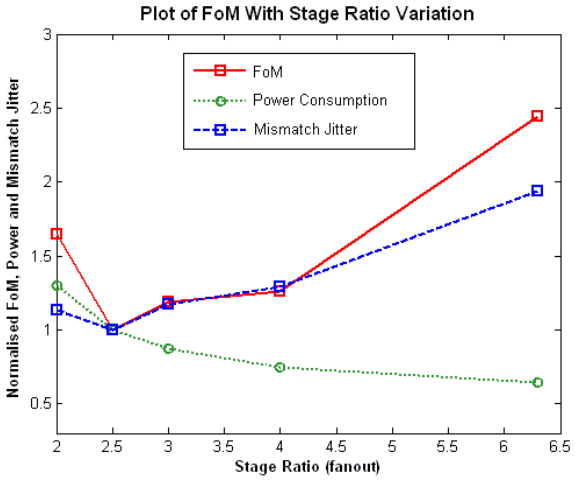

Figure 3: FoM versus inverter stage ratio in 90nm CMOS

The same simulations have been carried out in 180nm CMOS technology, where the inverter widths are the same as in 90nm, only the length changed to the minimum value of 180nm. The (normalized) power, mismatch jitter and FoM for different stage ratios are plotted in Fig. 4. Here again the minimum FoM is obtained when stage ratio is close to 2.5 which is similar to the result for 90nm technology. The FoM improves about 30% and 50% for 90nm and 180nm technology respectively at stage ratio of 2.5 compared to 4 which is often used as a thumb rule [21]. It also gives 2 to 2.5 times improvement compared to the power delay product approach.

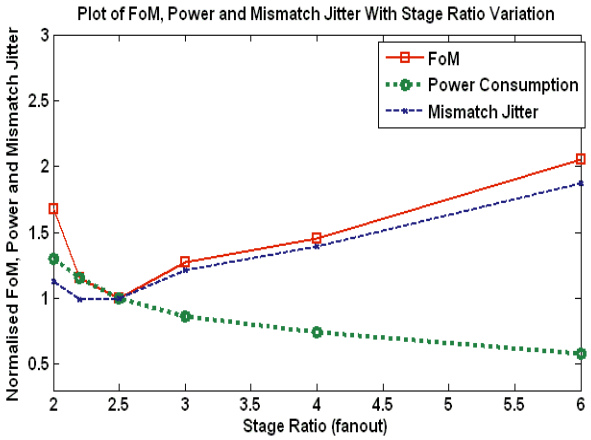

Figure 4: FoM versus inverter stage ratio in 180nm CMOS

8. Conclusion

We derived an optimum stage ratio for a tapered inverter chain to minimize the product of power and mismatch jitter variance with a simple inverter delay model. We assumed that transistor mismatch dominates jitter which is true for 90nm technology and above. The theoretical optimum is $r = 1 + \sqrt{1+\gamma}$, where γ is the ratio between the drain and gate capacitance of the inverter. Simulation results show an optimum $r \approx 2.5$ for both 90nm and 180nm CMOS technology, which fits to expectations ($\gamma \approx 1$). This result will help in sizing inverters and digital gates in phase error sensitive applications such as multiphase clock buffers.

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