A 1Volt Switched Transconductor Mixer in 0.18μm CMOS

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Abstract

A new CMOS mixer topology can operate at low supply voltages by using switches connected only to the supplies. Mixing is achieved exploiting two cross-coupled transconductors, which are alternatingly activated by the switches. A down conversion mixer prototype with 12 dB conversion gain was designed and realized in standard 0.18μm CMOS. It achieves satisfactory mixer performance up to 4GHz, at a supply voltage of 1 Volt. Moreover, the mixer topology features a fundamental high frequency noise figure benefit.

***Index Terms*—Mixer, receiver, low noise, wide band, CMOS.**

I. INTRODUCTION

Mixers are commonly used for frequency translation in radio frequency (RF) communication systems. The frequency translation results from multiplication of the RF input signal with a "local oscillator" (LO) signal. In practice, mixers are preferably implemented using "hard switching" via a large LO signal, which mathematically corresponds to multiplication with a square wave, instead of a sine wave. This renders higher conversion gain ($2/\pi$ instead of ½), and lower noise figure. Especially in CMOS and BiCMOS technology, where MOSFET switches are readily available, almost all mixers exploit switching in some form [1].

A key problem for the realization of analog circuits in current and future digital CMOS technology is the continuously reducing supply voltage. This leads to the well-known problem of non- or poorly conducting switches in the "middle voltage range" between the supply voltages [2]. This is a severe problem in analog and mixed analog-digital circuits exploiting switches, like A/D and D/A converters and switched capacitor circuits, but also in mixers. We will discuss this mixer switch problem in section II, taking a commonly used active CMOS mixer as a starting point. A *"switched transconductor"* mixer will then be proposed as a solution in section III. In section IV we show that it has a fundamental high-frequency noise advantage. Experimental results on a 1 Volt Switched Transconductor mixer realized in 0.18μm CMOS are reported in section V, while conclusion are presented in section VI.

II. SWITCH PROBLEM IN TRADITIONAL MIXERS

Fig. 1a shows a commonly used active mixer (single balanced version). It consists of a transconductance stage M1, switches M2 and M3, and a load network.

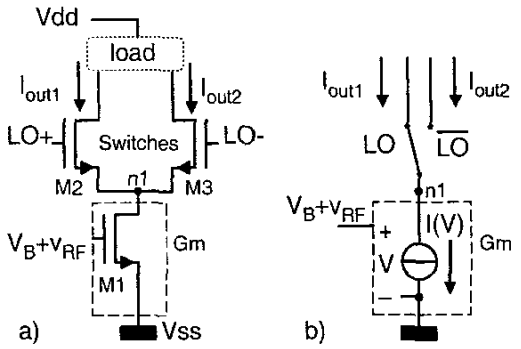

Fig. 1: a) Single balanced active MOS mixer and b) Schematic functional representation for large switching signals.

The transconductance stage (M1) is biased around V_B and is designed to implement a linear voltage to current conversion from v_{RF} to the variation in the drain current of M1. Source degeneration resistors are often added for linearization. The switches M2 and M3 are driven by anti-phase LO-signals LO+ and LO-, balanced around a bias voltage $V_{B,LO}$. To mimic multiplication with a square wave at the LO frequency, the LO-amplitude must be chosen sufficiently high to fully switch the transconductor current I_{d1} to either I_{out1} or I_{out2}. For the purpose of a first order functional description, we can model the operation of M2 and M3 as switches driven by the logic signals LO and its inverse $\overline{LO}$, as shown in Fig. 1b. Actually, M2 and M3 are preferably operated in saturation, to act alternatingly as cascode devices to M1, improving output resistance and linearity. Depending on the application, the output currents are connected to different load networks (e.g. resistors to positive supply voltage V_{dd} to provide wideband voltage conversion gain, or a tuned LC network to provide gain only in a narrow band). As we want to focus on the V-I core that realizes the frequency translation, we will leave out this load network for now. Thus, the mixer has a conversion transconductance, instead of conversion voltage gain.

Consider now the operation of this circuit for low supply voltages. For good linearity, transistor M1 in the G_m-stage must have sufficient gate-source and drain-source voltage headroom: only if M1 is well in strong inversion and saturation, the transconductance stage achieves good linearity. To achieve an IIP3 well above 0 dBm, typical minimum drain-source voltage values for a 0.18μm CMOS process are in the range of 0.5V or more. With threshold voltages around 0.5V, this means that the minimum voltage at the gate of M2 and M3, to switch these

devices on, is typically higher than 1 Volt. Moreover, large overdrive voltage for the switches is desired to achieve low switch resistance. Therefore, either supply voltages well above 1 Volt are required, or a switch driver circuit, driving the gate well above V_{dd}. Such drivers are not easily implemented at GHz frequencies, especially when wide bandwidth is required and LC tanks are impractical. Moreover, the maximum allowed gate voltage is decreasing for new technologies (oxide reliability).

To address these problems, folded topologies have been proposed, e.g. with PMOS switches following a NMOS transconductance stage [3]. However, this requires adding a bias current source that adds substantial noise, unless significant voltage headroom is reserved (but then the switch again becomes the problem). In other popular mixers, like the passive mixer, very similar problems occur, especially in downconverison mixers, where AC coupling often is not possible (e.g. zero IF architecture) or requires very large capacitors (low IF architecture). The essence of the problem is the same: achieving low switch resistance at voltage levels "in the middle range" between the supply voltages is impossible without driving gates outside the supply. This problem becomes even more severe in future processes with even thinner gate-oxides and lower supply voltages, while threshold voltage only scale down slowly. Alternative mixer architectures able to operate at a low supply voltage directly compatible with digital CMOS technology are therefore desired.

III. Switched Transconductor Mixer

The key to the new mixer is the observation that the problems discussed in the previous section relate to requiring a conductive channel at a voltage level in "the middle range" between the supplies V_{ss} and V_{dd}. However, it is easily possible to make low ohmic switches, provided that their conductive channel is connected to V_{ss} (NMOST) or V_{dd} (PMOST). We can rely on this even in future CMOS technologies, for the simple reason that *digital logic circuits rely on this functionality (inverters).*

Fig. 2a shows conceptually how a single balanced mixer can be constructed using two matched transconductors G_{m1} and G_{m2} and *switches connected to voltages V_{ss} and V_{dd} only.* The transconductors are alternatingly switched on by a switch to V_{ss}, and switched off by a switch to V_{dd}. Thus G_{m1} is on, if G_{m2} is off, and the other way around. Now, for matched transconductors and ideal timeless switching, either I_{out1} or I_{out2} is equal to $G_m v_{RF}$, just as in fig. 1. Actually, the circuits implement the same mixer function in different ways: the traditional mixer by a V-I conversion followed by current switching, the new mixer by directly switching transconductors (activate one of two "Switched Transconductors" G_{m1} and G_{m2}).

Single balanced mixers have a strong output signal at the LO-frequency, which can be cancelled in a double balanced version. By adding two additional transconductors driven by an anti-phase RF signal, as shown in Fig. 2b, this is readily implemented. Again, the double balanced switched transconductor mixer has the same nominal conversion gain than a double balanced version of the active mixer in fig. 1.

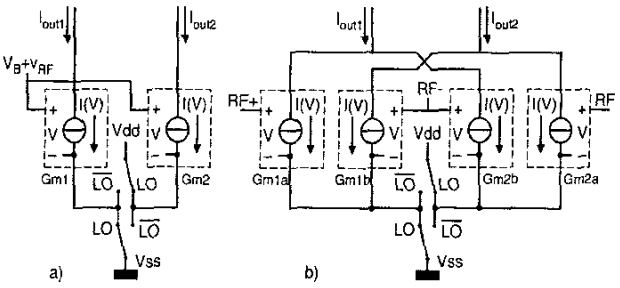

Fig. 2: a) Single balanced Switched Transconductor Mixer concept; b) Double balanced Switched Transconductor Mixer.

Despite of the functional equivalence, there are also very significant differences. Most notably, in the traditional mixer there is an internal node between the transconductor and the output node, which renders bandwidth limitations due to parasitic capacitance (node n1 in fig. 1) and also distortion and noise effects. This *internal node is lacking* in the switched transconductor mixer. Moreover, the switches to V_{ss} constitute a common-mode current path for the two active transconductors to the output. This ideally renders a constant common-mode output current, for ideal timeless switching. In practice, switching transients occur with most energy concentrated at $2f_{LO}$. This can easily be filtered out by capacitors to ground. These common-mode currents also come with noise, however this hardly harms mixer noise figure as will be discussed in the next section.

IV. High Frequency Switch Noise Advantage

As mentioned in the previous section, the noise current introduced by the switching devices is a common mode noise current. Thus, this noise current *cancels* in the *differential* output current I_{out1}-I_{out2}. For the mixer in fig. 1 the situation is completely different. This is because there is a *direct noise current path* between the outputs out1 and out2: when the nodes LO+ and LO- have approximately the same voltage, both switch transistors conduct and have significant noise current, resulting in a noise peak around the zero-crossing [4]. Also, LO noise is amplified during this time interval [1][4]. This noise comes on top of the noise of the transconductance stage, and dominates at high frequencies where the "zero-crossing region" constitutes a large portion of the LO time period. A similar effect occurs in passive mixers. In contrast, the switched transconductor mixer doesn't show this effect, as noise generated by the switch devices is *common mode noise!*

The difference in HF noise was verified by simulations. The transconductor was implemented using NMOSTs with W/L=15/0.3, nominally biased at V_{GS}=V_{DS}=0.65Volt (0.5Volt threshold voltage). The switches have W/L=15/0.18 (NMOST) and 30/0.18 (PMOST), and are driven with 0dBm LO power

(50 ohm termination, balanced signals around a common mode voltage $V_{dd}/2$). The conversion transconductance is around 1mS, and the bandwidth of both mixers was around 4GHz. Fig. 3 shows the simulated thermal output noise current density with a low-ohmic termination of both the switched transconductor mixer core and the traditional active mixer.

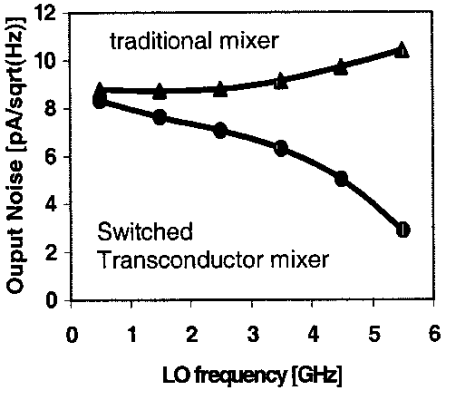

Fig. 3: Output Noise at 1MHz of a Switched Transconductor Mixer and Traditional Active mixer as a function of the LO frequency.

Clearly the output noise behavior is very different: where the Switched Transconductor mixer output noise decreases (roughly following the frequency roll-off of the conversion transconductance), the output noise of the traditional mixer increases! This low noise of the Switched Transconductor mixer is highly desired, because Low Noise Amplifiers usually have decreasing gain at high frequencies, thus increasing the relevance of low mixer noise at high LO frequencies.

V. Implementation and Measurements

In order to verify the new mixer concept experimentally, a down conversion mixer was designed to operate at 1 Volt supply voltage. Fig. 4 shows the schematic that was realized on chip: a straightforward simple implementation of the double balanced Switched Transconductor Mixer concept of fig. 3. The transconductors are shown in the dashed boxes (M5-M8). Somewhat arbitrarily, the transconductance was chosen around 1mS. Transistors M1 and M2 implement the switches to V_{ss}, while M3 and M4 implement the switches to V_{dd}. They are driven by anti-phase sine-wave signals around a common voltage equal to the inverter switch threshold (close to $V_{dd}/2$). Note that sine-waves are used here for experimental reasons, but full swing digital signals can also be used, enhancing the compatibility with digital CMOS.

To generate an output voltage, an I-V converter must be added. This is implemented by the common-mode current-absorption circuit with two resistors and two PMOSTs in the upper part of Fig. 4. However, this circuit has a rather low common-mode output voltage. By adding a bias current source I_b, the common-mode output voltage is shifted up to a value around 0.6 Volt, to fit in the 1Volt supply voltage. The mixer was designed for a maximum conversion gain of around 20 dB (R_{out1}=R_{out2}=10kohm), which can be lowered adding an external resistor between the output V_{out1} and V_{out2}. In the measurements that follow, this resistor was chosen in the middle of the gain range to achieve 12dB conversion gain.

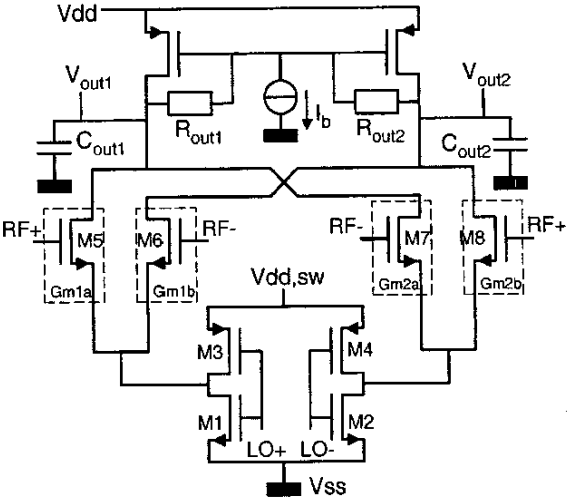

Fig. 4: Double balanced Switched Transconductor mixer implemented on chip.

The mixer was fabricated in a standard industrial 0.18µm CMOS process. Fig. 5 shows a photograph of the mixer core.

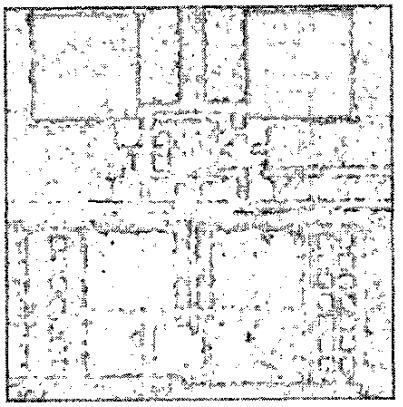

Fig. 5: Chip Photograph of the Switched Transconductor mixer core (0.18 µ CMOS, 75um * 65um) (capacitors not shown).

Termination resistors of 50ohm were added on chip for all the RF and LO inputs for ease of measurement. The chip was measured via wafer probing, using baluns for single to differential conversion at the input. A differential probe was used to measure the differential output voltage. The IF bandwidth was 2MHz, limited by the input capacitance of the probe (>10MHz is easily obtainable with an on-chip load).

The conversion gain as a function of frequency was measured using two baluns with overlap in frequency range: one for the 300MHz-3GHz band and one for 2-18GHz. The measurements

are shown in Fig. 6. Despite of experimental inaccuracies it can be concluded that the mixer has 12dB conversion gain and around 4GHz LO bandwidth, which is in reasonable agreement with simulation. The current consumption of the mixer consists of a more or less constant term of 180μA for the transconductors core, and a dynamic term determined by the switching (≈ 200μA/GHz). Note that the power consumption is low because the transconductance is rather low, resulting in a high equivalent input noise resistance. To achieve less than 15dB noise figure with respect to 50ohm, roughly 10 times higher transconductance, i.e. 10 times more power consumption, is needed ("Impedance Level Scaling", see section VI of [5]). At 1 GHz this will result in roughly 4mW power consumption.

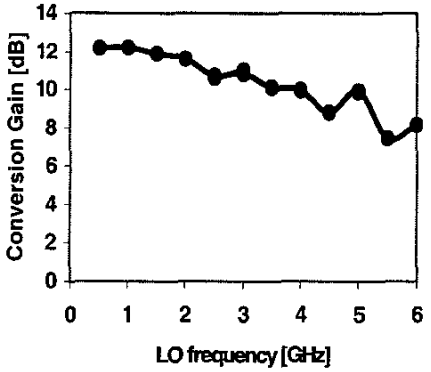

Fig. 6: Conversion Gain as a function of the LO frequency.

Fig. 7 shows the linearity of the mixer as a function of frequency. An IIP3 better than +4dBm is typically achieved for 12 dB conversion gain. Simulations and experiments with varying R_{out} showed that this linearity is limited by the output swing. Actually CG and IIP3 can be traded. Simulations show that an IIP3 in excess of +10dBm is possible if the output voltage swing is reduced.

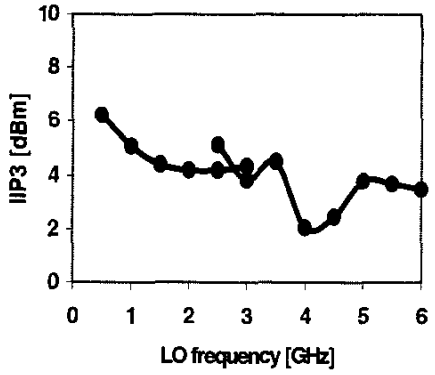

Fig. 7: IIP3 as a function of the LO frequency.

Last, but certainly not least, the remarkable noise properties of the new mixer were verified by measurements. Fig. 8 shows the output noise as a function of frequency, measured at 1MHz IF frequency. The trend is similar to the conversion gain fall off, in agreement with the simulation results shown in Fig. 3. Also the values fit roughly to the noise current expected from the transconductor core according to simulation. The 1/f corner frequency was around 1MHz.

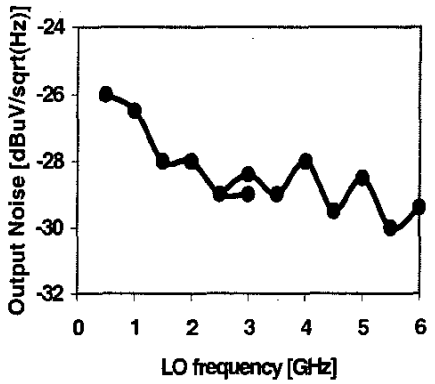

Fig. 8: Density of the output noise at 1MHz versus LO frequency

VI. Conclusions

A 1 Volt switched transconductor mixer has been realized in standard 0.18μm CMOS, with 0.5Volt threshold devices. It can operate at such low supply voltage, compatible with future digital CMOS, because only switches with a conductive channel connected to either V_{ss} or V_{dd} are used. In contrast to traditional active and passive CMOS mixers, the noise produced by the switch transistors is common-mode noise, which is rejected at the differential output. As a consequence, the output noise of the switched transconductor mixer does not increase with LO frequency, in contrast to traditional active and passive mixers.

Acknowledgements

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