A CMOS Spectrum Analyzer Frontend for Cognitive Radio Achieving +25dBm IIP3 and -169 dBm/Hz DANL

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Abstract—A dual RF-receiver preceded by discrete-step attenuators is implemented in 65nm CMOS and operates from 0.3–1.0 GHz. The noise of the receivers is reduced by cross-correlating the two receiver outputs in the digital baseband, allowing attenuation of the RF input signal to increase linearity. With this technique a displayed average noise level below -169 dBm/Hz is obtained with +25 dBm IIP₃, giving a spurious-free dynamic range of 89 dB in 1 MHz resolution bandwidth.

Index Terms—cognitive radio, cross-correlation, energy detection, IIP₃, linearity, noise figure, spectrum analyzer, spectrum sensing, spurious-free dynamic range

I. INTRODUCTION

The FCC was considering spectrum sensing for cognitive radio (CR) in the TV-bands (50 to 900 MHz), but has recently decided to use a spectrum database to register and protect primary users. This is partly based on an experiment where prototypes (mostly from companies) were able to detect very weak signals in a clean spectrum, but failed in the presence of a large interferer [1]. This is likely caused by their limited spurious-free dynamic range (SFDR), which is a key specification of radio receivers and spectrum analyzers (SAs). Nevertheless, the FCC has indicated it still thinks of spectrum sensing as a promising solution.

The SFDR characterizes the maximum power difference between signal and noise+distortion, and is limited by the linearity (IIP₃ mostly, sometimes IIP₂) and the noise floor. As receivers can already have low NF, there is more room for improving the SFDR by increasing the linearity. With a passive attenuator at the input, every dB of attenuation adds one dB to IIP₂ and IIP₃, but also to NF, keeping SFDR constant. The tradeoff between noise and linearity can be broken by using cross-correlation (xc) of the output of two independent receivers to lower the system noise [2].

In a traditional SA, the frontend adds noise n to the input signal a , which results in the power spectral density (PSD) of $a + n$. If n is large compared to a , a will be obscured by the noise. Using xc, two independent frontends add noise n_1 and n_2 respectively, giving signals $u = a + n_1$ and $v = a + n_2$. The resulting cross-spectrum $S_{uv} = S_{aa} + S_{an_2} + S_{n_1a} + S_{n_1n_2}$ converges to S_{aa} (the PSD of the input signal) for increasing

Fig. 1. Block diagram of the entire SA

integration time, because the other terms have an expected value of 0 (assuming uncorrelated signal and noise sources). In other words, by measuring longer, the displayed average noise level (DANL)¹ is reduced; doubling the measurement time reduces the uncorrelated noise power by 1.5 dB [2], [3]. Eventually, only the correlated noise remains.

As xc relies on uncorrelated noise in the receivers, reducing parasitic coupling between the two receiver paths is very important. In [2], artifacts due to the used discrete components and parasitic coupling between boards and cables played a role. To get a more realistic estimate of achievable SA performance, we now integrated two identical RF-frontends on the same chip, as the RF-stages are most noise-critical and parasitic coupling tends to be stronger at RF. Compared to [2], two RF-frontends including variable attenuation are now fully integrated on one IC. The analog baseband section is still left off-chip to allow for more experimental freedom and to more easily measure the achieved RF linearity.

II. DESIGN

Fig. 1 shows an overview of the proposed SA and what is implemented on-chip. The RF-frontend of [4], consisting of a low-noise transconductance amplifier (LNTA) and a passive mixer, is taken as a basis. The mixer-first concept of [2] is

¹A SA with 10 dB NF has a DANL of $-174 + 10 = -164$ dBm/Hz

Fig. 2. The noise generated by the impedance matching devices introduces correlated noise between the two receivers, here shown for the noise of receiver 2.

abandoned to get more isolation between the frontends and thus allow more phase noise reduction using xc [2].

The LNTA transforms the input voltage into a current, which is mixed down by the mixer. Basic harmonic rejection (HR) is implemented to prevent out-of-band signals to mix down and change the measured spectrum. To improve linearity of the receiver, a passive attenuator is placed in front of the LNTA. At IF, with better handling of large voltage swings, a transimpedance amplifier (TIA) (here externally implemented with a TI-THS4130 opamp with RC-feedback) provides voltage gain simultaneously with low-pass filtering. More opamp stages and a passive 5th-order anti-alias filter are used to interface with 14-bit PC-based analog-to-digital converters (ADCs). The xc is performed in software on a PC using double precision. The processing consists of fast Fourier transforms (FFTs) and multiply-accumulates (MACs) and is described in more detail in [2]. At the output of the accumulator (still complex), the magnitude is taken for robustness to phase mismatch between the receivers [2].

The noise currents from the input matching of each receiver find their way to the input of the other receiver, introducing correlated noise, see Fig. 2. Theoretically, 3 dB of correlated NF is expected in the matched mode (if there is no additional coupling), regardless of the attenuation [2].

When spectrum sensing is not being performed, the receivers can be disconnected, and the second receiver may be turned off, or can be used as a second receiver (e.g. for MIMO). To provide impedance matching in all cases, the receivers can switch between 50 \$\Omega\$ and 100 \$\Omega\$ input impedance.

Fig. 3 shows the principle of the attenuator and LNTA circuit. The CG-stage is divided into two equally sized transistors (\$M_1\$, \$M_2\$), where \$M_1\$ can be turned on or off to define 50 \$\Omega\$ or 100 \$\Omega\$ input impedance. The PMOS in the CS-stage with CMFB-loop ensures proper biasing in both settings. Inductor \$L_{ext}\$ shunts low-frequency IM2 components of the CG-stage, avoiding IIP₃ degradation. The attenuator in front of the LNTA improves overall IIP₃: with \$A\$ the attenuation in dB, ideally $IIP_{3,cascade} = IIP_{3,LNTA} + A$ [dBm]. However, based on simple approximations, to get $IIP_{3,cascade} > IIP_{3,LNTA} + A - 1$ [dBm], $IIP_{3,att}$ should be larger than $IIP_{3,LNTA} + A + 6$ [dBm]. Separate \$\Pi\$-attenuators, able to match to 50 \$\Omega\$ and 100 \$\Omega\$, are designed for each setting (0, 2, 6, and 10 dB) and placed in parallel.

Fig. 3. Attenuator and CG-CS LNTA (only half-circuit shown)

Fig. 4. Chip micrograph with annotations.

To obtain the desired linearity, each setting uses the IM3 cancellation effect of r_{ds} elaborated in [5].

The mixer is passive, driven by an 8-phase LO [4]. The LO-generating circuitry employs a divide-by-8 for 2nd to 6th order HR, which limits the maximum LO-frequency to 1.0 GHz (8.0 GHz in).

III. MEASUREMENT RESULTS

The chip of 1 mm $\times$ 1 mm is shown in Fig. 4; the total active area (excluding decap) is 0.15 mm². The two identical receivers are rotated by 180° in layout (no strict receiver matching is required [2]). Each half of the differential input is connected via two large NMOS-switches in series (each $R_{on} \approx 2 \Omega$) to implement the optional connection without IIP₃-degradation and to shield off the capacitance of the 1 mm long low-ohmic wire when operating in single-receiver mode. The LO-circuitry consumes 7.6–20.4 mW per receiver at f_{LO} =0.3–1.0 GHz, while the on-chip analog circuitry consumes 15.3/12.8 mW in the 50 \$\Omega\$/100 \$\Omega\$-mode.

The measurement results are shown in Fig. 5 for the situation that the inputs of the receivers are connected. The insertion loss (IL) of wires and hybrid, but not the PCB, have been corrected for in the measurement results; off-chip baseband circuitry is not de-embedded.

The combined capacitance of the attenuators, LNTAs, four bondpads, and the long interconnect limits matching to

Fig. 5. Measurement results. In (b)-(e) the squares (triangles) indicate measurements at the output of receiver 1 (receiver 2).

650 MHz ($S_{11} < -9.4$ dB) for 0 dB attenuation. At 2 dB attenuation, the attenuator partly shields the capacitance, providing matching up to 1 GHz, while higher attenuation settings provide matching to even higher frequencies. The feedback resistance of the TIA is chosen to be 1 k Ω , which yields a gain of roughly 30 dB, at a NF of 10 dB. The worst-case measured CP is -1 dBm, while the worst-case measured IIP₃ is +15 dBm (measured with two input tones at 0.6 MHz and 0.8 MHz IF). The gain at the output of the second receiver is somewhat less due to the IL of the switches connecting the inputs of the two receivers (see Fig. 1), which also shows in the NF, CP and IIP₃ measurements. The NF, gain, CP and IIP₃ scale 1dB-per-dB with the attenuation. At 10 dB attenuation, the CP for frequencies above 300 MHz is above +12 dBm.

Fig. 5f shows the residual noise floor after xc, measured by inserting a known tone of low power at 1 MHz IF and determining the noise floor around -1 MHz IF (the IF-gain at 1 MHz is the same as at -1 MHz). The measured NF_{corr} is mostly around 3 dB, as expected. It is somewhat higher at lower frequencies, most likely due to flicker noise leaking through the CG-stages. We do not (yet) have an explanation for the higher NF_{corr} at 10 dB attenuation for higher frequencies.

Fig. 6 shows an example of the noise floor as a function of normalized measurement time (NMT), where NMT=1 equals

the time required to obtain enough samples for one FFT per receiver. Note that the effective NF at NMT=1 is about 1 dB than the NF reported in Fig. 5e because we look at the expected value of the absolute value of the accumulator output [2]. For a resolution bandwidth (RBW) of 1 MHz, obtaining enough samples for each FFT (independent of the actual ADC sample rate) takes 1 μ s. From Fig. 6 the effective NF decreases from 19 dB to 7 dB after 600 FFTs, improving SFDR by 8 dB, which takes only 0.6 ms, an acceptable time for CR.

Table I summarizes the measurement results and compares it to several other SAs. The achieved IIP₃ and NF (without xc) are comparable to that of the discrete implementation we presented in [2], but also to expensive commercial SAs. The SFDR we obtain due to the noise reduction obtained using xc is much higher than that of previously integrated solutions, and even outperforms that of the commercial SAs. It does so at a much lower power consumption and with much more integration.

IV. CONCLUSIONS

By employing xc of two receivers to reduce the noise floor for spectrum sensing at the cost of measurement time, a highly linear system can be designed. The 65 nm CMOS integrated prototype presented here (1.2 V supply) achieves +25 dBm IIP₃, which is in the range of expensive commercial SAs,

(a) Noise floor as function of NMT (10 dB attenuation)

(b) Effective NF as function of NMT

Fig. 6. Crosscorrelation noise measurement example at $f_{LO}=400$ MHz

TABLE I
COMPARISON WITH OTHER SPECTRUM ANALYZERS

Architecture	CMOS Tech-nology [nm]	Band [GHz]	Power [mW]	NF [dB]	NF _{corr} [dB]	Time penalty factor ^a	IIP3 [dBm]	SFDR [dB] (RBW=1MHz)
This work, 0dB att	65	0.30–0.65	41–54	11	5	16	15	83
This work, 2dB att	65	0.30–1.0	41–66	13	5	42	17	84
This work, 6dB att	65	0.30–1.0	41–66	17	5	$2.7 \cdot 10^2$	21	87
This work, 10dB att	65	0.30–1.0	41–66	21	5	$1.7 \cdot 10^3$	25	89
[2]	65+discrete	0.05–1.5	191	23	5	$4.3 \cdot 10^3$	24	88
[6]	180	0.40–0.9	180	50		1	–17	31
[7]	90	0.03–2.4	30–44	39		1	8	42
Tektronix RSA2203A		0.00–3.0		24		1	30	80
Agilent PXA-N9030A-503		0.00–3.6		18	8	$2.0 \cdot 10^2$	22	85

^a Time required to reach NF_{corr} within 1 dB

while at the same time it can achieve a much lower noise floor. Although adequate RF pre-filtering and a sufficiently linear integrated baseband section are yet to be shown, we conclude that xc with two linear frontends is promising to realize integrated SAs in CMOS with high SFDR and sensitivity.

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