Above-CMOS a-Si and CIGS Solar Cells for Powering Autonomous Microsystems

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Abstract

Two types of solar cells are successfully grown on chips from two CMOS generations. The efficiency of amorphous-silicon (a-Si) solar cells reaches 5.2%, copper-indium-gallium-selenide (CIGS) cells 7.1%. CMOS functionality is unaffected. The main integration issues: adhesion, surface topography, metal ion contamination, process temperature, and mechanical stress can be resolved while maintaining standard photovoltaic processing.

Envisaged PV-powered autonomous microsystem

Ultra-low-power autonomous microsystems can be fed by ambient energy using a variety of approaches [1]-[4]. Such microsystems typically contain an energy scavenging module, energy harvesting electronics, and electrical energy storage (e.g. a supercapacitor). In this work we study integration of a solar cell on a chip (Fig. 1) by “above-IC” CMOS post-processing [5]-[7].

The technological challenge is to integrate a photovoltaic energy scavenging component without compromising CMOS performance. Thin-film solar cell technology is mature, utilizes low-temperature process steps, and is well optimized for high yield at low cost [8]. In particular, amorphous-silicon (a-Si) and copper-indium-gallium-selenide (CIGS) photovoltaic (PV) technologies are attractive because of their relatively high efficiencies at indoor-lighting conditions [8][9]. Cadmium telluride (CdTe) solar cells also meet this requirement but raise environmental concerns. Above-IC integration of the *materials* a-Si and CIGS have been reported [10][11], but monolithic integration of PV cells above CMOS is to the best of our knowledge not yet shown.

Fig. 1: Envisaged autonomous microchip, comprising of a PV cell for energy collection; power management circuits in CMOS; integrated energy storage (high-density capacitor or solid-state battery) and low power circuits. The PV cell can be realized on the chip's front (CMOS) side or the back side.

Integration of solar cells on CMOS

Utrecht University's process [12] is used to fabricate the a-Si solar cell stack (Fig.2, left). Ag and ZnO:Al were deposited by RF magnetron sputtering, followed by PECVD a-Si ($T < 200^\circ\text{C}$). The ITO top electrode was sputtered. On the glass reference sample, an Au grid was thermally evaporated. Fig. 2 (right) shows the Nankai University CIGS process [13]. Mo is sputtered; an optional 10–20 nm efficiency-boosting NaF layer [8] is evaporated, followed by CIGS thermal co-evaporation at different substrate temperatures. CdS is deposited in chemical-bath; i-ZnO and Al-doped ZnO are magnetron sputtered, followed by thermal evaporation of an Ni/Al top electrode through a stainless steel shadow mask. Shadow masking is employed to prevent short circuits.

Solar cells (typically few-mm² area) were fabricated on the front or back side of functional 0.25 μm (Al backend) CMOS chips [14], 0.13 μm (Cu backend) CMOS process-control-module (PCM) chips, and on glass reference substrates, in the same run (Fig. 3 left). The finished a-Si and CIGS solar cell samples are shown in the middle and right of Fig.3, respectively.

Fig. 2: Schematic cross-section of a-Si (amorphous-silicon) solar cell on CMOS chip (left) and CIGS (Copper-Indium-Gallium-Selenide) solar cell on CMOS chip (not to scale).

Fig. 3: Left: photograph of a 10x10 cm² sample holder for solar cell deposition experiments; middle: finished samples with a-Si; right: finished samples with CIGS. For all three, A, B, C stand for the glass reference plates, 0.25 μm Al backend CMOS chips and 0.13 μm Cu backend CMOS chips, respectively. Extra additional test samples and PCMs are also included in the same run.

Integration Challenge

Several issues were tackled to get successful integration. As the substrate is changed, the **adhesion** of the solar cell's first layer required some process tuning. For CIGS a Mo thin film is normally deposited by magnetron sputtering [15]. We observed Mo delaminating from PECVD SiO₂ and SiN_x surfaces. An improved deposition recipe, utilizing DC sputtering at reduced pressure and half the deposition rate resolved the issue, passing a scotch-tape test. An adhesion layer (e.g. Ti) might be a more robust solution to maintain the standard solar cell process. The a-Si cell's bottom electrode conventionally contains silver, yielding a high internal reflection to boost efficiency. CIGS cells contain both copper and sodium. A robust diffusion barrier is required to protect the CMOS from **metal ion contamination**. PECVD SiO₂/SiN_x/SiO₂ stacks were deposited on *both sides* of the CMOS chip as diffusion barriers with total thicknesses around 800 nm. Electrical characterization confirms that these stacks function well as diffusion barriers, and have a negligible impact on CMOS device parameters (last column of Tables III, IV). The layers also protect against **plasma processing induced damage** [16][17].

The normally used **peak process temperature** of a-Si solar cells is around 275 °C. For CIGS, standard processing goes above 500 °C. Good efficiencies are however reported at 400-450 °C peak temperatures [18] as reproduced in the present work. During the CIGS deposition, the CMOS chip surface stays at the peak temperature for around 30 minutes. **Mechanical stress**, originating from thermal expansion differences between solar cell and silicon substrate, is critical in the CIGS case. Table IV shows loss of chip functionality after processing above 400 °C. The yield drops at lower temperatures in front-side integrated solar cells than in back-side integrated cells. This suggests mechanical stress, not thermal budget, as the root cause for CMOS degradation. This is confirmed by a positive functional test after a 450 °C thermal anneal (Table IV).

Solar cell characterization

Fig. 4 shows typical *J-V* curves of the solar cell on glass reference cell and on CMOS measured under AM 1.5 illumination. The derived efficiencies are listed in Table I. For both a-Si and CIGS solar cells, the on-chip solar cell efficiencies reach 5-7%, compared to an efficiency above 8% on the glass reference cell.

Depending on the last patterning steps, different CMOS chips have different surface profile amplitude (Fig. 5), which negatively impacts the CIGS PV efficiency, but not the efficiency of a-Si solar cells (Fig. 6). The root cause is the poor step coverage of CIGS thermal co-evaporation, compared to PECVD a-Si.

The crystallinity and the chemical composition [8] of the CIGS layer of the samples were measured by XRD and

XRF respectively, and the results are shown in Fig.7 and Table II. The ratio of XRD intensity of <220/204> peak over the <112> peak increases with temperature, indicating an increase in the preferred crystal orientation for higher efficiency CIGS solar cells in line with literature [19].

Fig. 4: Typical *J-V* curves of solar cells (a-Si and CIGS) under AM 1.5 illumination conditions, on glass (reference) and on CMOS.

Table I. Solar cell performance on glass reference and on CMOS.

Substrate	Efficiency	J_{sc} mA/cm ²	V_{oc} V	FF	R_s Ω cm ²	R_p Ω cm ²
a-Si on Glass	8.11%	17.1	0.86	0.56	33.0	625
a-Si on CMOS	5.19%	11.3	0.88	0.52	43.8	1324
CIGS on Glass	8.60%	26.6	0.48	0.67	2.46	378
CIGS on CMOS	7.07%	23.8	0.45	0.66	2.98	303

Fig. 5: As-fabricated different type CMOS chips' surface topography measured with a profilometer.

Fig. 6: Efficiency of a-Si:H and CIGS solar cells deposited on CMOS chips with different surface topography. The a-Si:H solar cell maintains its efficiency on a very rough surface, while the CIGS solar cell is strongly influenced by the surface topography.

Fig. 7: X-ray diffraction (XRD) data for CIGS fabricated at 400 – 450 °C.

Table II. Chemical composition by X-ray fluorescence of CIGS on various substrates and deposited at various temperatures, and the efficiency at AM1.5 illumination.

T (°C)	substrate	Cu (at.%)	In (at.%)	Ga (at.%)	Se (at.%)	Cu/(In+Ga)	Ga/(In+Ga)	Eff. (%)
	Expected	22–24	19–20	6–7	50–51	0.88–0.91	0.25–0.27	—
400	Glass	22.84	18.67	7.57	50.95	0.87	0.29	11.51
	CMOS	22.52	18.03	8.22	51.22	0.86	0.31	4.53
425	Glass	19.58	20.09	8.21	52.20	0.69	0.29	8.60
	CMOS	19.50	21.68	7.53	51.25	0.67	0.26	7.07
450	Glass	23.63	20.82	4.76	50.18	0.92	0.19	13.10
	CMOS	22.65	21.51	4.40	50.25	0.87	0.17	5.74

In the 400 °C and 425 °C fabricated CIGS solar cells there is an indication of the existence of $(\text{In}_{1-x}\text{Ga}_x)_2\text{Se}_3$ in the $\langle 112 \rangle$ and the $\langle 220/204 \rangle$ lines, attributed to a lack of thermal activation energy from the substrate [20].

Table II shows the chemical composition of CIGS on various substrates and deposited at various temperatures, and the efficiency at AM1.5 illumination. The “expected” row indicates the aimed composition [19]. In each run (i.e. deposition temperature), the element stoichiometry on glass and on CMOS is almost identical (within measurement error). The 425 °C run shows a deviating stoichiometry, resulting in a reduced efficiency on glass. The differences between efficiency obtained on glass vs. CMOS (at any temperature) are explained from topography and Mo adhesion differences.

CMOS chip functionality

Electrical characterizations have been performed on individual devices (MOS capacitor and transistor) and on integrated circuits to evaluate the CMOS compatibility of the solar cell integration.

MOS capacitors (area of $1.44 \times 10^{-6} \text{ cm}^2$, oxide thickness of 2.2 nm) and transistors (0.13 μm gate length), part of the PCM module of the 0.13 μm technology chip, were measured with a Keithley 4200 SCS. The circuit functionality of the Timepix [14] (0.25 μm CMOS) chip was measured by Pixelman software [21] connected to a MUROS2 interface [22] by a custom readout probe card.

Fig. 8: Left: C - V curves of a MOS capacitor before and after a-Si (top) and CIGS (bottom) solar cell integration on chip's frontside at 400 °C. Right: I - V curves of a NMOS transistor before and after the same post-processing. Insets show threshold voltage shift statistics of 8 transistors.

Table III. Functional testing of MOS capacitor and MOSFET for 0.13 μm (Cu backend) CMOS chips after post- processing steps (The *Front* row lists front-side integration of the cells; *Back* means backside integration).

Process Condition	< 200 °C a-Si:H	400 °C CIGS	425 °C CIGS	450 °C CIGS	450 °C CIGS (No NaF)	450 °C 30 min anneal
ΔV_{FB} (mV)	<i>Front</i>	2.0	-9.3	(no data)	-4.0	-8.6
	<i>Back</i>	1.0	-6.4	-11.8	-10.0	
ΔV_{th} (mV)	<i>Front</i>	4.7	-20.9	-39.2	-25.9	-20.4
	<i>Back</i>	-0.1	-20.7	-20.1	-24.6	
ΔS (mV/dec)	<i>Front</i>	0.08	-1.36	-1.03	-1.27	-1.23
	<i>Back</i>	0.07	-1.61	-1.40	-0.44	

Table IV. Functionality test results [14] of Timepix chip after various post-processing sequences (Terminology as in Table III). Values in the Table give the number of columns (out of 256) passing the functionality test before and after post-processing. For practical reasons the experiments were carried out on “leftover” Timepix chips with known defects.

Process Condition	< 200 °C a-Si:H	400 °C CIGS	425 °C CIGS	450 °C CIGS	450 °C CIGS (No NaF)	450 °C 30 min anneal
Digital functional column	<i>Front</i>	248→247	254→228	malfunction	malfunction	malfunction
	<i>Back</i>	(no data)	253→253	253→253	247→233	(no data)
Analog functional Column	<i>Front</i>	247→244	254→212	malfunction	malfunction	malfunction
	<i>Back</i>	(no data)	253→252	253→253	247→232	(no data)

The C - V and I - V curves of the individual devices are shown in Fig. 8, and the change in flatband voltage V_{FB} , threshold voltage V_{th} , and subthreshold swing S are summarized in Table III. The small changes in device parameters are related to the thermal budget (cf. last column) and comparable to packaging-related parameter shifts [23]. The test results of integrated circuits from the 0.25 μm technology are shown in Table IV. Yield loss occurs only when CIGS is deposited at > 400 °C on the CMOS side (front) of the chip, whether the NaF thin film is applied or not. Backside-deposited CIGS (up to 425 °C) as well as front-side integrated a-Si:H maintain full IC functionality.

Energy scavenging benchmark

Solar cells can supply 1-10 $\mu\text{W}/\text{mm}^2$ in typical indoor lighting conditions [4][24]. CMOS circuits consuming a time-averaged $\sim 1 \mu\text{W}/\text{mm}^2$ can thus be powered, e.g. the continuously operating low-power IC in [25] (down to 700 nW/mm^2) or low-duty-cycle circuits.

PV harvesting in outdoor lighting conditions outperforms other harvesting techniques by orders of magnitude when normalized per unit volume [24]. However, a comparison of monolithic CMOS-integrated solutions for general use is better made *per surface area*, because CMOS power consumption scales with chip area. Table V shows a comparison between published energy scavengers and our present PV performance. In direct sunlight, integrated solar cells offer orders of magnitude more power than known alternative scavenging solutions. Even at indoor lighting conditions, the PV approach is estimated to outperform the alternatives for energy scavenging. Power conversion losses for PV energy scavenging are relatively low [26] compared to most other energy sources as they generate a low-voltage-amplitude ac signal.

Prospects for further efficiency improvement include a-Si tandem cell concepts and CIGS bandgap tuning by varying the Ga/(In+Ga) ratio to better match the indoor spectrum.

Table V. Comparison between (presumably CMOS-compatible) energy scavengers and this work. For the vibration energy scavengers only those fitting general vibration sources [3] are included.

Scavenger	Reference	area [mm^2]	power/area ($\mu\text{W}/\text{mm}^2$)	Requirements
Integrated a-Si	This work	4	50	AM1.5 (sunlight)
Integrated CIGS	This work	27	70	AM1.5 (sunlight)
Integrated solar cell	Est. indoor, this work and [4][24]	--	1	Indoor lighting, 10% efficiency
Piezoelectric	Elfrink [27]	49	0.49	Good frequency match required
Electromagnetic	Jones [28]	99	0.37	
Electrostatic	Arakawa [29]	400	0.015	Gradient $> 5^\circ\text{C}$
Thermo-electric	Boettner [30]	1.12	0.6	
Micro-windmill	Holmes [31]	113	0.02	5 m/s wind speed

Conclusions

We conclude that both a-Si and CIGS thin-film solar cells can be integrated on CMOS. CMOS functionality is maintained both with Cu and with Al interconnect. In view of mechanical stress CIGS solar cells are preferably integrated on the chip's back side. Front side integration, which allows more straightforward interconnection, has a wider process window with a-Si cells, where plasma damage and silver contamination are the main integration concerns. For both technologies, the CMOS IC should be planarized, covered by a diffusion barrier, possibly an adhesion layer; followed by the conventional PV process flow. The single-chip integration scheme shown in this work is suitable for wafer level processing. Integrated photovoltaic energy scavenging offers high power, low manufacturing cost, a broad application range (as light is commonly available), and the advantages of a mature micro-technology.

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