Temperature Effect on Antenna Protection Strategy for Plasma-Process Induced Charging Damage

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Abstract— In this paper, the leakage current of different drain-well diodes for plasma-charging protection has been simulated at high temperature. The simulation shows that the high ambient temperature, especially during plasma deposition process, enormously enhances the efficacy of the protection diodes in protecting thin oxide. The efficacy of different diodes has been compared by simulation and experiment. Based on our discoveries, a strategic protection scheme for plasma-process induced damage (PPID) is proposed.

I. INTRODUCTION

Plasma processes are widely used in the manufacturing of VLSI devices for etching and deposition. However, it also induces charging damage to the devices. In 1989, Shone et al. proposed protection diodes as a means of avoiding wafer charging [1]. The diodes are connected in parallel to the gate providing an alternate leakage path for the plasma-induced current. Historically, junction breakdown voltage has had a lower value than gate oxide breakdown voltage and therefore, even reverse bias has been effective in protecting gates. As the thickness of the gate oxide is scaling down, the gate oxide breakdown voltage strongly decreases. It was predicted that for oxides thinner than 11nm, gated diode provides little or no protection [2]. However, later it was reported that the protection by diodes is still effective for 2.1nm– 3.2nm thin gate oxide FETs [3]. Even reverse diodes with high junction breakdown voltage can still offer some charging protection. This protection is due to their reverse bias leakage and can be adequate if they have a large enough area [4].

Apparently the protection diodes are more capable than what was anticipated. One of the explanations

of the enhancement of the efficacy of the protection diode is the presence of light during plasma processing. During the plasma process the diode reverse leakage current is enhanced by a photon generated current resulting from the light emission of the plasma [4].

However, the light effect is strongly affected by the metal on the top of the diode. If the diode is shielded from plasma illumination by metal, the reverse current of the diode rapidly decrease by more than one order of magnitude [5]. As the integration density of the VLSI technology continuously increases, the metal layers fabricated in the back-end processes increases from 3 layers to 5 layers, and even more. Furthermore, tiling of metal will block even more light, which makes it more likely that the protection diodes are shielded by the metal and there is no to plasma-assisted photo-conduction in these diodes.

In this paper, we report for the first time that the enhancement of the efficacy of diodes in protecting very thin gate oxides is primarily due to the high ambient temperature during the plasma processes. During the plasma etching the wafers can be heated to about 70 °C and during the plasma depositions processes, the ambient temperature is even 400 °C. Recently more and more research groups report the plasma damage is mainly due to the deposition process [6]–[8]. Therefore, studying the diode characteristics at high temperature becomes important for plasma damage protection prediction.

Since it is not possible in practice to measure the diode characteristics at 400 °C, a commercial simulator called SILVACO is used to investigate the diode behavior at elevated temperatures. The efficacy of different diodes is also compared under

both positive and negative voltage charging. Based on our discoveries, a strategic protection scheme for PPID is proposed.

II. EXPERIMENTAL DETAILS

The test structures have been subjected to an experimental 0.18 μm CMOS backend-of-line process. The test structures are small transistors with minimum channel length and 3.5nm gate oxide thickness. The charging tester consists of a MOS transistor with a finger-shaped antenna connected to the gate. A protection diode is connected to gate at the same level as the antenna in order to test its protection efficacy, as shown in figure 1.

Figure 1: Schematic layout of tester with metal2 finger antenna. The protection structure is connected on the same level of antenna.

In our study, the test structures are protected by different drain-well diodes. The schematic view of the diode protections is shown in figure 2. The antennas of all test structures with protection at the antenna level are finger antennas with narrow spacing (0.32 μm). Since the leakage current of double sided protection “diode”, or floating base PNP protections, is negligible at room temperature, it can be used both for pMOSFET and nMOSFET. Considering the working potential of the MOSFET, n+/psub and p+/nwell, so called single diode can only be used for nMOSFET and pMOSFET respectively.

Moreover, antenna test structures with various spacing between the fingers of the antennas (from 0.32 μm to 4 μm) have been designed, in order to investigate the electron shading (ES) effect and the polarity of the plasma charging.

Figure 2: Schematic overview of different protection schemes.

The IV characteristic of different diode under positive as well as negative voltage charging is compared by simulating. The antenna testers protected by different diodes have been measured and analyzed. An antenna tester is considered to fail when the leakage current ($I_{g,leak}$) measured through its gate oxide exceeds 0.1nA, indicating that (soft or hard) breakdown occurred. The failure fraction of the antenna testers protected by different diodes has been compared.

III. RESULTS AND DISCUSSION

A Simulation results

The saturation current I_s doubles for about every 10 °C increase in diode's temperature. The temperature dependence is determined by:

$$I_s(T_1) = I_s(T_0) \left[\frac{T_1}{T_0} \right]^{2/N} \exp \left[\frac{E_g q (T_1 - T_0)}{Nk(T_1 - T_0)} \right]$$

where N is the emission coefficient, which is a model parameter, k is Boltzmann's constant, q is the electronic charge, E_g is the energy gap which is a model parameter. The temperature parameter is an exponential factor. The leakage current of the double sided diode is enormously influenced by the temperature, as shown in figure 3 and figure 4. By increasing the temperature by 100 degrees, the leakage current is about 1000 times higher.

Figure 3: Simulation of leakage current of the double sided diode under negative bias at different temperatures (°C).

Figure 4: The leakage current of the double sided diode is evaluated by high temperature. Note that the current values presented in the figure are absolute values. The bias voltage is $\pm 0.75V$.

The IV characteristic of different diodes under both positive charge and negative charge conditions are compared by simulation. The results are presented in figure 5 and figure 6.

Figure 5: Simulations of the single diode and double sided diode current at 400 °C under positive bias.

Figure 6: Simulations of the single diode and double sided diode current at 400 °C under negative bias.

The double sided diode shows better efficacy in the case the gate of the MOSFET is positively charged. The leakage current of double sided diode is 100 times higher than that of reverse biased n+/p single diode. Under negative charging, the n+/p single diode has higher current because it is forward biased.

B. Experimental results

The antenna testers protected by different diodes have been measured. In figure 7, the $I_{g,leak}$ of the antenna testers protected by different diodes has been compared.

Figure 7: Distribution of the gate leakage current.

The failed fraction of the antenna testers protected by different diodes has been compared, as presented in table 1 and table 2.

Table 1 Failed fraction (%) of NMOS transistor with protection diode at antenna level

Antenna	floating n-well diode	n+/p diode
Poly	0.20	11.60
LIL	2.45	10.98
M2	0.25	2.45

LIL: Local interconnect level.

Double sided diode: p+/nwell/psub

Table 2 Failed fraction (%) of PMOS transistor with protection diode at antenna level

Antenna	floating n-well diode	n+/p diode
LIL	0.11	5.69

All the results show that the antenna structures protected by double sided diode fail less than that protected by n+/p single diode.

The failure fractions of antenna test structures with varying inter-finger spacing are compared in figure 8. It was reported that dense finger antennas collect positive charging and the damage increases with

the decrease of the inter-line spacing due to ES effect; while the sparse finger antennas collect negative charging and the damage increases with the increase of the inter-line spacing due to extended ES effect [7][9]. In figure 8 it is shown that the failure fraction of antenna testers with inter-line spacing narrower than $1\mu\text{m}$ increases with the decrease of the inter-line spacing, indicating the antennas collect positive charging; while the failure fraction of antenna testers with inter-line spacing wider than $2\mu\text{m}$ increases with the increase of the inter-line spacing, indicating the antennas collect positive charging. The turn over trend can be apparently observed in figure 8.

Figure 8: Dependence of damage on the spacing between fingers of the antenna.

C Discussion of the correlation between the simulation results and experimental results

Since the antennas of all test structures with protection on the antenna level are finger antennas with narrow spacing ($0.32\mu\text{m}$), the protection diode is under positive voltage charging. According to the simulation results, the double sided diode provides better protection than n+/p single diode under positive bias. Therefore, the antenna structures protected by double sided diode show much less fail than that protected by single n+/p diode. The experimental results agree with the simulation results well.

IV. CONCLUSIONS

Our work shows that the high ambient temperature during the plasma processes enormously enhanced the efficacy of both single and double diodes in protecting very thin gate oxides. The best protection scheme depends on the specific charging polarity and temperature. For plasma deposition charging at high temperature, the double sided diode is sufficient, whereas for

plasma etching charging at low temperature, a single diode is the best. Considering the fact that plasma deposition is gaining importance, double sided diodes are considered the best choice in most cases.

ACKNOWLEDGMENTS

The authors would like to thank the Dutch Technology Foundation (STW) for sponsoring this research. The authors are also thankful to Jay Kolhatkar, Andre Hof, and Rien van Leeuwen for their fruitful discussion.

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