23.2 UMTV: a Single Chip TV Receiver for PDAs, PCs, and Cell Phones

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In this paper, a single-chip TV receiver called universal mobile television (UMTV) is presented. UMTV requires no external components and has a power dissipation of 150mW. It is a multi-standard receiver for all analog and digital TV standards. The device needs a single supply of 3V, a 3-wire interface to a microcontroller, and an antenna connection. Its outputs are composite video, low-IF, and mono sound. The signal processing itself is performed in dedicated analog hardware but all control and alignment functions are realized in the digital domain.

There are several silicon tuners available [1-3], but they are dedicated to the digital set-top box market. Due to their high power consumption they are not attractive for portable use. Furthermore, they still require more than 15 external components like external SAW filters for channel selectivity, a tunable resonator, several external varicaps for the RF oscillator (LO), and multiple tunable RF antenna circuits. For demodulation and sound reception additional ICs and external components are required which are different depending on the TV standard [4].

In mobile phones with portable TV applications, advanced technology is used to miniaturize the normal tuner cans. The smallest reported size is 2400mm³ (20mm×30mm×3mm) [5]. Its power consumption is 900mW. The proposed solution has a size of 45mm³ (7mm×7mm×0.9mm) and consumes 150mW. In the design of UMTV the following design targets are set: high sensitivity (low NF), low power dissipation, high harmonic suppression, and multi-standard operation (PAL, NTSC, SECAM, DVB-H, etc.).

Figure 23.2.1 shows the architecture of the UMTV chip. No front-end antenna filter is required. The signal processing starts with a selective tunable LNA. It plays a crucial role in obtaining the targets of high sensitivity and low power. The principle of the selective LNA is illustrated in Fig. 23.2.2. The antenna signal is converted from voltage to current. This current is injected in the loop of an inverting amplifier and two LPFs. The cut-off frequency of the LPFs can be controlled with current I₂. This will concurrently change the R₀ of transistors T1, T2, and T3. The resistors R act as RF blocking devices. The positive feedback with a phase shift of approximately 360° in the loop will be achieved at different frequencies depending on I₂. By controlling the total gain in the loop, sufficient phase margin at gain>1 is obtained to keep the loop stable. By making more phase shift in the loop (e.g., by increasing the order of the LPF) the Q-factor will be higher and the shape of the curve will change. Also, by changing the ratio of C1, C2, and C3 the Q-factor can be controlled. For an LNA to keep the noise at a low level, it is important to keep component count as low as possible. This wideband tunable LNA is designed in silicon with only 5 transistors and no dominant resistors in the signal path. The LNA measurement results are given in Fig. 23.2.4. Frequency response for various tuning currents is shown. The inset in Fig. 23.2.4 shows that the NF is always better than 9dB over the total VHF and UHF band (40MHz to 900MHz). This NF is measured at the end of the IF filter/amplifier, so it includes the LNA itself, the mixer construction for suppression of the 3rd and 5th harmonics, the active-IF filter, and the IF amplifier. The suppression of the 3rd, 5th, and the 7th harmonics is better than 60dB, 80dB and 50dB over the whole TV band. The LNA draws a total current of 2mA at 40MHz and 3mA at 900MHz, respectively. The supply range is 2.7V to 5V.

Another crucial block of the UMTV chip is the LO. It is a quadrature oscillator with a tuning range from 420 to 900MHz. The principle of the integrated digital capacitance bank is similar to

the multi-band LC oscillator used in the FM radio [6], but the tuning range is improved and it is a polyphase oscillator. One section of the oscillator is shown in Fig. 23.2.3. The resonator of each section makes use of bond-wire inductors, which are together with the capacitor bank connected to i_{bank}. Unlike most I/Q oscillators no cross-coupled pair (thus eliminating a self-oscillation mode) is present within each section, making the circuit very robust against multi-mode oscillations. Transistors Q7 and Q8 together with their external (and internal) base resistors, implement active inductors that tune the total phase shift of each section close to 90°, thus realizing operation at the resonance frequency of the LC-tank circuit where the Q-factor is maximum.

A digital AFC system compensates temperature drift. Dividers and a MUX are used to generate a frequency range from 25 to 900MHz. The large spread of the bond wires can be coped with, because the tuning range of the oscillator is more than a factor of 2, and the divider chain is used to generate all the lower frequencies. The spread of the bond wires will only change the maximum oscillation frequency. By designing a 15% higher maximum frequency, a spread of ~30% in bond-wire length can be accommodated.

After down-conversion, a fully integrated programmable high precision (FPHP) filter with a dynamic image suppression (DIS) system implements the IF filter. One filter section contains 3 controllable transconductance circuits and a capacitive load; one for controlling the center frequency, one for the bandwidth, and one for the gain. The circuit is resistorless and the only spread is in the G_m and the capacitor. The IF filter allows accurate tracking of various FPHP filters by relative G_m-C matching of filter sections, in which G_m is the transconductance of the OTAs and C the capacitance of the capacitor within the respective filter sections. Calibration of the FPHP filters against IC inherent spread and parasitic effects is realized by a single calibrated master filter device with a frequency calibration reference signal for frequency scaling and a gain calibration reference signal.

The IF output can be used for a low-IF OFDM demodulator chip (see the output in Fig. 23.2.1). For analog TV reception, a split filter separates sound and video. Fig. 23.2.5 shows the measured frequency response of the 12th-order FPHP filter with a DIS system. The image suppression is 60dB. The significance of the DIS system is that good reception can be realized with low-IF systems even if a signal is transmitted at the image channel.

The IF-video signals are demodulated with a wideband PLL demodulator [7] that is followed by an anti-aliasing filter to suppress spurious signals. The sound is up-converted to the original inter-carrier sound frequencies. Therefore, external sound demodulators can be used. For on-chip demodulation of the sound, a demodulation concept similar to the no external component FM receiver [7] is extended with synchronous AM demodulation. The receiver can be tuned to all different sound carrier frequencies.

A short list of specifications of the UMTV IC is given in Fig. 23.2.6. The IC is realized in a low-cost 8GHz f_T BiCMOS process. The die micrograph (size 5×5mm²) is shown in Fig. 23.2.7.

References:

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Figure 23.2.1: UMTV block diagram.

Figure 23.2.2: Schematic diagram of the tunable LNA.

Figure 23.2.3: One section of the I/Q LO.

Figure 23.2.4: Measured Front end selectivity and NF at IF.

Figure 23.2.5: Dynamic image suppression (DIS).

Parameter	Value
External components	0
Technology	BiCMOS (8 GHz f_T)
Supply voltage	3 Volt
Supply current	50 mA
Chip size	25 mm ²
Total volume	45 mm ³
Noise figure	< 9 dB
1dB gain compression	81 dBuV
Osc. tuning range	45 – 900 MHz
Osc tuning resolution	250 kHz
Osc. Phase noise	-125 dBc/Hz @ 1MHz
IF center tunable	4 – 8MHz
IF bandwidth tunable	2 – 8MHz
Sound traps	N and N+1
PLL lock range	+/- 1 MHz
Video output	1 Vpp (1 kΩ)
Sound output	100 mVp

Figure 23.2.6: UMTV short specification list.

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Figure 23.2.7: Die micrograph of the UMTV chip.