A 3 Gb/s optical detector standard 0.18um CMOS

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Abstract - **This paper presents a monolithic optical detector, consisting of an integrated photodiode and a pre-amplifier in a standard 0.18μm CMOS technology. 3Gb/s data-rate was achieved at λ=850nm with an average optical power of 25 μW and BER10^{-11}. This data-rate is over half an order of magnitude higher than that of current state-of-the-art optical detectors in standard CMOS.**

High speed operation is achieved without reducing circuit responsivity by using an inherently robust analog equalizer that compensates (in gain and phase) for the photodiode roll-off in the range from 1 MHz to 1 GHz. The presented solution is applicable to various photodiode structures, wavelengths and CMOS generations.

Keywords – **Optical communications, CMOS, equalizer, robust design, high-speed**

I. INTRODUCTION

For cost, size, and assembly reasons monolithically integrated CMOS optical detectors are preferred in (very) short-range optical data communication [1,2] and in optical storage systems [3]. Another significant advantage of an integrated photodiode is that high interconnect capacitances and inductances are avoided. Furthermore many parallel optical receivers can be placed on a single chip at low cost, opening the door to optical interconect. However the serious disadvantage of photodiodes integrated in standard CMOS is the low speed, reported up to 700Mb/s [2].

In this work we present a fully integrated photodiode with pre-amplifier for bit-rates up to 3 Gb/s in standard 0.18um CMOS: which is over half an order of magnitude speed-increase.

For gigabit fiber Ethernet [5] 850 nm light is used. For photodiodes in modern CMOS at this wavelength the majority of the generated carriers slowly diffuse towards junctions, resulting in a physical (intrinsic) bandwidth of the photodiodes in the low MHz range. This effect typically forms the speed bottleneck in integrated CMOS optical receivers. One solution [1,2] achieves 700Mb/s thanks to cancelling the effect of the slowly diffusing carriers by subtraction of two diode responses; this however results in lower responsivity and hence lower sensitivity. We present a solution for high-speed data communication with integrated photodiodes *without* reducing circuit responsivity, achieving 3 Gb/s data-rate by exploiting an analog equalizer.

II. BANDWIDTH LIMITATIONS IN CMOS

A minimal-distance finger nwell/p-substrate diode, see Figure 1, is used as the optical detector. Its overall response consists of three current contributions: two slow diffusion responses (in the nwell and in the p-substrate) and one fast drift current response.

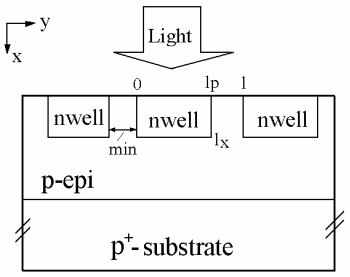

Figure. 1. Cross-section of the finger nwell/p-substrate photodiode in standard CMOS technology.

The latter is frequency-independent up to frequencies in the GHz range. The typically dominant substrate current has a bandwidth that is several orders of magnitude lower than the bandwidths of the other current components: this substrate current component limits the overall photodiode bandwidth.

The overall *intrinsic* photodiode response shows a slow decay starting in the low MHz range, due to the combination of the three current components. It can be shown [6] that the roll-off in the overall photocurrent response is only about 5 dB/decade for frequencies between roughly 10 MHz and the lower GHz range. In the low-GHz range, the roll-off is even lower (<4dB/decade) because then the fast depletion region response dominates the overall photocurrent. So the signals from the photodiode are low bandwidth (MHz range), but still relatively strong at very high frequencies (GHz range).

III. A SOLUTION: EQUALIZATION

Therefore we introduce an analog equalizer that compensates (in gain and phase) for the diode photocurrent roll-off in the range from 1 MHz to 1 GHz. As a result, 3Gb/s data-rate with a low bit-error rate (BER<10^{-11}) is achieved.

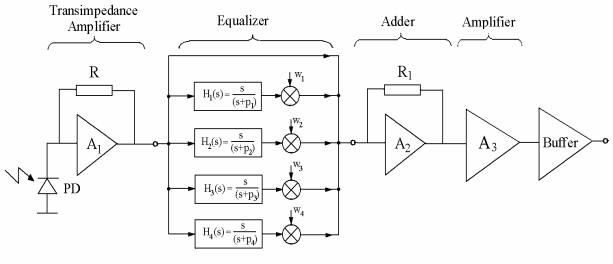

Figure. 2. Block-diagram of integrated photodiode and preamplifier system using the analog equalizer.

The presented analog equalizer is designed to compensate the frequency characteristic of the applied photodiode from DC to 1GHz, using 4 high-pass filters. Although a parallel configuration as shown in figure 2 is optimum w.r.t. equalization, the current implementation uses 3 parallel high pass filter sections (R_2C_2, R_3C_3 and R_4C_4) and one HF peaking section (with C_1) for area and power efficiency reasons. With the circuit of figure 3 it is fairly straight-forward to compensate the diode-characteristic for frequencies where the roll-off is low (for ≤5dB/decade).

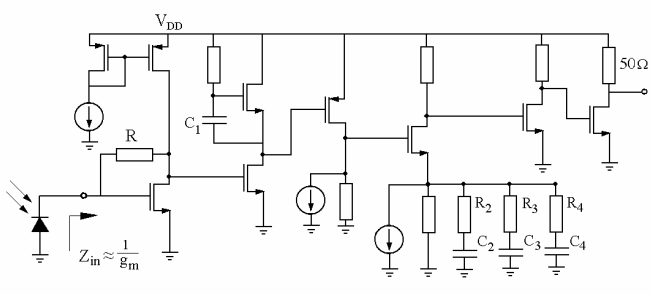

Figure 3. Circuit topology of the preamplifier including the analog equalizer.

This is for frequencies up to $f_{3dBdrift}$=0.4 v_s/W, where v_s is saturation velocity of charge carriers and W is a depletion region depth. For 0.18 μm CMOS, this frequency is about 8 GHz.

IV. ROBUSTNESS

Important in the design of equalizers is spread both on the characteristic to be compensated and on the equalizer itself. Due to the low roll-off of the photodiode the robustness against spread is high, which is conformed by Monte-Carlo simulations including +/- 20% component spread in the equalizer: only 10% decrease in the data eye amplitude results. Hence adaptive equalization is not required: the system is inherently robust. Figure 4 shows the simulated pulse response with and without equalization and with component spread.

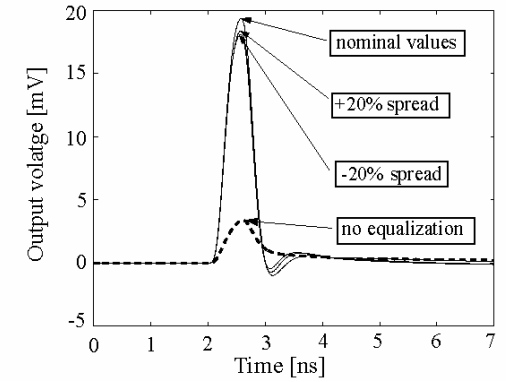

Figure 4. Simulated time responses of the circuit without the equalizer and with the equalizer with its nominal values and ± 20% spread in the component values.

The current design is optimized for 850 nm light. For shorter light wavelengths, the photodiode bandwidth is higher but shows a similar low roll-off. Also then, the application of an analog equalizer increases the diode bandwidth

considerably, with the equalization required over a smaller frequency range. A similar result holds for other CMOS generations.

V. MEASUREMENT RESULTS

Apart from the intrinsic bandwidth of the diode and the equalization of its response, also the electrical bandwidth of the diode and the pre-amplifier are important. Usually this bandwidth is determined by the diode and interconnect capacitance in combination with the pre-amplifier's input impedance. For our system the capacitance is dominated by the photodiode capacitance of roughly 1.3pF, requiring an input resistance of the TIA (see figure 2) below 50 Ω for 3Gb/s data rates; an LNA-like circuit is used for the TIA.

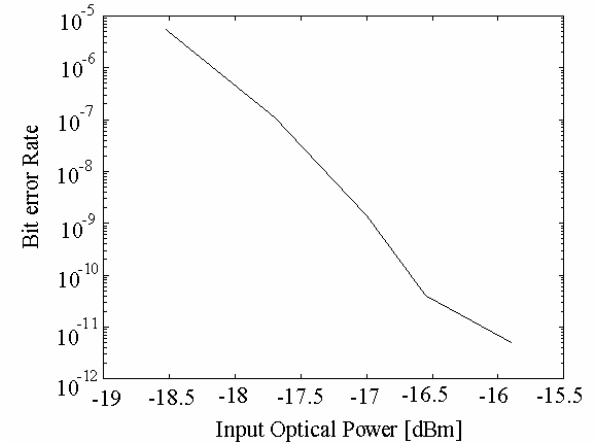

Figure 5. Bit-error rate vs. input optical power

Important for the BER of optical systems is the signal-to-noise ratio (SNR). With the proposed circuit, the responsivity (signal level) of the photodiode is maximal since the *total* photocurrent is amplified. However, the equalizer boosts also the gain for high frequency noise thereby degrading the SNR. The total noise in the circuit is dominated by the TIA (~75%), while the equalizer's frequency response is band-limited to maximize the SNR [4]. Then, with approximately 60% more photocurrent available in comparison with [1,2], for the same SNR more than 4 times higher data-rates are achieved. Figure 5 shows the BER as a function of the optical power and With respect to conventional CMOS detectors a few orders higher datarates are achieved.

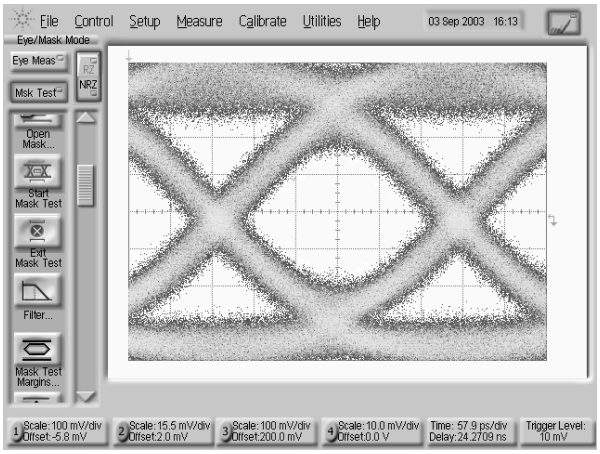

Figure 6. The eye diagram of the equalizer output with 2 Gb/s PRBS input signal.

The dimensions are 145×305 μm^2. The photodiode size is 50×50 μm^2, corresponding to a multimode fiber's core size. The sensitivity is comparable to [1,2]. An eye diagram measured at 3 Gb/s and 2^{31}-1 PRBS input signal for -19.6dBm input power (22μW peak-peak) is shown in Figure 6. The overall transimpedance is 4500 Ω. Power consumption with 1.8V supply voltage is 34mW + 16mW for the 50 Ω output buffer for evaluation.

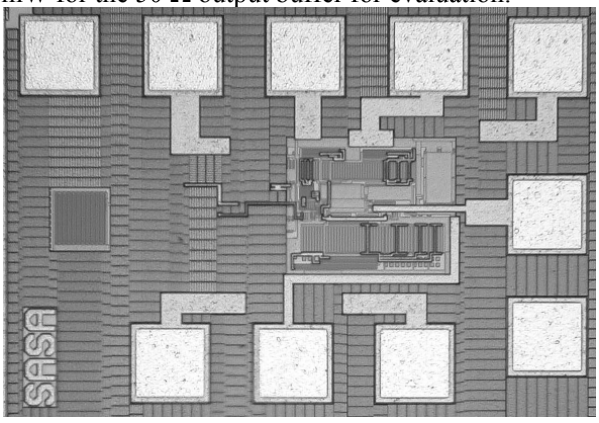

Figure 7. Chip micrograph of the integrated photodiode and pre- amplifier with an analog equalizer in standard technology.

The chip micrograph is shown in Figure 7.

VI. CONCLUSIONS

This paper presents an optical detector architecture with an analog equalizer that increases the bandwidth of the state of the art CMOS detectors by a factor of 4 for λ=850 nm, without reducing responsivity. Adaptive equalization in the proposed architecture is not required. A 3 Gb/s data-rate is achieved with 25μW light input power and BER<10^{-11}. With respect to conventional CMOS detectors almost three orders of magnitude higher data-rates are achieved.

The high-speed optical detector with an analog equalizer is very robust. Firstly, it was shown that due to the low roll-off of the photodiode characteristics, the robustness against spread is high. Secondly, the change in temperature results in a very small change much in the diffusion coefficient as well as the lifetime of the minority carriers. therefore, robustness on the temperature is high too.

VII. REFERENCES

[1] J.Genoe et al., “Calculation of the current response of the spatially modulated light CMOS detectors”', IEEE Tr. El. Dev., vol. 48, No. 9, pp. 1892-1902, 2001.

[2] C. Rooman et.al, "Inter-chip optical interconnects using imaging fiber bundles and integrated CMOS detectors", ECOC'01, pp. 296-297

[3] G.W.de Jong et al., "A DC-to-250MHz Current Pre-Amplifier with Integrated Photo-Diodes in Standard CBiMOS, for Optical-Storage Systems", ISSCC 2002, s21.8

[4] P.Amini and O.Shoaei:"A low-power gigabit Ethernet analog equalizer", ISCAS 2001, pp 176-179

[5] IEEE 10 Gigabit Ethernet Standard 802.3ae.

[6] S. Radovanovic et al."Physical and electrical bandwidths of integrated photodiodes in standard CMOS technology", submitted to EDSSC2003