Record RF performance of standard 90 nm CMOS technology

L.F. Tiemeijer, R.J. Havens, R. de Kort, A.J. Scholten, R. van Langevelde, D.B.M. Klaassen,
G.T. Sasse[1], Y. Bouttement*, C. Petot*, S. Bardy*, D. Gloria[2], P. Scheer[2], S. Boret[2],
B. Van Haaren[2], C. Clement[2], J-F. Larchanche[2], I-S. Lim[3a], A. Zlotnicka[3a], A. Duvallet[3b]

Philips Research Laboratories, Eindhoven, The Netherlands, *Philips Semiconductors, Caen, France,
[1]Mesa+ Research Institute, University of Twente, The Netherlands, [2]STMicroelectronics, Central R&D,
Q&TPS Lab., Crolles, France, [3]Freescale Semiconductor Inc., [a]Tempe, [b]Austin, U.S.A.

Abstract

We have optimized 3 key RF devices realized in standard logic 90 nm CMOS technology and report a record performance in terms of n-MOS maximum oscillation frequency f_{max} (280 GHz), varactor tuning range and varactor and inductor quality factor.

Introduction

For the 90 nm CMOS technology node a cut-off frequency f_T as high as 150 GHz [1-4] has been reported for the nominal n-MOS device. In this paper we describe optimized device layouts which on top of that enable a record performance in terms of n-MOS maximum oscillation frequency f_{max}, varactor tuning range and varactor and standard logic back-end inductor quality factor, which makes this technology node extremely suitable to realize highly integrated mixed mode RF/Analog/Digital system on a chip (SOC) applications.

90 nm CMOS technology

The Crolles II Alliance 90 nm dual V_T, dual gate oxide CMOS process features 1.0 Volt 16Å GP and 1.2 Volt 21Å LP "thin" oxide devices with nominal physical gatelengths of 65 and 83 nm, respectively, and a choice of 1.8 Volt 28Å, 2.5 Volt 50Å and 3.3 Volt 65Å "thick" second gate oxide devices. On top of that various resistors, MIM and MOM capacitors, diodes, bipolars and SRAM devices are supported. Cobalt silicide is used on the junction and the polysilicon gates, reducing the gate sheet resistance to about 9 Ω/square. The Cobalt silicide-polysilicon interface resistance [16] is less than 5 $\Omega\mu m^2$. A low-k (ϵ_r =2.9) dielectric and dual Damascene copper backend with up to 9 levels of metal, the top two with a thicknesses of 0.9 μm completes the package.

n-MOS transistors

Fig. 1 shows the layout of the (triple-well) n-MOS unit cell. As before [5], our proven concept was used, where each unit cell contains a number of parallel gate fingers contacted from both sides to minimize the gate resistance and is surrounded by a ring of well contacts at minimum design rule to minimize the substrate resistances. To comply with the electro migration design rules the source and drain interconnect is made wider than the minimum design rule and realized in the metal levels 2, 3, and 4. For characterization, several of these unit cells are placed in parallel to achieve a total width of 120 μm. Figs. 2 and 3 illustrate the standard extraction of the RF figures of merit f_T and f_{max} from measurements of the current gain H21 and Mason's gain (U), taken up to 110 GHz, where all interconnect parasitics have been de-embedded using a "simple-open/short/dedicated-open" version of [17]. The f_T and f_{max} values were extracted at the bias condition providing maximum g_m, (here V_{ds}=0.9V and V_{gs}=0.85V). Comparing devices differing in drawn gatelength, finger width and oxide thickness, as expected [10], f_T only scales with the physical gatelength and shows values in line with literature [1-9] (fig. 4). A record f_{max} of 280 GHz is obtained when the effective gate resistance is minimised using a finger width of only 2μm (fig. 5,17). The important [18] ratio C_{gin}/C_{Miller} is 3.5 for these devices. When the local interconnect shown in fig. 1 is included in the measurements to mimic the way the n-MOS device is used in actual circuits, f_T is reduced much more than f_{max} (fig. 6). The intrinsic device behaviour is generally quite well captured by the scalable compact model described in [10].

Differential varactors

Figs. 7 and 8 show the layout and simplified equivalent circuit of the differential n^+-nwell varactor device. Instead of using STI [11], for which device simulations showed that this would lead to a considerable increase in series resistance, the LDD implant is blocked to improve the tuning range. To further avoid tuning range degradation due to excessive interconnect capacitances, the alternating gate fingers are only contacted from one side. Since only the resistances Rv are seen in differential operation a significant gain in quality factor can be obtained by omitting the well contacts between the gate fingers and positioning the alternating gates closer to each other. The impact of the oxide thickness on capacitance tuning is stronger than reported in [12] (fig. 9). For an identical layout we see a 6-fold (from 35fF/V to 210fF/V) increase in the peak tuning sensitivity going from a thick oxide to the thin 16Å oxide. As

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shown in fig. 10, and contrary to [3], the capacitance is flat with frequency, whereas Q decreases with frequency, in line with the equivalent circuit of fig. 8. Apparently down to the 16Å GP oxide device gate leakage does not adversely affect the varactor performance. Attractive combinations of Q-factor and tuning range were obtained for all oxide thicknesses studied as illustrated in figs. 11, 12 and 18. The varactor Q-factors show a strong dependence on gate finger width (fig. 13). At elevated temperatures these Q-factors were seen to decrease due to an increase of the resistances Rv (fig. 8). Since these resistances represent the sum of the polysilicon gate resistance with a temperature coefficient (TC) of 0.3%/°C and a few fairly temperature independent contributions coming from the rest of the device, the overall TC of the varactor Q-factor varies with finger width from 0.1 to 0.3%/°C (solid lines in fig. 13). These TC's are two times less than those reported in [19].

Differential inductors

Fig. 14 shows the differential inductor layout. These inductors employ the metal levels 5, 6 and 7 in parallel to achieve a low resistance and have a polysilicon patterned ground shield [13] to prevent Q-factor degradation due to capacitive coupling to the lossy substrate. Results obtained for a set of 4 inductors with low frequency target inductance values of 1, 2, 4 and 8 nH, realized employing 2, 3, 4, or 5 7.5 to 9 μm wide turns at 2.5 μm spacing, resulting in outer diameters of 165, 170, 205 and 260 μm, respectively, are given in figs. 15 and 16. Their differential peak quality factors range from 13 to 24. Typically their measured inductances, resonance frequencies and Q-factors agree within 1, 3 and 5%, respectively, of the values predicted by our compact inductor model [13]. At elevated temperatures the inductor Q-factors decrease due to the increase of the metalization resistance. However since this also increases the corner frequency for current crowding [13], the overall TC of the inductor peak Q-factor is less than the 0.3%/°C of the back-end metallization.

Benchmarking and Conclusions

We have characterized 3 key RF devices realized in standard 90 nm CMOS technology and demonstrated record performance (figs. 17, 18 and 19) using optimized layouts. For the nominal n-MOS transistors reported in this work we achieve a record f_{max} of 280 GHz by minimising the effective gate resistance. This value is about twice the f_T (150 GHz), and significantly better than literature (fig. 17). For the varactors we were able to combine attractive tuning ratio's of 1:3 to 1:5 with high tuning sensitivities and Q-factors which are almost a factor of 3 better than literature. For the inductors realized in the standard logic back-end process we show a considerably enhanced performance compared to what has been reported before, approaching quality factors previously only seen in special thick metal back-end processes [14]. The combination of these devices yields an overall RF performance for our 90 nm RF technology that is the best reported so-far in literature.

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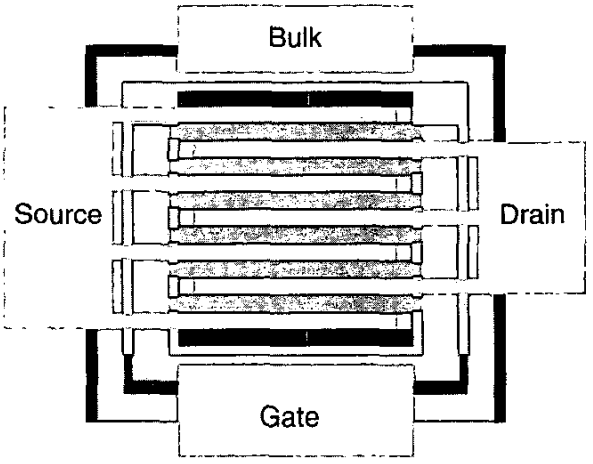

Figure 1: Layout of the NMOS device. The gate fingers are contacted from both sides. A ring of p-well contacts at minimum design rule minimises the substrate resistances. Visible layers from dark to light: OD, poly, M1, M2.

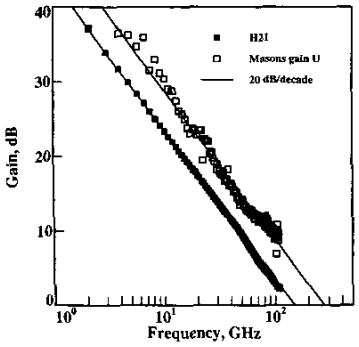

Figure 2: H21 and Mason's gain for a nominal 16 Å GP device with 2 μm finger width measured at V_{ds}=0.9V and V_{gs}=0.85V (max. g_m).

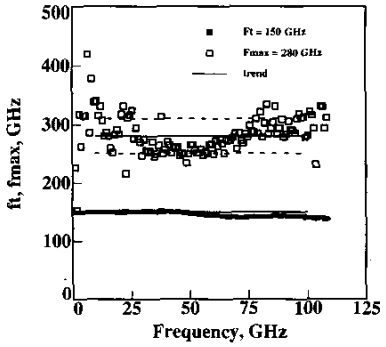

Figure 3: f_T (150 GHz) and f_{max} (280 $\pm$ 30 GHz) values obtained extrapolating the H21 and Mason's gain data of fig. 2 with -20 dB/decade.

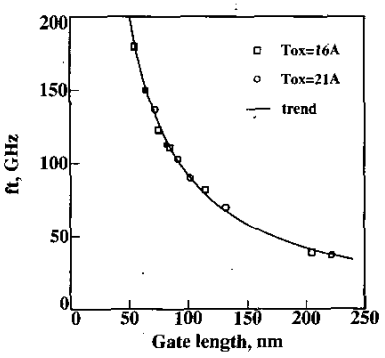

Figure 4: Cut-off frequency f_T versus physical gatelength for both the LP and GP devices. The solid symbols denote the nominal gatelength devices.

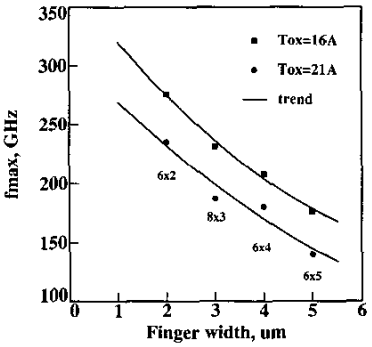

Figure 5: Maximum oscillation frequency f_{max} versus finger width for both the nominal LP (Lg=83nm) and GP (Lg=65nm) devices.

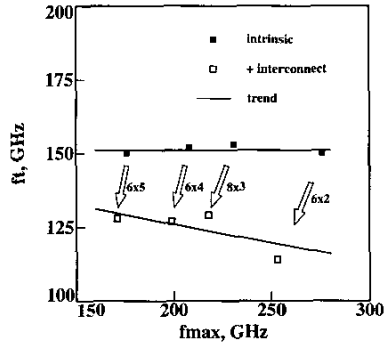

Figure 6: Impact of local interconnect on f_T and f_{max} for different finger widths for the nominal GP devices. The lines serve to reflect the trend.

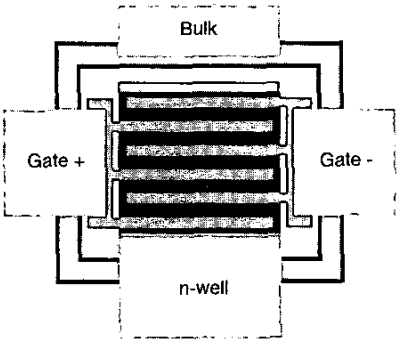

Figure 7: Layout of the differential varactor device. Gate fingers are only contacted from one side. Visible layers from dark to light: OD, poly, M1, M2.

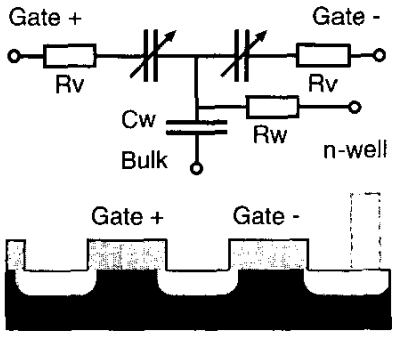

Figure 8: Simplified circuit and cross-section of the differential varactor. The resistance Rw is not seen in differential operation.

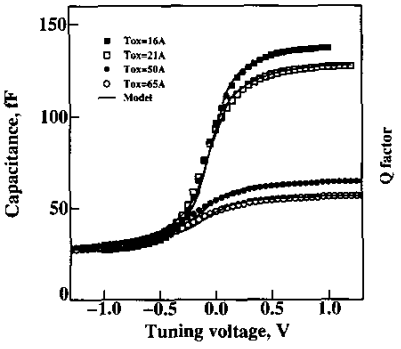

Figure 9: Impact of oxide thickness on tuning for devices with 32 280 nm x 5 μm fingers. Lines: varactor model (unpublished).

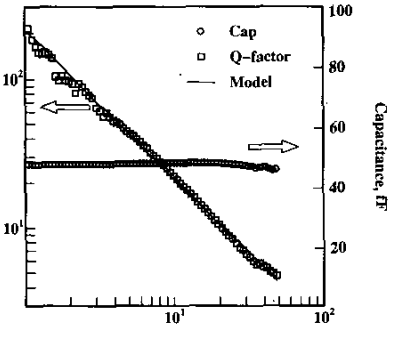

Figure 10: Capacitance and quality factor of a 16 Å gate oxide 2 x 32 x 65 nm x 2.5 μm varactor measured at V_T=0V. The line reflects the circuit of fig. 8.

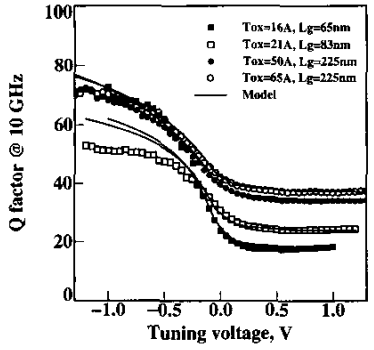

Figure 11: Quality factor measured at 10 GHz versus tuning voltage for structures containing two cells in parallel each having 32 fingers of 2.5 μm width.

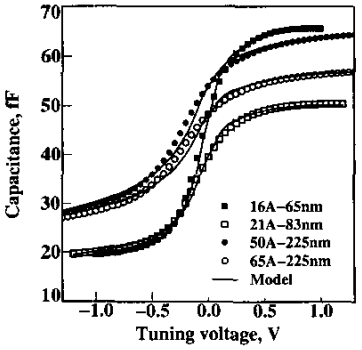

Figure 12: Capacitance at 10 GHz versus tuning voltage for the devices of fig. 11. A trade-off between tuning sensitivity and minimum Q-factor is seen.

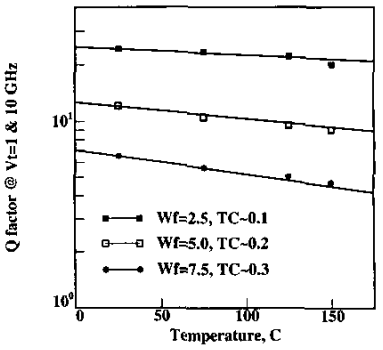

Figure 13: Quality factor measured at V_T=1V and 10 GHz versus temperature for 21 Å gate oxide Lg=83 nm devices of different finger width.

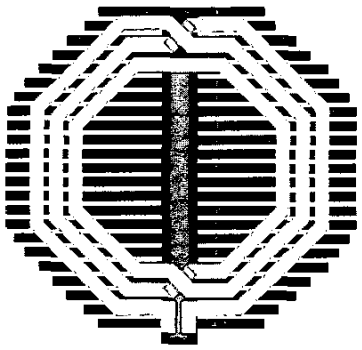

Figure 14: Differential inductor layout. A polysilicon ground shield reduces substrate loss. Visible layers from dark to light: poly, M2, M5, M7.

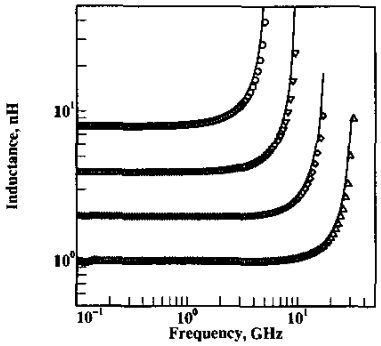

Figure 15: Inductance versus frequency. The solid lines are predicted using the compact model of [11]. Excellent agreement is seen.

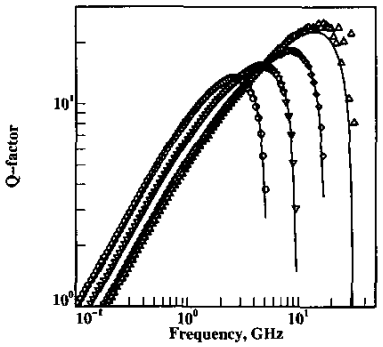

Figure 16: Differential quality factor versus frequency. The solid lines are predicted using the compact model of [11]. Excellent agreement is seen.

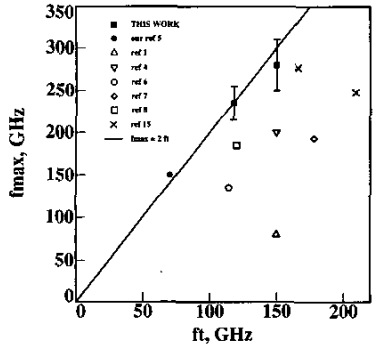

Figure 17: Reported NMOS device maximum oscillation frequency f_{max} versus cut-off frequency f_T. Our devices have f_{max} about twice f_T.

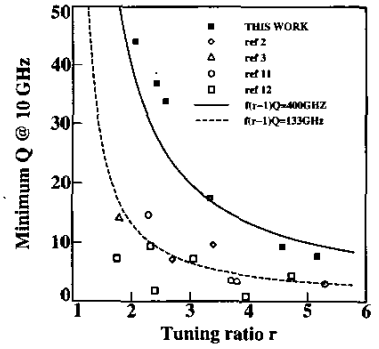

Figure 18: Reported varactor device minimum Q-factor at/translated to 10 GHz versus maximum tuning ratio r. Trendlines reflect observed trade-offs.

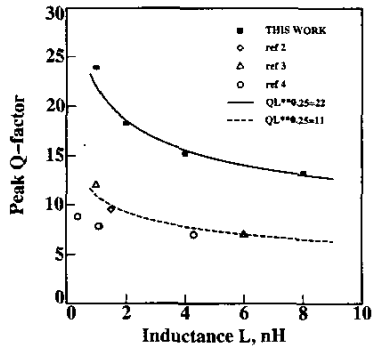

Figure 19: Reported Q-factor versus inductance for inductors realized in standard logic 90 nm node back-end processes. Trendlines reflect trade-offs.