

# Gate-Capacitance Extraction from RF C-V Measurements

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## Abstract:

In this work a full two-port analysis of an RF C-V measurement set-up is given. This two-port analysis gives insight on the limitations of the commonly used gate capacitance extraction, based on the  $Y_{11}$  parameter of the device. It will be shown that the parasitics of the device can disturb the extracted gate capacitance and a new extraction scheme, based on the Z-matrix, is introduced that eliminates the effect of these parasitics. Measurement results prove the validity of this new extraction scheme, under different conditions.

## 1. Introduction

With decreasing dimensions of CMOS devices, the reducing oxide thickness leads to an increase of the gate oxide tunnelling current [1-6]. This high leakage current causes problems in the characterization of the oxide capacitance, because the quality factor of the measured capacitor can become very low. The RF C-V method presented in [2] deals with this problem by measuring C-V curves at RF frequencies, thereby minimising the effect of the tunnelling current in comparison to the oxide capacitance. If the measurements are performed using a two-port network analyzer, a lot of useful information is available. In this paper for the first time full use will be made of this two-port data to extract the gate-capacitance in a more accurate way.

In the RF C-V method, the capacitance is extracted using the  $Y_{11}$  parameter. Besides the desired gate-capacitance this  $Y_{11}$  parameter also contains parasitics caused by the gate resistance, the well impedance, the drain/source series resistance and the junction capacitance between the channel region and drain/source region. Ideally, devices are designed in such a way that these parasitics can be neglected. This paper will show that with increasing measurement frequencies the junction capacitance can disturb the extracted C-V curve, using the extraction method of [2] or [3]. A more precise capacitance extraction procedure can relax the design and measurement guidelines earlier proposed in [4,5].

In figures 1 and 2 a MOS capacitor is illustrated and the connections are shown that are used for RF C-V measurements; the drain and source are connected to port 2 and the gate terminal is connected to port 1, the well contact is connected to the ground. In figure 1 an

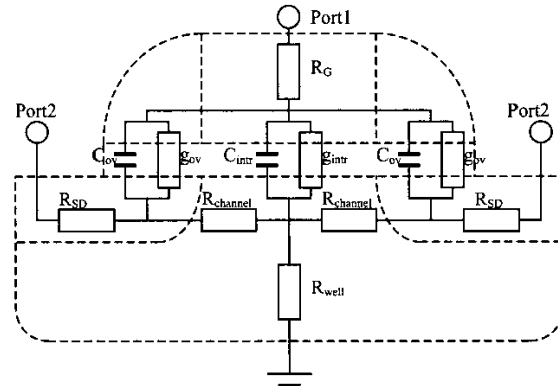


Figure 1. Schematically drawn cross section of a MOS capacitor used in S-parameter measurements with an equivalent circuit in inversion bias. Overlap regions are separated from the intrinsic oxide region. The channel region is modelled by a channel resistance.

equivalent circuit for the MOS capacitor is drawn when it is biased in inversion and in figure 2 the equivalent circuit in accumulation bias is shown. In these equivalent circuits the overlap regions between the gate and the drain and source terminals are separated from the intrinsic oxide region between the gate and the channel region. In figure 1 a channel resistance can be seen that exists between the channel region and the drain/source regions. In the accumulation circuit a junction capacitance is included between the channel and the drain/source regions.

From figure 1 and 2 the effect of the gate resistance  $R_G$ , the well resistance  $R_{well}$ , the drain/source series resistance  $R_{SD}$  and the channel impedance,  $Z_{ch}$ , on  $Y_{11}$  can clearly be seen. It is obvious that if these parasitics become too large, the extracted gate-capacitance using only  $Y_{11}$  can become erroneous.

## 2. MOS capacitor model

In order to analyse the limitations of the  $Y_{11}$  extraction method, the correctness of the commonly used three-element model of a leaky gate dielectric will be investigated. This model is shown in figure 3a). The tunnelling current is represented by  $g_{ox}$  and  $R_S$  models the behaviour of the gate, well and source/drain resistances. The model is based on a 1-port measurement set-up with the source and drain connected to ground while the effect of  $R_{channel}$  and  $C_j$  can be neglected. This

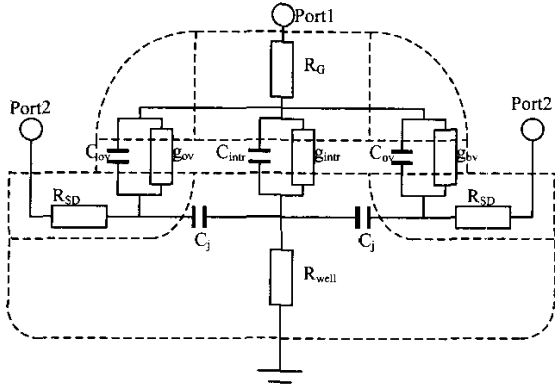


Figure 2. The same schematic MOS capacitor cross section as in figure 1, but now the equivalent circuit of the MOS capacitor biased in accumulation is given.

three-element model is a simplification of the two-port model shown in figure 3b). In this two-port model the intrinsic oxide region is separated from the overlap regions and the effect of the channel impedance is included. In accumulation the channel impedance  $Z_{ch}$  consists of the junction capacitance and in inversion this impedance models the channel resistance. Furthermore, the gate resistance, the well resistance and the drain/source series resistance are separately taken into account. The total gate capacitance that we are looking for is the intrinsic capacitance  $C_{intr}$  in parallel with the two overlap capacitances  $2 \cdot C_{ov}$ . In extractions based on the model of figure 3a) this capacitance is equal to  $C_{ox}$ . Both the RF C-V method in [2] and the two-frequency method of [3] use this three-element model. If  $R_S \ll 1/(j \cdot \omega \cdot C_{ox} + g_{ox})$  the capacitance can be extracted using: [2]

$$C_{ox} = \frac{C_{intr} \cdot 2 \cdot C_{ov}}{C_{intr} + 2 \cdot C_{ov}} = \frac{\text{Im}(Y_{11})}{\omega} \quad (1)$$

For the two-frequency method to be applicable only  $\text{Im}(R_S)$  must be negligible compared to  $\text{Im}(1/(j \cdot \omega \cdot C_{ox} + g_{ox}))$ . The two-port model shows that the actual series resistance consists of two parts: the series resistance that is seen by the signal flowing through the intrinsic oxide region and the series resistance of the signal that flows through the overlap regions. These series resistances can be derived from figure 3b) and two conditions can be set up that must hold if the capacitance can be correctly extracted using the two-frequency method in combination with the three-element model.

$$\text{Im}\left(\frac{R_{well} \cdot Z_{ch} + R_{well} \cdot R_{SD}}{R_{well} + Z_{ch} + R_{SD}} + R_G\right) \ll \text{Im}(Z_{intr}) \quad (2)$$

$$\text{Im}\left(\frac{R_{SD} \cdot Z_{ch} + R_{SD} \cdot R_{well}}{R_{well} + Z_{ch} + R_{SD}} + R_G\right) \ll \text{Im}(Z_{ov}) \quad (3)$$

Since the imaginary part of  $Z_{intr}$  and  $Z_{ov}$  can become very small at increasing frequencies (it has a  $1/\omega \cdot C$  dependence), it is not trivial to assume that the two conditions of (2) and (3) are met.

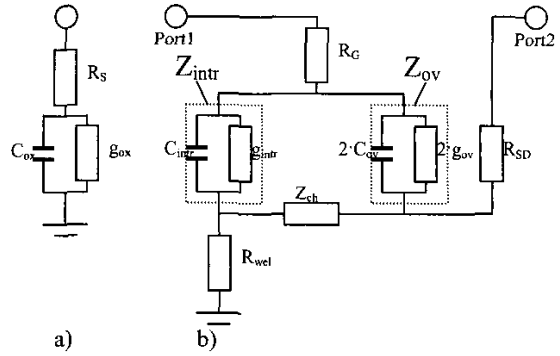


Figure 3. Circuit approximations of a leaky MOS transistor. a) three-element model, b) two-port model. The intrinsic oxide region is separated from the overlap region and the parasitics are separated as well. All impedances are bias dependent; in inversion  $Z_{ch}$  models the channel resistance and in accumulation it models the junction capacitance.

In order to use the extraction of (1) the conditions are even more stringent: The real part of the two series resistances must also be negligible compared to the real part of  $Z_{intr}$  and  $Z_{ov}$ .

### 3. Two-port Extraction method

If the two conditions in (2) and (3) are not met, it is not possible to extract the gate-capacitance using the three-element model of figure 3a). In this situation the two-port model of figure 3b) needs to be used. To simplify the analysis of this model it can be converted into the circuit shown in figure 4, making use of a  $\Pi$ -T transformation of the  $\Pi$  network consisting of  $Z_{intr}$ ,  $Z_{ov}$  and  $Z_{ch}$  in figure 3b). The transformed model shows three new impedances, named  $Z'_{ox}$ ,  $Z'_{ch\_intr}$  and  $Z'_{ch\_ov}$ .  $Z'_{ox}$  is the impedance that we are looking for, under the assumption that  $Z_{SD} \ll Z_{intr} + Z_{ov}$  it can be derived that

$$Z'_{ox} \approx \frac{Z_{intr} \cdot Z_{ov}}{Z_{intr} + Z_{ov}} = \frac{1}{j \cdot \omega \cdot (C_{intr} + 2 \cdot C_{ov}) + g_{intr} + 2 \cdot g_{ov}} \quad (4)$$

The assumption made is acceptable because typically  $C_j \gg C_{intr} \cdot C_{ov} / (C_{intr} + C_{ov})$  and the channel resistance is generally very small. Expression (4) shows that  $Z'_{ox}$  models the parallel impedance of the overlap and the intrinsic oxide region. The two other new impedances that can be seen in figure 4 are the channel impedances  $Z'_{ch\_intr}$  and  $Z'_{ch\_ov}$ . They can be derived to be:

$$Z'_{ch\_intr} = \frac{Z_{ov} \cdot Z_{ch}}{Z_{intr} + Z_{ov} + Z_{ch}} \quad (5)$$

$$Z'_{ch\_ov} = \frac{Z_{intr} \cdot Z_{ch}}{Z_{intr} + Z_{ov} + Z_{ch}} \quad (6)$$

If we look at the  $Y_{11}$  parameter derived from figure 4 we get:

$$\frac{1}{Y_{11}} = R_G + Z'_{ox} + \frac{(Z'_{ch\_intr} + R_{SD}) \cdot (Z'_{ch\_ov} + R_{well})}{Z'_{ch\_intr} + Z'_{ch\_ov} + R_{well} + R_{SD}} \quad (7)$$

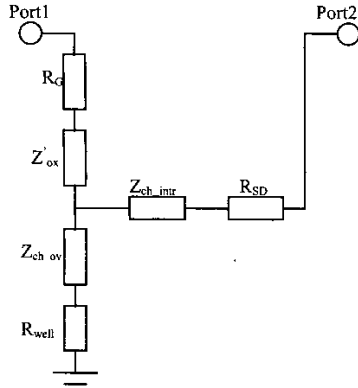


Figure 4. Equivalent circuit of the two-port model from figure 3b after a  $\Pi$ -T transformation.

In this expression we recognise  $R_G$ ,  $Z'_{ox}$  and the series impedance originating from  $R_{well}$ ,  $R_{SD}$ ,  $Z_{ch\_intr}$  and  $Z_{ch\_ov}$ . If  $R_{SD}$  and  $R_{well}$  are not negligible and the transistor is biased in accumulation (a junction capacitance exists) it can be seen that this  $Y_{11}$  parameter cannot be used to extract the gate capacitance. If we look at the  $Z$ -matrix however, we get:

$$Z = \begin{bmatrix} R_G + Z'_{ox} + Z_{ch\_ov} + R_{well} & Z_{ch\_ov} + R_{well} \\ Z_{ch\_ov} + R_{well} & R_{SD} + Z_{ch\_intr} + Z_{ch\_ov} + R_{well} \end{bmatrix} \quad (8)$$

Based on this  $Z$ -matrix we can derive the following expression:

$$R_G + Z'_{ox} = Z_{11} - Z_{12} \quad (9)$$

Now the gate capacitance can be extracted using the two-frequency method or, if  $R_G \ll Z'_{ox}$  the following expression, similar to (1) can be used

$$C = \text{Im} \left( \frac{1}{Z_{11} - Z_{12}} \right) \cdot \frac{1}{\omega} \quad (10)$$

From this two-port analysis it can be concluded that the gate capacitance can be extracted in a more accurate way if it is done using  $Z_{11}$ - $Z_{12}$  extraction instead of  $Y_{11}$  extraction. It should be noted that although the two-port model is based on a configuration with the source and drain connected together, it is easy to see that this method also holds for devices with a common source structure.

#### 4. Measurement Results

To compare the conventional  $Y_{11}$  and the new two-port method, measurements taken on two types of devices were analysed: devices that are optimised for RF C-V measurements (source connected to drain, type A) and devices with a common source structure (type B). The two devices were processed in two different research process flows, based on 0.18  $\mu\text{m}$  CMOS for the type A devices and on 100-nm CMOS for the type B devices. The type A device is a p-channel device with a relatively high well resistance (400  $\Omega$ ). It has a channel length of 0.15  $\mu\text{m}$  and width of 9360  $\mu\text{m}$ . The type B devices are n-channel devices with a low well resistance. The devices have a channel length of 0.11  $\mu\text{m}$  and a width of

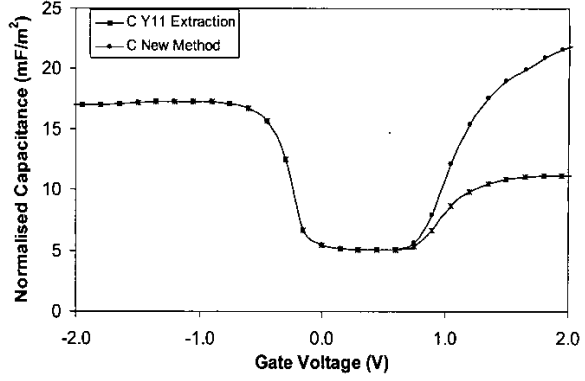


Figure 5. Capacitance extracted for type A devices, extracted at 810 MHz.  $Y_{11}$  extraction is compared to the new two-port extraction scheme.

40  $\mu\text{m}$ . Measurements were done using a HP 8510C network analyzer. The capacitance was extracted using (10). Figure 5 shows the normalised extracted capacitance of the type A devices with the two-port extraction method compared to the  $Y_{11}$  extraction. The new two-port extraction scheme was only used in accumulation bias. In the inversion regime the well impedance of this device becomes too large compared to  $Z'_{ox}$ , so that a proper extraction of  $Z'_{ox}$  is not possible. The limitations given in section 2 for the  $Y_{11}$  extraction show that this method can still be used when both the channel impedance and the drain/source series resistance are small. In inversion bias this is the case and therefore in this situation the most accurate C-V curve can be obtained using a combination of the  $Y_{11}$  extraction and  $Z_{11}$ - $Z_{12}$  extraction. This is typical for devices that have such a very high well resistance; if the well resistance is moderately high  $Z_{11}$ - $Z_{12}$  extraction can be used under all biasing conditions.

In Figure 6 the normalised C-V curves of the type B devices are shown. From figure 5 and 6 it can be seen that the newly extracted capacitances have the typical shape of the accumulation behaviour of ultra-thin dielectrics and inversion capacitance decreasing due to gate depletion. The curves in figure 6 have the same shape for both extraction methods: this is because for the type devices B all conditions for the extraction of (1) to hold are met. The type A devices suffer from a high well resistance and it can be seen that in accumulation the C-V curves of the two different methods differ greatly. By looking at figure 3b) this difference can easily be explained: the signal that flows through  $Z_{intr}$  does not flow through  $R_{well}$ , but through  $Z_{SD}$ . This means that in accumulation the junction capacitance lies in series with the intrinsic oxide capacitance if  $Y_{11}$  is measured. This effect is made clear in figure 7. The inverse of the capacitances gained from the two methods is plotted and also  $C_{j\_intr}$  is plotted. This capacitance is defined as:

$$C_{j\_intr} = C_j \frac{Z_{intr} + Z_{ov}}{Z_{ov}} \quad (11)$$

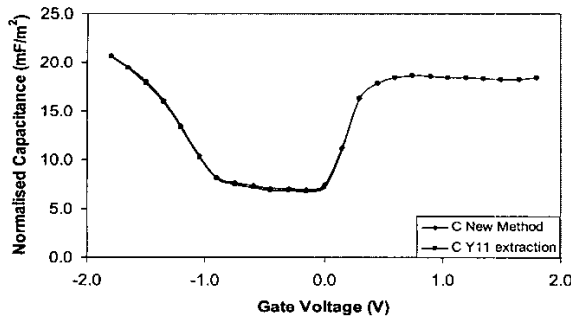


Figure 6. Capacitance extracted for type B devices, the capacitance is extracted at 1 GHz.  $Y_{11}$  extraction is compared to the new two-port extraction scheme.

In words  $C_{j\_intr}$  models the effect the junction capacitance has on only the signal flowing through  $Z_{intr}$ . This capacitance can be derived using the Z-matrix and under the assumption that  $Z_{SD} \ll Z_{intr} + Z_{ov}$ :

$$C_{j\_intr} = \text{Im} \left( \frac{1}{Z_{22} - Z_{21}} \right) \cdot \frac{1}{\omega} \quad (12)$$

Figure 7 clearly shows that the difference between the  $Z_{11}$ - $Z_{12}$  extraction method and the  $Y_{11}$  extraction method can be completely explained by the effect of the junction capacitance on the signal flowing through  $Z_{intr}$ . In the new two-port approach this effect is eliminated.

## 5. Discussion

The plots in figure 5 and figure 7 show that the extraction scheme described in this paper eliminates the junction capacitance from RF C-V measurements. The plot of figure 6 shows that the two-port approach can also be used for devices having a common source configuration. Although usually RF C-V measurements are performed on devices with a lower well impedance than the type A devices used in this paper, the new method is also useful on devices having a moderate well impedance. Having a low well impedance, the extracted C-V curves may coincide better with each other; the well impedance is however never infinitely small; therefore a small error on the extracted capacitance using  $Y_{11}$  extraction is always present.

Since this new extraction scheme is based on making full use of two-port data, this method is in the first place intended to use in combination with a two-port network analyzer. In the event that only one-port data is available, it can be shown that a similar method can be derived, based on the  $Z_{11}$ ,  $Z_{22}$  and the  $Y_{11}$  parameter (obtained with two measurements with the output open and one with a short circuited output). This will not be further discussed in this paper, but this allows to use an LCR meter in combination with the new two-port extraction scheme.

The only limitation necessary for the new approach to hold is that  $Z_{ch} \ll Z_{intr} + Z_{ov}$ . This condition is easily met. A situation in which the new approach cannot be used is when the channel length of the devices becomes so large that non-quasistatic effects start to play a role. In this case a distributed model of the gate leakage current and the well impedance should be used [6]. The two-port model of figure 3b) will no longer hold and the

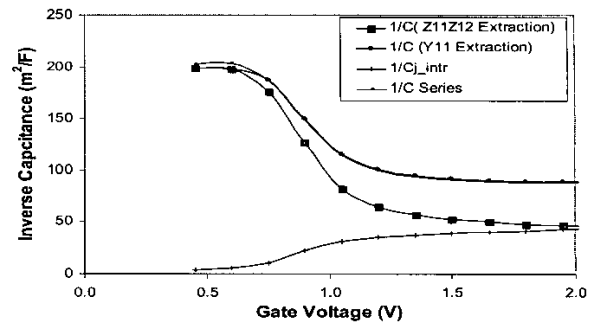


Figure 7. The inverse of the extracted capacitances compared to the junction capacitance, extracted at 810 MHz. The series capacitance of the junction capacitance and the extracted capacitance using the new method is also included.

gate-capacitance derived using the new two-port extraction will no longer be accurate.

## 6. Conclusions

A new capacitance extraction scheme has been developed for measuring the capacitance of leaky gate dielectrics. The new method makes use of a two-port model of a MOS capacitance and thereby eliminates the effect of the junction capacitance between the channel and the drain/source region if the transistor is biased in accumulation. Measurement results have shown that the effect of the junction capacitance can be quite large if the well impedance of the device is not negligible. The new method can completely eliminate this junction capacitance. The new method holds if the channel length is sufficiently small so that it does not suffer from NQS effects.

## 7. Acknowledgement

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## 8. References

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