BiCMOS Technology Improvements for Microwave Application

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Abstract—**. The third generation of NXP 0.25 µm SiGe BiCMOS technology (QUBiC4Xi) is presented. The NPN has f_T /f_{max} of 216/177 GHz and BV_{cb0} of 5.2 V. The high-voltage NPN has 12 V BV_{cb0}, and f_T /f_{max} of 80/162 GHz. This is complemented with an improved MIM capacitor with 1THz cutoff frequency and new on-chip isolation structures that demonstrate a record |S12| of -60 dB at 10 GHz.**

Index Terms—**HBT, heterojunction bipolar transistor, substrate isolation, MIM capacitor, BiCMOS, bipolar, Si, SiGe, SiGe:C, TaO_5.**

I. Introduction

SiGe HBT technology and performance has been improved tremendously in the last decade. This has opened up new opportunities for silicon-based technology in the area of microwave and millimeter wave applications. However, these markets are not mature enough to support high wafer volumes and highly integrated solutions that are required for cost-effective manufacturing. Therefore, NXP has developed various SiGe process variants that are derived from the highly successful QUBiC4 0.25µm BiCMOS technology family [1, 2]. A high degree of commonality with the parent technology that is running in high volume is maintained in all cases. This ensures low cost of wafers and development, high manufacturability and control, and high quality that is proven in high volume.

Here an improved version of QUBiC4X is presented: (QUBiC4Xi) [2]. The technology comes with all the advanced passives of the parent technology and maintains full compatibility to the 0.25µm CMOS node [1, 3]. Here we introduce a faster NPN heterojunction bipolar (HBT) that is discussed in Section II. A modified (single mask adder) 5fF/µm^2 TaO_5 MIM capacitor with improved scalability and reduced top-plate resistance is presented in Section III. Section IV highlights the outstanding substrate isolation that can be achieved with the high-resistivity substrate (200 Ωcm, CZ) and optimized layout techniques. We will finalize with some conclusions in the last section.

II. The NPN

The bipolar device lies at the heart of the technology. The SiGe module has been implemented in such a way that most integration steps and mask levels can be shared with the (full-silicon) parent technology. The basic architecture is similar to the original concept [4]. Key aspects are the double poly architecture that ensures an excellent base link and a non-self aligned approach that maintains process simplicity; it adds a mask but avoids a lot of critical process steps (*e.g.* selective epitaxy or critical CMP steps).

For this generation emphasis was placed on the base link region, the emitter-base spacer in particular and the SiGe:C layer stack.

The emitter-base region is shown schematically in Figure 1. The base link is determined by two factors: the emitter-base spacer and a patterned etch-stop layer to facilitate robust emitter-window patterning.

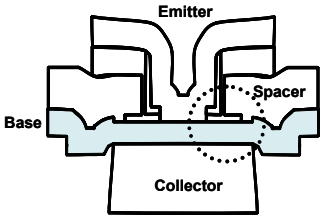

Figure 1 Schematic cross-section of the NPN device with the base-link area highlighted.

The spacer is most critical because it also determines the scalability of the emitter width. Figure 2 shows two TEM images that compare the new spacer module that was introduced to the original spacer.

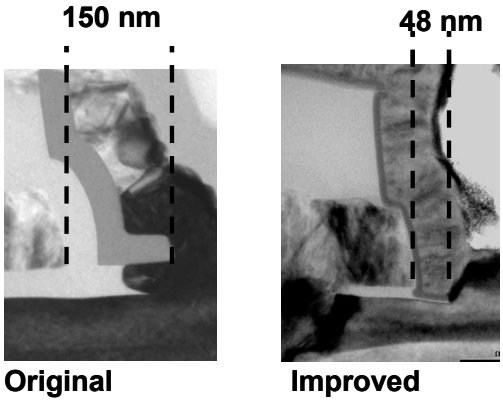

Figure 2 TEM image of original and improved emitter-base spacer.

The spacer width has been considerably reduced from 150 to 48 nm. It is composed of a much thinner oxide nitride stack that is easier to integrate than the thicker layers.

The very thin layers form a nitride "blanket" that effectively seals off all the oxide layers. Wet etching solution cannot penetrate the tiny exposed oxide areas. This eliminates any undercut and allows for very aggressive pre-cleaning prior to deposition of the epitaxial mono emitter. This leads to a high quality interface, very reproducible spacer dimensions and (effective) emitter width.

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The shorter distance under the spacer also leads to 50% reduction in base-link resistance as is shown in Figure 3. The improved scalability facilitates downscaling of the emitter width from 0.4 µm to beyond 0.25 µm.

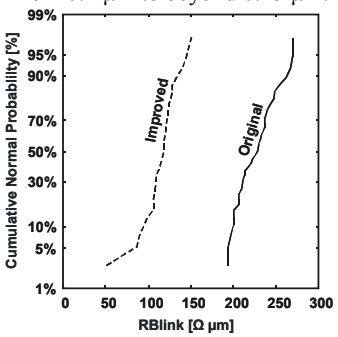

Figure 3 Cumulative probability of the base link resistance.

The SiGe base layer was also improved, a 30% reduction in base width and increased Ge content gives substantially higher current drive.

Table 1 shows parameters for a selection of scaled-down devices with the improved spacer module and the new SiGe stack. A "Fast" SiGe stack is also included in the first column. We consider the "slightly slower" stack to be a better tradeoff between base resistance and high-voltage/low voltage combination of devices.

		NPN				
		high freq			high V	Comment
Area	µm²	10x0.25x1.0*	10x0.25x1.0	0.3x20.7	10x0.4x1.0	
Annotation		A1	B1	B2	C1	see figures
f_T	GHz	216	176	163	80	V_{cb}=1V
f_{max}	GHz	177	172	129	162	V_{cb}=1V, unilateral gain
slope	dB/dec	-19.7	-19.3	-19.9	-20.7	V_{cb}=1V, unilateral gain
C_{be}	fF	45	37	66	47	off state, 1GHz
C_{cb}	fF	31	35	50	15	off state, 1GHz
C_{cs}	fF	8	8	6.25	12	off state, 10GHz
τ_N	ps	0.61	0.78	0.8	1.56	on state, 13 GHz
$(C_{be}+C_{cb})$	fF	105	95	224	76	on state, 13 GHz
BV_{ce0}	V	1.44	1.44	1.44	2.5	
BV_{cb0}	V	5.2	5.2	5.2	12	
Hfe	-	2700	2700	2100	1700	at 0.7 V Vbe
re	Ω	3.4	14	2.9	<1	
I_{e0}	fA	0.94	0.55	2	3.7	
Rpinch	kΩ sq	4.8	3.25	3.25	3.25	

* Alternative SiGe base layer

Table 1 A selection of devices with some basic parameters. The first column is an alternative base layer with a different rb/f_T tradeoff.

The emitter has been divided into smaller islands to optimize the base resistance and to keep the power density (with regards to self-heating) in check. The total device size is large enough to allow for accurate RF characterization and deembedding.

All RF data presented was obtained from on-wafer measurements with an 8510 Agilent network analyzer (NWA) that is hooked up to a Cascade 12k semiautomatic probestation with Cascade 125 µm pitch GSG Infinity probes. The system was calibrated with the customary SOLT procedure. The measurement was subsequently deembedded with on-wafer "OPEN" and "SHORT" dummy structures.

Figure 4 shows the actual RF characteristics of the devices listed in Table 1. the highest f_T (216 GHz) is obtained with the "fast" 4.8 kΩ/sq. stack. Nevertheless, the slower stack has identical f_{max} and a superior high-voltage device. This device is fabricated on the same wafer as the 176 GHz f_T device. It has a remarkable combination of 12 V breakdown (BV_{cb0}) with an f_T/f_{max} of 80/162 GHz.

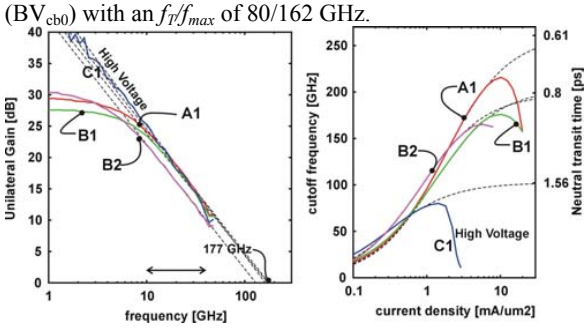

Figure 4 RF characteristics: unilateral gain vs frequency biased at maximum f_T (left) and f_T (|H21|*f@13 GHz) vs. Ic. All measurements were performed with 1 V Vcb. The annotation is relates to the detailed information in Table 1.

III. METAL3 MIM CAPACITOR

The 5 fF/µm² MIM capacitor in the parent technology is fabricated between metal 4 and metal 5 with a stack of TiN, TaO_5 capped with another layer of TiN. It is implemented as a single-mask adder by virtue of optimized dry etching and cleaning procedures [5]. It is used extensively as an RF component and for decoupling.

High frequencies require much smaller capacitors, but the capacitance density must remain fixed as there will be a need for large decoupling capacitors regardless of the application frequency.

A smaller minimum geometry is the only solution. This can only be achieved in a lower metal level because the designrules for the very thick metal 4 and 5 and via 4 are very crude (i.e. Via4 size is 1x1 µm, Metal 6 lines/spaces: 6/3 µm). Via 3 is more than 4 times smaller (in area), with a 3 times smaller pitch. A 4x smaller minimum size (that fits two vias) is achieved by moving the MIM layer from metal 4 to metal 3, reducing the minimum capacitance to 10 fF. A comparison of MIM position between parent technology and QUBiC4Xi is shown schematically in Figure 5.

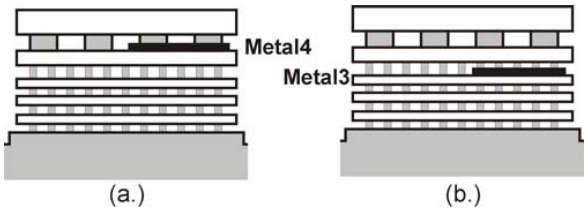

Figure 5 Schematic figure showing MIM position in parent technology (a.) and QUBiC4Xi (b.).

The RF quality factor (Im(Y12)/Re(Y12) with C between port 1 and 2) is dominated by the series resistance imposed by limited conductivity of the TiN top plate. This was originally compensated with a thick TiN layer and a large number of vias connecting the top plate to the highly conductive metal 5. Here we have added a layer of AlCu to the top plate and reduced the TiN thickness. The overall stack is: metal 3, TiN, TaO_5, TiN, capped by AlCu. The higher conductivity of AlCu vs. TiN allows for a thinner overall stack with a 10x reduction in top-plate sheet resistance.

The RF performance up to 50 GHz of various geometries is shown in Figure 6.

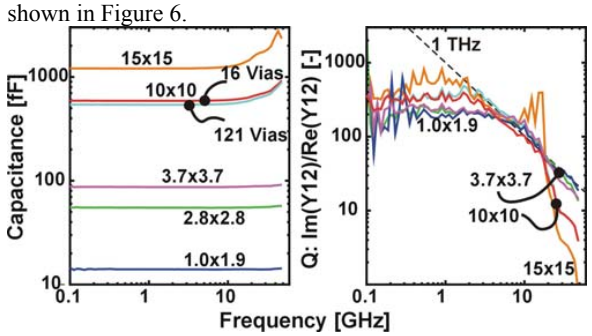

Figure 6 Measured RF performance of 6 MIM designs. Capacitance (left plot) is Im(-*Y*12)/2πf, Q factor (right) the ratio between imaginary and real part of *Y*12.

All capacitors have an excellent bandwidth, over a large range of capacitance values. The larger values are impacted above 10GHz or so by miniscule parasitic inductance (~5 pH).

The quality factor (as defined for a capacitor) follows a limit corresponding to a 1THz cutoff. The large capacitors are in close proximity to self resonance at high frequency. This increases the real part of Y12 that is unrelated to RF losses (resistance) and thus defeats the Q definition that assumes pure capacitive behavior.

The parasitic capacitance to the substrate is obviously increased (from 5.55 to 7.77 aF/µm^2) by moving down one level. Nevertheless, it is still ~3 orders of magnitude smaller than the capacitance itself (5 fF/µm^2); negligible in both cases.

IV. Substrate Isolation

Isolation is a major challenge in electronic circuits and becomes especially challenging in analog/RF IC design due to close proximities, high dynamic range, high frequency and a shared silicon substrate.

There are various design aspects that play a crucial role in achieving high isolation. Three concepts discussed here are illustrated in Figure 7.

The signal pads are connected to the underlying P-Well with Buried P or N-Well with Buried N (as shown in the cross section). The substrate is a (200 mm) 200 Ωcm P-type CZ wafer; standard material for QUBiC4+ and all SiGe derivatives [1, 2].

In the first structure, isolation is provided by several rings of deep-trench isolation (DTI) around the well (a. in the figure). The second structure is similar but has an additional conductive, grounded guard ring around each pad (b. in the figure). The third variant is similar to the second, but now the ground domains between the two ports have been disconnected (c. in the picture).

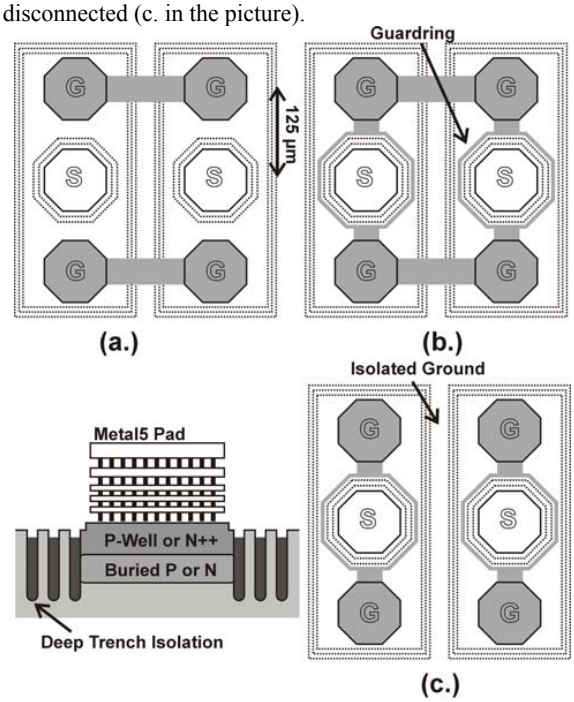

Figure 7 Schematic drawing of the layout of isolation GSG test structures. The signal pad is connected to a P-type or N-type area (lower left crossection). Three concepts: DTI isolation (a.), DTI isolation with a grounded guardring (b.), DTI isolation with a grounded gurdring with isolated ground domains.

The layouts are designed in such a way that they fit directly to on-wafer (125 µm pitch) GSG probes. This way open/short deembedding is avoided, which would be problematic with very poor isolation of "OPEN", and sometimes, "SHORT" dummy. Consequently, results shown in this section are non-deembedded values taken straight from the (calibrated) NWA.

Structure	Type	Diameter	# DTI rings	Guardring	shared Ground	Figure
		µm				
I	P	80	5	No	-	a.
II	P	80	5	Yes	No	c.
III	P	50	5	Yes	No	c.
IV	N	80	1	Yes	Yes	b.
V	N	80	5	Yes	No	c.
VI	N	50	5	Yes	No	c.

Table 2 A selection of isolation structures with reference to Figure 7.

RF measurements of the selection of structures presented in Table 2 are shown in Figure 8 and Figure 9.

The high degree of isolation that can be achieved with properly designed guardrings in separate ground domains is

remarkable. To our knowledge these values exceed anything previously reported [6, 7]. Furthermore, it is surprising, counterintuitive, to see equivalent isolation between P-type and N-type connections above 1 GHz or so. This is clearly the high substrate resistivity at work.

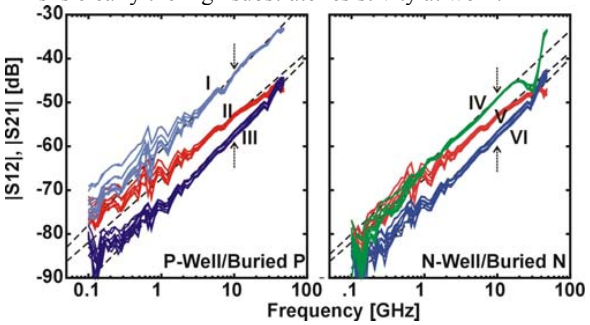

Figure 8 Isolation for structures in Table 2 in terms of |S12|, |S21| with 50 Ω system impedance. Left plot: P-type, right plot: N-type.

The behavior is predominantly capacitive with a slope slightly deviating from 20dB/dec, which can be explained by distributed RC effects. It is somewhat arbitrary to present the results in terms of S parameter magnitude. The isolation between actual circuit nodes will depend on their impedance level, which is likely to be different from the 50Ω system impedance.

To complement the picture, the input impedance of the isolated pads also needs to be considered. Note that in the particular case of isolation the transfer coefficients are much smaller than the reflection coefficients thus resulting in Y11≈1/Z11 and Y22≈1/Z22 (with Y and Z following the usual two-port definitions). Hence the apparent arbitrary choice of inverse input/output impedance in Figure 9 reflects the general case very well.

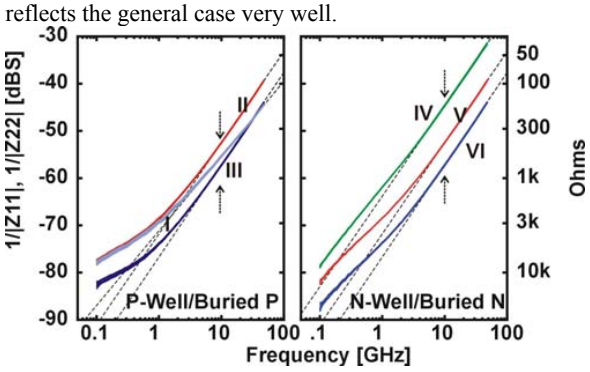

Figure 9 Inverse input impedance of structures in Table 2 in dB(Siemens). Left plot: P-type, right plot: N-type.

The impedance exhibits capacitive behavior at high frequencies. Below 1 GHz the direct DC connection (~ 30 kΩ resistance) between the P-type pads becomes noticeable.

The pads without guardring (I), despite poor isolation, have a very decent input impedance al the way up to 50 GHz. The guardring with a single DTI ring (IV) reaches unacceptable low impedance already at 10 GHz. The structures with 5 DTI rings and a guard ring (II, III, V, VI) have a considerably higher input impedance combined with high isolation.

The pad diameter also plays an important role, the smaller pads (50 µm diameter) have superior isolation that scales roughly with the perimeter at high frequency (20·log(80/50)~ 4dB).

V. Conclusions

A highly versatile and low-cost 0.25 µm SiGe:C microwave technology is presented. It features a scaled NPN with cutoff frequency of 216 GHz and 177 GHz f_{max}. A high-voltage device with 12 V BV_{cb0}, 80 Ghz f_T and 162 GHz f_{max} is also supported. The 5 fF/µm^2 MIM capacitor is very similar to that of the parent technology but with improved scalability and versatility by introducing smaller designrules and higher top-plate conductivity. It has ample RF performance with a cutoff frequency (frequency where Q reaches 1) of ~ 1 THz and a bandwidth in excess of 10 GHz for a 1 pF capacitor.

On-chip isolation of -60dB (S12 magnitude) of a 50µm diameter N-Well or P-Well island is demonstrated, this is among the highest values reported. The highest isolation is achieved with a combination of deep trench isolation and guardrings with isolated ground domains.

Acknowledgements

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