

Design of a Highly Dependable Beamforming Chip

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Abstract—As CMOS process technology advances towards 32nm, SoC complexity continuously grows but its dependability significantly decreases. In this paper, a beamforming chip¹ is designed using 64 reconfigurable Xentium tile processors. A functional dependability analysis for this application was carried out following the IEC standard 62347. To meet the dependability requirements, a dedicated infrastructural IP (IIP) and supporting software and hardware have been designed and included as part of the dependability infrastructure of the chip. This IIP can periodically verify the correctness of the tile processors and coordinate the run-time mapping reconfiguration software to isolate the faulty tiles at run time and assign spare processors for the open DSP tasks. Dependability graphs show a significant improvement of the application chip incorporating the design-for-dependability hardware and software.

Keywords—dependability; beamforming; SoC; design-for-dependability; reconfigurable tile processor

I. INTRODUCTION

Nowadays, the CMOS process technology has advanced to 45 nm and the industry has indicated that the 32 nm process will become available for mass production in 2010 [1]. The technology progress provides the possibility to include many arithmetic processing units in one System-on-Chip (SoC) to perform sophisticated digital signal processing (DSP) tasks such as the beamforming in a phased array radar.

With the size of the transistors shrinking, the complexity of SoC is steadily increasing, which results in ICs containing several hundred million transistors. A direct consequence of the IC complexity increase is that the dependability of these ICs drops significantly. Fig. 1 shows the calculated reliability [2] of a 10-million gates LSI goes down to about one third of that of a 1-million gates LSI over a 10 years period.

Today, multi-core processor ensures a continuous growth of system computing capability even when the clock frequency of a single core has reached its power limitation [3]. In addition to the boost of processing power, this multi-core architecture can also be used to improve the

dependability of complex ICs. A word-level reconfigurable domain-specific core, the Montium [4] of Recore Systems [5], is a suitable building block for a multi-core processing unit with ultra-low energy consumption. Recently, research has been carried out on the reconfigurable Montium tile processors and how to use its unique reconfiguration function to improve the dependability of a complex SoC [6], [7].

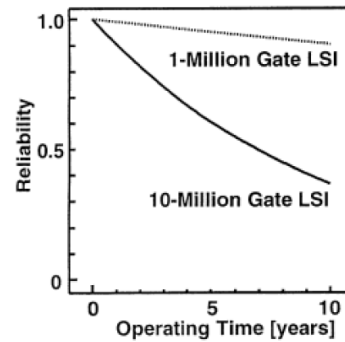


Figure 1. Reliability degradation over time: 10 million and 1 million gates LSI comparison [2].

In this paper, a heavy DSP capability reliant application, being the beamforming system of a phased array radar, is designed using the Xentium processing tiles. The Xentium is a programmable digital signal processing tile designed for high-performance computing from Recore Systems. Considering the dependability requirements for a beamformer application, the design evolves from a printing circuit boards (PCB) based solution to a single chip solution. To enhance the system dependability, an infrastructural IP (IIP) and supporting software have been designed and added in the SoC; calculations will show that a significant dependability improvement is achieved.

In section II, we analyze the dependability specifications of the beamforming system and show the dependability requirements from the end user point of view. A structural SoC-based design of the beamforming system is demonstrated in section III and the need for dependability improvement is explained. Then in section IV, the infrastructural IP and its operational capability are given in detail and the subsequent dependability improvement is indicated. Conclusions are provided in section V.

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II. FUNCTIONAL DEPENDABILITY SPECIFICATIONS OF THE BEAMFORMING SYSTEM

In this section, we will follow the IEC standard 62347 [8] to identify the beamforming system, describe its objective, operating profile and key functions. The dependability requirements for the implementation will also use IEC standard 60300-3-4 [9] as guidance.

A. Beamforming system introduction

Beamforming is a technique which combines signals received from multiple antennas. It requires a massive amount of digital signal processing and can be applied in e.g. phased array radars.

The objective of a beamforming system is to calculate the key parameters of objects in a three-dimensional space. It can increase the sensitivity of wanted signals and decrease that of unwanted signals. The application area emphasizes specifically on low ownership costs and a long life time.

B. Operating profile and key functions

To meet the system objective, a set of tasks have to be carried out in a given sequence (i.e. the operating profile [8]). In this paper, we only consider the operating profile of the normal operating scenario.

The complete beamforming system acquires the receiving signal from each antenna element and subsequently converts the analogue signal into a digital word ("ADC" block in Fig. 2). There can be a number of channels performing this task for a specific system. We will refer to this set of functions as the *pre-processing* task.

A typical function after the beamforming system is the Doppler filtering (DPL) as can be seen in Fig. 2. The pre-processing and Doppler filtering tasks are out of our current dependability research scope. Hence when it comes to the determination of system dependability requirements, infinite dependability will be assumed for them in this paper.

The central tasks (Fig. 2) which are the focus of this paper are:

- Channel filtering
- Beamforming (BF)
- Control

Functions within the channel filtering *task* are Hilbert filtering and Band-Pass filtering. FFT is the abbreviation for Fast Fourier Transform (see Fig. 2). Functions within the beamforming (BF) block are channel matrix multiplication and scalar multiplication of beam coefficients.

All the tasks are shown in detail in Fig. 2. The dashed boxes show part of the pre-processing (right) and part after the beamforming (left) and they will not be considered in the dependability calculations in this paper.

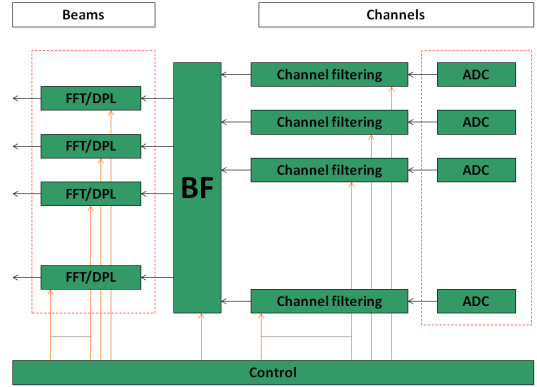


Figure 2. Operating profile details of the beamforming application.

C. Dependability requirements

IEC standards 62347 and 60300-3-4 have been used as references for the dependability requirements calculation. Some general remarks on the dependability attributes of the target beamforming system are explained:

Reliability. Reliability is, by definition, the ability of a system to correctly perform required functions under given conditions for a specific period of time [9]. It can be described by a probability that the system can successfully complete its function without failures.

In industry, the mean time between failures (MTBF) data (in hours) is also used to describe system reliability. The MTBF requirements (in hours) for the system functions mentioned in section II are representative for a typical industrial application (the specific MTBF values of the functions are not disclosed in this paper).

A commercial dependability evaluation software tool like BlockSim 7 [10] can be used to plot the system reliability over time based on the MTBF information of the basic functions/blocks of the system. We currently assume a constant failure rate and hence an exponential failure distribution will be used for reliability calculation.

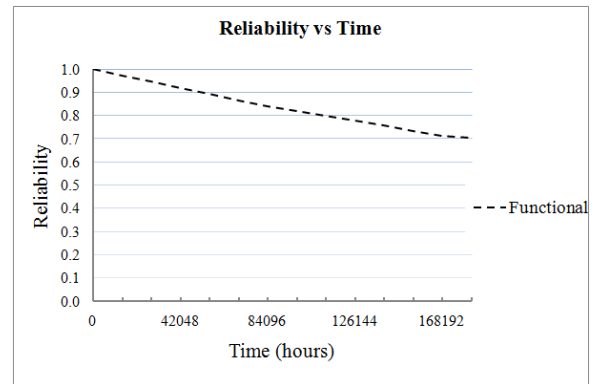


Figure 3. System reliability requirements from a functional perspective.

Fig. 3 shows the system reliability curve in 20 years calculated by BlockSim based on the MTBF values of basic

system functions. This data will be considered as the minimum reliability requirement for the system.

Maintainability. Maintainability and availability both involve repair options. The repair of the system will only take place after fault detection and hence corrective maintenance is performed.

After a fault (restrictions are provided in section II, D) is detected, the related Mean Time To Repair (MTTR) is required to be within 1 ms. This requirement is derived from system operation considerations at a higher level.

From a conventional electronic point of view, an IC will usually be discarded if an internal defect has been detected, which means effectively no maintainability work can be done at the chip level. However, our suggested approach features *chip-level maintenance* possibilities. This is achieved by having redundant processing tiles as spare on the chip and replacing the faulty tiles with good ones once faults are detected. More details will be introduced in the following sections.

Availability. The requirement for the availability of a state of the art system is at least 99 % for conventional cases. As the beamforming system can be used for mission critical operations, a mean down time (MDT) is optionally specified for some core functions. For example, a preferred MDT for the beamforming function is 50 ms. That means after a fault takes place, the mean time it takes to both detect the fault and correct the fault is 50 ms.

The overall system dependability is summarized as following:

- Reliability: 0.98 (1 year), 0.70 (20 years) as shown in Fig. 3.
- Life time: 20 years.
- Availability: 99.0 %, best case mean down time 50ms.
- Maintainability: limited best case repair time 1 ms, worst case 2160 s (0.6 hr for manual PCB replacement).

D. Dependability boundary conditions

Scope of research. The beamforming system consists of many elements. In the scope of this paper, we confine our research only to the hardware elements; software dependability and human interactions issues will not be considered.

Moreover, among all possible hardware faults, only permanent stuck-at faults in the SoC will be tackled in this paper. We explicitly target at the permanent manufacturing defects that may occur after production and the defects which may occur due to transistor and interconnect degradation [11].

Environmental factors. In the existing products, propriety boards are used in a conditioned environment. But nowadays an increasing amount of commercial off-the-shelf (COTS) components are being adopted and assembled on the PCBs. Since these COTS components often operate under normal consumer electronics conditions (temperature,

humidity, pressure and shock, etc.) a sheltered environment is offered to them during operation. Hence, the anticipated environmental condition of the beamforming system is specified as a *sheltered* environment, which is the same as a normal consumer electronics environment.

III. STRUCTURAL IMPLEMENTATION OF THE BEAMFORMING SYSTEM

System dependability is determined early in the design phase and is also influenced by the chosen implementation method. In this section, we explain two implementation methods for the beamforming system and compare the resulting system dependability with the user requirements.

A. How to meet the system dependability requirements

After the dependability specifications of the beamforming system have been fixed from a functional behavior perspective (*functional dependability*), the system is designed and implemented at the structural level and the resulting dependability of the system (*structural dependability*) will be evaluated by gathering the dependability data of each building block to see whether the functional dependability requirements have been met. If not, then the block limiting the dependability has to be improved. If the dependability data of that block have been fixed (normal situation for COTS), fault-tolerant techniques can still be used (spare blocks) to obtain a desired system structural dependability.

The reliability data of the basic building blocks are currently provided in the form of MTBF by our SoC implementation partner. This data can be used in our commercial dependability evaluation tool and the overall system reliability over time and other parameters can be calculated.

B. Important building blocks and system function mapping

The key functions of the beamforming system are mapped to hardware blocks in the design phase. Most DSP functions (such as Finite Impulse Response and Fast Fourier Transform) are processed by an array of Xentium tile processors working in parallel. The less computation intensive functions and control are handled by a general purpose processor (GPP) which could be an “Arm 9” [12] or an equivalent embedded processor.

The target beamforming system is specified being capable of processing many channels at the same time (quality of service specification). The system function mapping to hardware blocks were accordingly made:

The *channel filtering* task (including Hilbert filtering and band-pass filtering) for 16 channels is carried out by the 32-bit Xentium tile processors using 36 individual tiles.

The *beamforming* function is also mapped to the tile processors. The same number of beams will be formed as

the filtered channels. 18 tile processors are required to process the required beamforming function of 16 beams.

The *control* task will be carried out by the GPP. One GPP is sufficiently capable to handle this function. The run-time mapping software which takes care of the reconfiguration of the Xentium tile processors is also executed on the GPP.

In conclusion, 54 tile processors and 1 Arm 9 equivalent GPP is used to fulfill the beamforming task.

C. Dependability evaluation of a PCB based implementation

Considering the available technology on market, the system was first prototyped using UMC 90 nm technology from a cost-economic perspective. The general purpose processor was implemented in a general purpose device (GPD) and an array of 9 Xentium tile processors were implemented in a reconfigurable fabric device (RFD). In total, the system would require six RFDs and one GPD and they were interconnected on a PCB to form the central part of a beamforming system.

The dependability data of the PCB and GPP were provided by our implementation partner according to their experiences with previous similar products. The reliability of the PCB is 300,000 hours in terms of MTBF. The GPD and RFD are processed in the same technology hence same reliability has been assumed for them. A MTBF of 3,000,000 hours will be used for both ICs for system reliability calculations. Replacement of both ICs is possible as plug-in sockets are used in the PCB. In case of failure, a MTTR of 30 minutes can be achieved by experienced technicians.

The major functional blocks of the system, e.g. PCB, GPD and RFD are connected in serial in BlockSim. By assigning the provided reliability data, the reliability of the overall system implemented on a PCB can be calculated as shown in Fig. 4. It is clear that the reliability of the PCB based system is much lower than the reliability requirements specified in the functional dependability calculation part. The low MTBF of the PCB is the key reason why the system reliability is low.

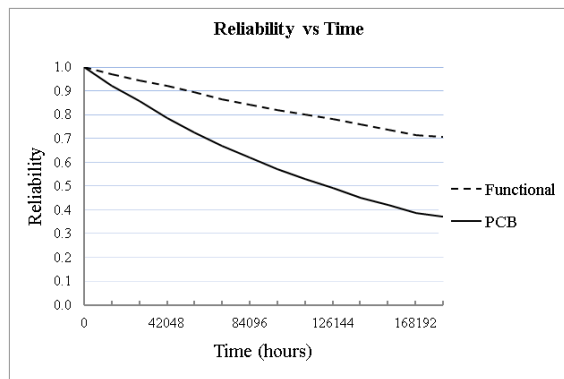


Figure 4. System reliability calculation of the PCB based implementation.

Moreover, the MTTR of the RFD is much longer than the allowed time (minutes versus milliseconds) hence resulting in a much worse availability. And there is no way to achieve a MDT of 50 ms for the core function (beamforming) on the RFD.

In conclusion, the system implemented on a PCB using several stand-alone SoCs has a much lower specification in terms of dependability. Changes must be made concerning the implementation method to meet the specified dependability requirements.

D. Dependability evaluation of a single chip implementation

To meet the functional dependability requirements, a new implementation method for the beamforming system has been proposed. The new method will require the UMC 32 nm processing technology and integrate all the processing elements into one single SoC to circumvent the low reliability of the PCB and availability.

A block diagram showing the major functional elements of the proposed single chip implementation is given in Fig. 5. An 8×8 array of 64 Xentium tile processors (blue “tiles” in the figure) and 1 GPP are included in the SoC. A network-on-chip (NoC) is adopted as the communication backbone (the orange lines) among each part. Xentium tile processors are connected to the NoC routers (the blue “dots” at each intersection of the NoC) via a network interface [13].

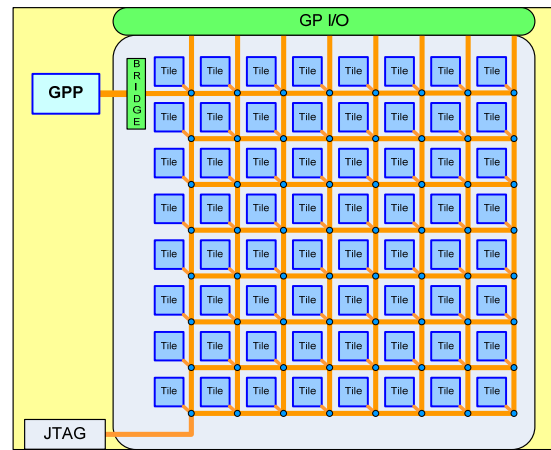


Figure 5. Proposed single IC implementation of the beamforming system.

Since the beamforming system will be implemented in a single chip, the PCB block is removed when calculating the overall system reliability in BlockSim. The result is shown in Fig. 6. A noticeable reliability improvement can be observed compared to the PCB based implementation. However, it is still lower than the minimum reliability requirement from the functional dependability specification. The reliability still needs to be improved.

Moreover, no maintenance work can be carried out in a traditional IC, which means the maintainability of the

proposed implementation is close to zero. And the 50 ms MDT for the beamforming cannot be achieved. Therefore, one needs to add dedicated DfD hardware in the single SoC implementation to meet the expected functional dependability requirements.

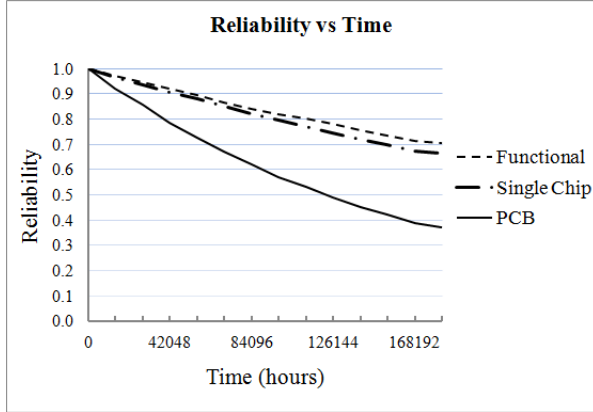


Figure 6. System reliability calculation of the single IC implementation.

IV. THE DEPENDABLE SINGLE SOC FOR THE BEAMFORMING APPLICATION

A. Dependability requirements analysis

Since the calculated reliability of the single chip implementation still does not meet the minimum functional reliability requirement, a reliability improvement is necessary. This can be achieved by considering the extra reconfigurable Xentium tile processors in the SoC as spare resources. Note that in an advanced version of our approach, also processors which are not fully utilized can be (partly) considered as such. The whole system actually becomes a redundant system and the reliability can be enhanced in this case. This idea is feasible because of the chip-level maintainability feature.

As introduced in section II, system maintainability automatically involves the needs for fault detection and fault correction procedures. In the case of a dependable single chip implementation for the beamforming system, dedicated hardware and software need to be designed and included in the target SoC to guarantee chip-level dependability. We will refer to this dedicated hardware as the infrastructural IP (IIP) in this paper.

The IIP has two essential missions: built-in self-test/self-diagnosis (BIST) and built-in self-repair (BISR). The quantitative measurements for these two tasks are Mean Time To Detection (MTTD) and Mean Time To Repair (MTTR) respectively. In the context of this paper, the Mean Down Time (MDT) should actually be interpreted as the “mean malfunction time”. On the other hand MUT is the abbreviation of Mean Up Time, where the system is available. When a fault occurs in one of the reconfigurable Xentium tile processors, the system will enter a

malfunction status and cannot provide correct service anymore. The average period of time, from the fault occurs till it is detected and corrected so that the system can again provide correct service, is defined as the MDT. Fig. 7 shows the fault detection and correction scenario; it is clear that $MDT = MTTD + MTTR$.

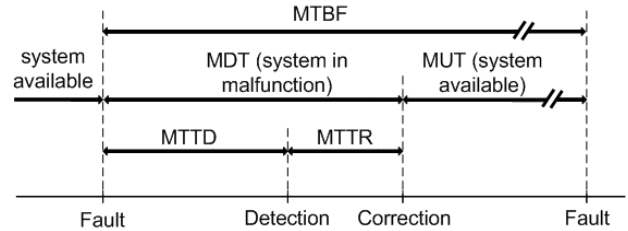


Figure 7. Fault detection and correction timing analysis [9].

Since the MTTR is quite short in our special case (1 ms can be achieved) due to the fast reconfiguration capability of the run-time mapping software [14], the MDT is almost equal to MTTD. Hence a MTTD less than 50 ms has to be guaranteed in order to meet the functional dependability requirements.

B. SoC architectural overview

The architecture of the improved SoC with IIP is shown in Fig. 8. An array of 64 reconfigurable Xentium tile processors is incorporated. An additional GPP is also proposed to be included compared to the SoC in Fig. 5 as its correct operation is vital. It will be used as a “spare” block which will further enhance the reliability of the overall system. The IIP, which is used for dependability improvement, consists of a test pattern generator (TPG) and a test response evaluator (TRE) with a finite state machine (FSM) coordinating their activities. A JTAG (IEEE 1500 compatible) interface for external access to the IIP and wrappers is also included.

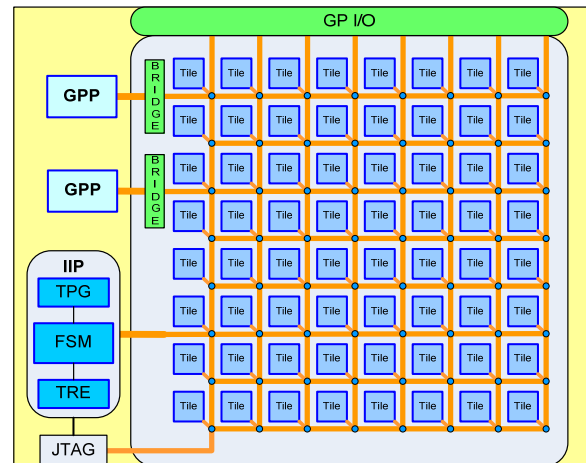


Figure 8. Single chip implementation of the beamforming system with IIP.

The IIP communicates with the reconfigurable tile processors and the GPP via the NoC. It means that besides transmitting data for the application, the NoC is also reused as a test access mechanism (TAM). It delivers the test stimuli generated by the TPG to the tile processors and transfers the corresponding test responses back to the TRE.

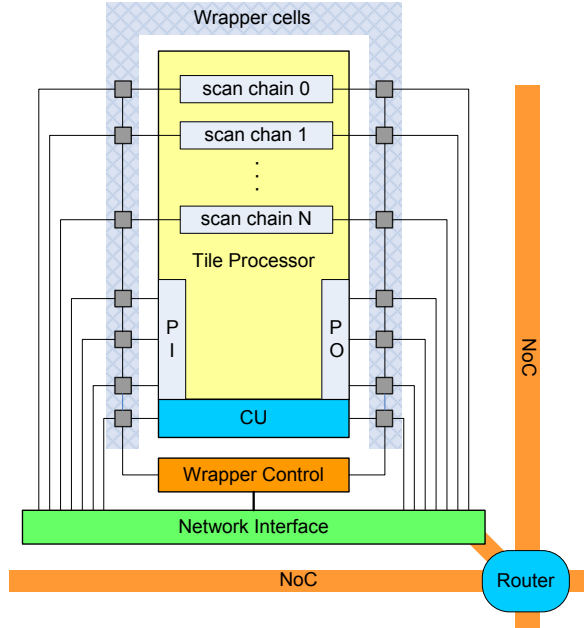


Figure 9. Reconfigurable Xentium tile processor is surrounded by wrapper cells and connected to the NoC via a network interface.

A closer look of a tile processor connected to the NoC is shown in Fig. 9. The processor and its reconfiguration unit (CU) are surrounded by a chain of wrapper cells which comply with the of IEEE 1500 standard. The wrapper cells take control of the input and output pins of the tile processor and can set the processor in a normal operation mode or an “in-test” mode when necessary.

In the normal operation mode, the wrappers are transparent and the input/output of the tile processors are connected to the NoC via the network interface. In the “in-test” mode, the tile processor is isolated from the normal input data but the test stimuli are applied to its internal parallel scan-chains. The test responses are collected and transferred to the TRE via the NoC.

C. IIP operational capabilities

The basic idea for testing the reconfigurable tile processors is based on the multi-voting principle. Since the reconfigurable tile processors all have identical hardware structures, the same responses can be expected when the same stimuli are applied to them. A faulty tile processor, however, will generate different responses due to the internal fault and thus can be detected.

At the end of the design phase, deterministic test patterns for testing structural faults are generated for the

reconfigurable Xentium tile processors using a commercial ATPG (Automatic Test Pattern Generation) tool TetraMAX from Synopsys. Parallel scan-chains are inserted into the processor. Since very little storage space is available for dependability related task within the SoC, the test patterns will have to be regenerated at run time. This test pattern regeneration mission can be achieved by using a linear feedback shift register (LFSR) combined with the bit-flipping technique [15].

The testing software in the IIP will periodically pick out 3 operating tile processors (core-under-test, CUT) at a time for fault detection. The run-time mapping software will map another 3 spare processors to take over the running tasks of those CUTs therefore the testing task can be carried out at run time and system operation will not be interrupted.

The test stimuli generated by the TPG will be broadcast to the 3 CUTs (set to “in-test” mode by the test manager) via the NoC. The test responses will be collected by the TRE. A bit to bit comparison of the responses from the 3 tiles will take place in the TRE to verify whether the results from each tile are identical. If so, the three tile processors are considered as fault-free as the possibility of 3 processors become defective at the same time with the same types of stuck-at faults, thus yielding the same derived responses, is extremely low. A detailed design approach of the TRE has been published in [7].

In normal case, one tile processor could become faulty and will therefore generate different test responses from the other two. This difference can be identified by the TRE and the processor will be considered as faulty. The fault correction procedures will immediately follow to flag the faulty tile processor and it will not be treated as a usable resource by the run-time mapping software anymore. Once this fault correction procedure is completed, the system will be considered as functionally correct again and the malfunction status ends.

This fault detection flow needs to be repeated at least once for all the 54 working tile processors in every 50 ms so that when a fault occurs in one tile processor, it always takes less than 50 ms to detect and correct it. The 54 tiles processors can be divided into 18 groups. Given the 50 ms time period, about 2.7 ms is allowed for each group.

The tasks required to be carried out within the 2.7 ms include: reconfiguration of CUT from the current system (this can be finished within 1 ms), test pattern generation and test response evaluation. The latter two tasks can be completed within 1 ms or more depending on the fault coverage needs to be achieved. In general, the 50 ms MTTD, thus MDT, can be guaranteed.

D. Dependability evaluation

As already discussed, the MDT requirement can be met by restricting appropriate test time to test the tile processors. Since the mean repair time is extremely low (milliseconds)

compared to the time when the system is available (hundred thousands of hours), the availability of the system is near 100%.

In addition, a reliability improvement is achieved due to the on-chip maintainability feature. A MTBF of 6 million hours is achieved for the reconfigurable tile processors considering the redundant reconfigurable tile processors. In Fig. 10, calculations show that the system reliability has been increased and the functional reliability requirement can be well met.

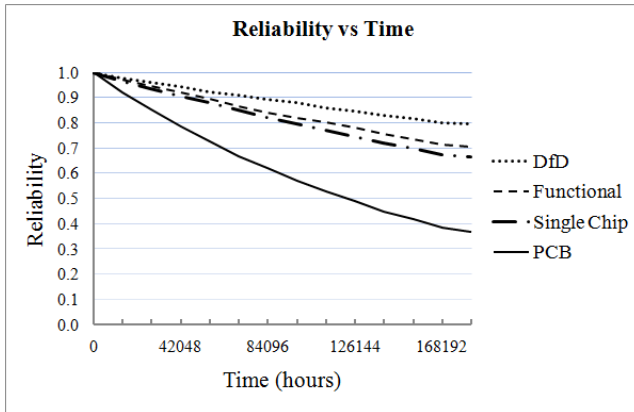


Figure 10. System reliability improvement with the DfD infrastructures.

V. CONCLUSIONS

In this paper, the dependability of an advanced beamforming system was analyzed from a functional perspective using actual dependability requirement data. Reliability, availability and maintainability requirements were provided in a quantitative form.

Next, the dependability attributes of one possible implementation, being a PCB-based implementation with several chips, have been calculated using the actual data of the chips. The calculated reliability was too low to meet all functional dependability requirements. This has been improved by implementing the system as a single SoC.

With the design for dependability infrastructure (IIP) included in the original SoC, the reliability of the whole system was further enhanced. In addition, the availability and maintainability specifications were also satisfied.

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REFERENCES

- [1] "UMC claims move to metal-gate process for 32nm", <http://kn.theiet.org/news/nov08/umc-metal.cfm>, Published on 26 November 2008.
- [2] M. Takamita, "Challenges to Dependable VLSIs", *44th meetings of IFIP working group 10.4 on dependable computing and fault tolerance, workshop on "Hardware Design and Dependability"*, Jun. 28, 2003.
- [3] P. Gepner and M. F. Kowalik, "Multi-Core Processors: New Way to Achieve High System Performance", *Parallel Computing in Electrical Engineering, 2006*, pp.9-13.
- [4] P.M. Heesters, "Coarse-Grained Reconfigurable Processors – Flexibility meets Efficiency", PhD. thesis, University of Twente, 2004, ISBN 90-365-2076-2.
- [5] Recore Systems, www.recoresystems.com
- [6] H.G. Kerkhoff and J.J.M Huijts, "Testing of a Highly Reconfigurable Processor Core for Dependable Data Streaming Applications", *IEEE DELTA08*, Hong Kong, Jan. 2008, pp. 38-44.
- [7] O.J. Kuiken, X. Zhang and H. G. Kerkhoff, "Built-In Self-Diagnostics for a NoC-Based Reconfigurable IC for Dependable Beamforming Applications", *Defect and Fault Tolerance of VLSI Systems, 2008*. Oct. 1-3, 2008, pp. 45-53.
- [8] IEC standard 62347, "Guidance on system dependability specifications", Nov. 11, 2006.
- [9] IEC standard 60300-3-4, "Application guide to the specification of dependability requirements", Sep. 1, 2007.
- [10] From Realsoft, <http://www.reliasoft.com/>.
- [11] J. W. McPherson, "Reliability challenges for 45nm and beyond", in *Proceedings for the 43rd Annual Design Automation Conference (DAC)*, June 2006.
- [12] ARM Ltd, "ARM9 family", <http://www.arm.com/products/CPUs/families/ARM9FaFami.html>, Dec. 2008.
- [13] H. G. Kerkhoff, O. J. Kuiken and X. Zhang, "Increasing SoC Dependability via Known Good Tile NoC Testing", *The 38th Annual IEEE/IFIP International Conference on Dependable Systems and Networks, DSN 08*, supplemental volume, Anchorage, USA, Jun. 24-27, 2008.
- [14] L. T. Smit, G. J. M. Smit, J. L. Hurink, H. Broersma, D. Paulusma, and P. T. Wolkotte, "Run-time assignment of tasks to multiple heterogeneous processors", in *Proceedings of the 4rd PROGRESS workshop on embedded systems*, Oct. 2004, pp. 185-192.
- [15] G. Kiefer; H. Vranken; E. J. Marinissen; H.-J. Wunderlich, "Application of deterministic logic BIST on industrial circuits," in *Proceedings of the International Test Conference 2000*, pp. 105-114, 2000.