Substrate Bounce in Mixed-Mode CMOS ICs

Bram Nauta* and Gian Hoogzaad.

Philips Research Laboratories, Eindhoven, The Netherlands.

* Now with University of Twente, Enschede, The Netherlands

1 ABSTRACT

Substrate noise is one of the key problems in mixed analog/digital ICs. Although measures are known to reduce substrate noise, the noise will never be completely eliminated since this requires larger chip area and thus higher cost. Analog circuits on digital ICs simply have to be resistant to substrate noise. A general strategy is given which can be summarized as: the *supply* of the analog circuits must be referred to the substrate and the analog *signals* must be referred to a clean analog ground. Furthermore several design constraints are given to minimize the effect of substrate noise on analog. Two bandgap circuits are discussed and it is shown that apparently minor design issues, such as the connection of an n-well of a PMOS differential pair, can have large impact on the substrate sensitivity of this circuit. This has been verified by measurements.

2 INTRODUCTION

One of the major challenges in mixed signal IC design is to deal with substrate noise and crosstalk problems. Especially in CMOS technology the problems are serious, since both analog and digital share the same - low ohmic - substrate. As the switching speed and packing density of digital CMOS increases, and the supply voltage drops, it's more and more difficult to design analog modules with good performance. For example it is not trivial to design a 10 bit video ADC (1LSB = 1mV) or to design a low-jitter PLL while there is 300mV substrate noise.

This paper[1] describes briefly the origin of substrate noise (section 3), followed by an example of a simple current source to illustrate the problems in analog (section 4). In section 5a general substrate strategy for analog is given and in section 6 a practical example is given on what can go wrong with the design of a simple CMOS bandgap reference. Finally conclusions are drawn.

3 SUBSTRATE NOISE

Figure 1 shows a well known cross section of a standard CMOS IC. The substrate is very low-ohmic (say 0.01 Ohm cm) on top of which an epi-layer is grown. This epi-layer is several micrometers thick and has a higher resistance (say 10 Ohm cm). On this low-ohmic substrate both analog and digital circuits are located, and due to the low substrate resistance this causes crosstalk problems. Now a brief explanation of the origin of the substrate noise is given.

In figure 2 schematically the typical power routing of a digital CMOS IC is shown. The digital part of the IC is here simplified to a (huge) inverter. The digital part has its own VDDD and VSSD pins. The CMOS logic is switching and this means current spikes through the VDDD and VSSD pins. The current spikes are due to (dis)charging of capacitances and short circuit current as present in CMOS gates [1]. In the digital standard cells normally substrate contacts are present for latch-up reasons. A single substrate contact has a resistance of several kOhms, however on a large IC with - say 500k - gates, the substrate is

1. This work has been published before at the , ETTCD'97 conference, August 1997. Budapest, Hungary.

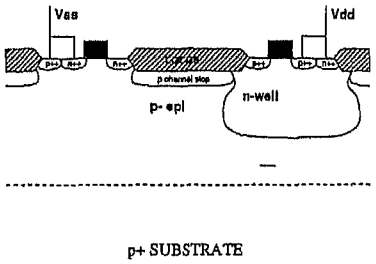

Figure 1: cross section of a p-substrate p-epi CMOS IC

very well connected to VSSD. The problem is now the self inductance of the VDDD and - more serious for analog - the self inductance of the VSSD pins. The self inductance of a single bondwire is typically 5nH and the resulting voltage drop over the VSSD bondwire is $V_{bondwire} = L_{vssd} * d_{Iss}/dt$. In a system the PCB (Printed Circuit Board) ground is usually the reference for analog and digital circuits and thus the substrate noise is equal to $V_{bondwire}$ [2].

If no precautions are taken then substrate noise can be several Volts. However in this case even pure digital circuits will not operate correctly. A practical method to limit substrate noise is to decouple the digital supplies with on-chip capacitors (as denoted with Cdd in figure 2). If these capacitors are large enough then the peak currents needed are drawn from these capacitors. A problem is that these capacitors need area, and are thus expensive. Furthermore the series resistance of these capacitors must be low (the RC time constants must be in the GHz range). Consequently the capacitors must be merged with the logic. Another problem with these capacitances is the LC-resonance effect with the inductance of the bondwire. Therefore a series resistance (as denoted with Rdd in figure 2) must be present to damp the oscillations [2]. Rdd can be a parasitic metal resistance in the VDDD path. Another option to limit substrate noise is to use many VSSD pins. Usually many VDDD pins are also needed for correct operation of the digital

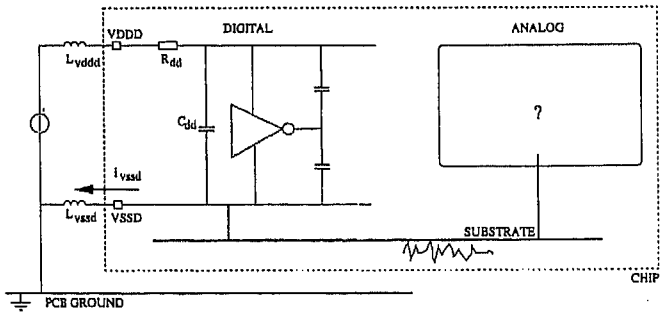

Figure 2: The origin of substrate noise: switching of digital circuits result in dI_VSSD/dt, and thus in a voltage drop over the VSSD bondwire.

part and separate supply pins for the digital I/O are used. Also lowering the digital supply voltage will help to reduce the substrate noise, however at the penalty of speed. It can also be shown that the internal digital supplies are oscillating in antiphase[3]. Disconnecting substrate contacts from the digital Vss and balancing the capacitance of the substrate to both supplies is a possibility to suppress groundbounce [3]. However this requires knowledge about existing capacitance within the circuit in any state. Furtermore digital librariy cells with a separate substrate rail are needed, (to prevent latch-up) which consumes more chip area.

Substrate noise can thus be limited, be it at the cost of money; either area, pins or dedicated libraries. Therefore substrate noise will never be reduced to the millivolt level. Always some $300mV_{pp}$ will be present, dictated by proper functioning of the digital part. Even so, in general the frequency content of the substrate noise is not known, because of multiple clock domains on the same IC.

Guard rings for shielding the analog part from the digital substrate have no effect in CMOS with a low-ohmic substrate [4]. It's the same as building a fence around your house to keep it safe from earthquakes: the substrate noise comes from the bottom of the analog circuit. Sub-

strate noise will simply be there, and the analog circuitry must therefore simply be able to deal with this interference.

4 PROBLEMS IN ANALOG

In this section the problems in analog will be discussed. Since analog circuits share the same substrate these circuits will always be affected by substrate noise. three mechanisms can be distinguished;

1) *direct incoupling*. The - normally - high frequency substrate signal couples directly into the analog circuit. If the frequency content of the substrate signal is outside the signal band in the analog part, this needs not to be harmful as long as the analog circuit behaves like a linear circuit. This behaviour can be investigated in an AC simulation. Unfortunately true linear circuits are rare.

2) *demodulation*. If a substrate signal couples into an analog circuit which contains non-linear elements (which is normally the case) then demodulation can occur. Even if the frequency content of the substrate noise is outside the signal band, demodulation or AM detection can result in noise in the signal band of the analog circuit. An example of this is described in section 6, where substrate noise in a bandgap reference circuit results in a DC shift of the output voltage. Transient analyses are needed to tackle these problems.

3) *sampling*. In a mixed-signal IC normally an AD converter is present, which means a sampling operation on the analog signal. If substrate noise has coupled into the analog circuits preceding the AD converter (Clamp, AGC, filter, buffer, etc.) at a frequency outside the signal frequency band, this sampling operation will fold the substrate noise back into the signal band.

In conclusion it can be mentioned that analog modules and circuits must have a good rejection for substrate signals. The rest of this paper discusses how this can be achieved.

Consider a very simple analog circuit like the current source in figure 3a. The current source is supplied with a clean analog VSS (analog ground) and the gate has a parasitic capacitance Cgate. Due to the na-

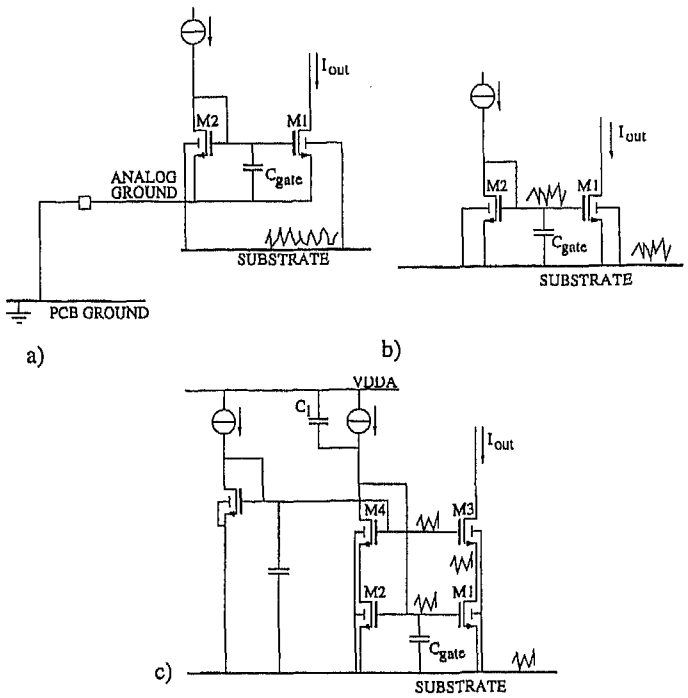

figure 3: example to illustrate the effect of substrate noise on analog circuits a) current source, realized by a current mirror, with a clean VSSA. b) improvement of the current source of 3a) with VSSA connected to the substrate c) improvement of the current source of 3b) by means of small cascode transistors

ture of the CMOS process, the backgate of M1 is coupled to the substrate. For high frequencies the Vgs of the MOST is fixed due to Cgate, and the substrate noise on the backgate directly modulates the drain current of M1. It is therefore better not to use a clean analog ground, but to use a VSS, equal to local substrate voltage. This is shown in fig-

ure 3b. The AC content of the substrate noise is now present on the gate, source and backgate of M1. The drain is not coupled to the substrate and the substrate noise couples only via the drain-bulk and drain-source admittances. This is better than coupling via the backgate. For noise and matching reasons the dimensions of M1 and M2 are normally far from the minimum as dictated by the technology, resulting in still a large drain-bulk capacitance of M1 and M2. For this reason the current source is often provided with cascode transistors. Figure 3c illustrates how these cascode transistors should be biased in order to have small substrate sensitivity. Now the drain, gate, source and backgate of M1 and the gate, source and backgate of M3 have the same AC (substrate) signals. The output impedance of the current source is high including the capacitance since M3 can have small dimensions. Note that the capacitance C1 should be kept small for good substrate rejection.

Thus by choosing the right references, in this case the substrate for NMOS transistors, performance can be improved. In the next section a more general approach will be given.

5 STRATEGY FOR ANALOG

In this section several design rules are given to make circuits for analog signal processing less sensitive for substrate noise.

- Use NMOS transistors only as DC current sources. These NMOS transistors should be referred to the substrate and not to a clean VSS.
- Use PMOS transistors for signal handling: i.e. PMOS as differential pairs and signal handling current mirrors. PMOS transistors have an n-well which can be used to shield the transistor from the substrate. Be sure to put enough well contacts to the VDDA, and be aware of series resistances in the well, which are normally not properly modeled.
- Make analog circuits fully differential, with a possibly clean common mode level. A common mode control circuit must suppress interference. Matching and large signal behaviour is still limiting the effect of balancing.
- Use shielding of resistors and wires only for signals not referred to the substrate. Shielding can be done with n-well, poly or one of the lower

metal layers, connected to VDDA. Be careful with series resistances in n-well and high-ohmic poly, since the RC time constant will limit the effect of shielding. Bondpads carrying analog signals can be shielded with n-well.

The remaining problem is now the analog interface. Analog signals are usually single-ended and defined w.r.t. the "clean" PCB ground. Inside the IC large parts of the analog circuits are referred to the substrate (all NMOS) and the signals are differential. This makes interfacing a serious matter.

Figure 4 shows the recommended supply and reference routing for a mixed-signal IC. The digital part has several VDDD and VSSD pins, and the substrate is contacted to VSSD in the digital part as mentioned before. The analog part has a separate VDDA, since VDDD will be polluted by the digital. The VSS of analog (VSSA) should be connected to the substrate with enough substrate contacts, and should contain the same signal as the substrate. VSSA is thus NOT clean w.r.t. PCB ground, and there is actually no difference between VSSA and VSSD. In order to interface with the outside world of the IC, a clean reference signal on chip is needed. This signal is denoted as "analog ground". Analog ground is connected to PCB ground via a bondwire and thus di/dt of this bondwire must be (almost) zero. The pin of analog ground therefore may only carry DC signals or signals with relatively low frequencies, depending on the demands. The analog ground wires on chip, must be shielded from the substrate (with n-well or lower interconnect layers, connected to VDDA) and no unwanted signals ought to couple into analog ground.

The input signal is referred to PCB ground and is fed into a first stage on the IC, which is, in the example of figure 4, a transconductance amplifier. Important is that this first stage has analog ground as a reference for the signal. The output of the first stage is preferably differential, in order to be less sensitive to substrate or supply noise. The common mode level of the differential signals should be clean. After optional analog preprocessing the analog signal can be converted to the digital domain for further signal processing. The signal can be converted into the analog domain via a DA converter and may be followed by postprocessing functions, such as smooth filtering. The differential

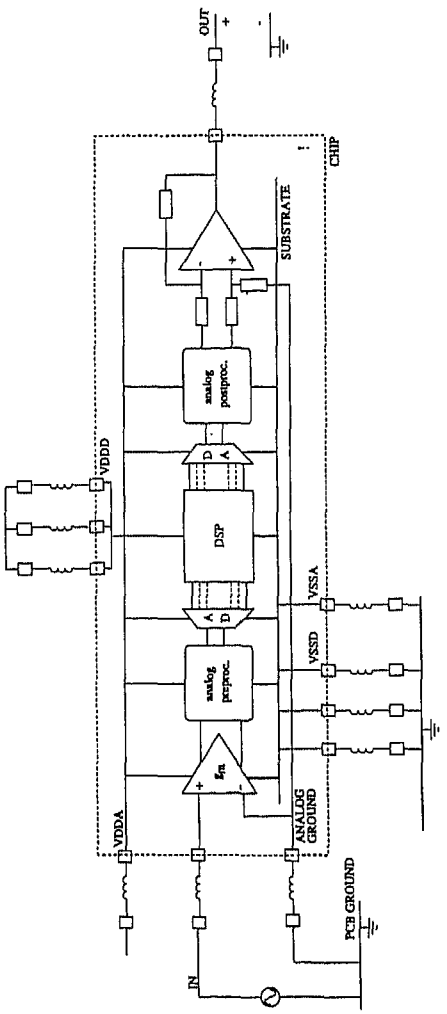

Figure 4. recommended supply and reference routing for a mixed signal IC.

signal must be converted to a single-ended signal referred to analog ground. This is also illustrated in figure 4. It would even be better if the "outside world" signals of the IC are differential, however this is often not feasible for cost reasons.

Summarizing it can be said that: the supply of the circuits are referred to the substrate and the signals are referred to a clean analog ground.

6 EXAMPLES

In this section a practical example of the effect of substrate noise on a bandgap circuit is illustrated. Figure 5a shows a well known bandgap voltage reference [5], generating a reference voltage V_{bg} with respect to the substrate. This means that the output voltage of the bandgap circuit V_{bg} is constant w.r.t. the substrate. (and thus not constant w.r.t. analog ground, if there is substrate noise). The core of the circuit is R1,R2, R3, Q1 and Q2. The folded cascode amplifier (all MOSFETS) is responsible for the proper feedback, needed for correct bandgap operation. This bandgap is denoted here as bandgap "A"

For correct operation of bandgap A, all NMOS transistors are referred to the substrate, as illustrated in the example of a current mirror of figure 3b. The bases of the parasitic vertical pnp transistors are also connected to the substrate. In order to keep the feedback loop stable a capacitor Cc has been added. A further advantage of Cc is that the gate-source voltage of M9 is low-pass filtered, and thus filters more or less incoupling substrate noise.

It appeared to be very important during the evaluations of these types of bandgap circuits how the n-well of the input differential pair is connected. One can connect the n-well to VDDA or to the common source node of the differential pair. Figure 6a shows the simulation results of the two possibilities. The figure shows the bandgap voltage versus time while a 10MHz clock signal of 400mVpp is present on the substrate. If the n-well is connected to the VDDA the bandgap voltage starts drifting away from the nominal value (figure 6a-curve 1). Note that even if the ripple is low-pass filtered, the DC value is not correct and will depend on the substrate noise which is highly unwanted. The explanation is that the base and emitter of Q1 and Q2 follow the substrate noise. So

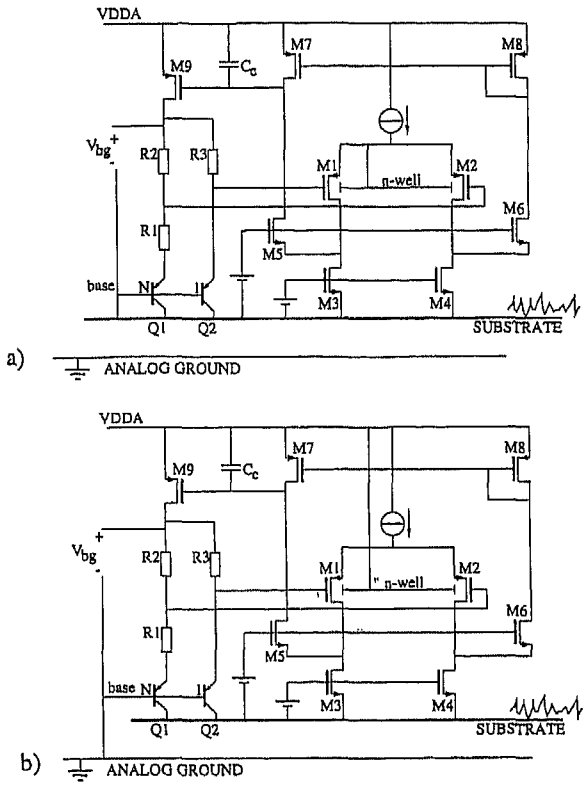

figure 5. a) bandgap type A, generates a reference voltage w.r.t. substrate b) bandgap type B, generates a reference voltage w.r.t. analog ground.

do the gates, sources and drains of M1 and M2. If the n-well is connected to the VDDA, the source-well capacitances of M1 and M2 conduct a current related to the substrate noise and thus modulate the currents of M1 and M2. Due to non-linear effects (see section 4) this results in DC shift of the bandgap voltage. If the n-well is connected to

the common source, as shown in figure 5a, then all terminals (drain , gate, source and well) of M1 and M2 have the same substrate-related signal and the modulation does not occur. Important is that the capacitance from common source to VDDA is held small. The results of the simulations with n-well connected to the common source node is shown in figure 6a, curve 2.

The other bandgap - type B - is shown in figure 5b. The reference voltage is now wanted w.r.t. the "clean" analog ground, and the bases of Q1 and Q2 are now connected to this analog ground. If the n-well of the differential pair M1, M2 would be connected to the common source node, then the bandgap voltage would drift away as shown in figure 6b, curve 1. This is because the n-well to substrate capacitance picks up the substrate noise and pollutes the common source node, which should not follow the substrate noise in this case. The result is again modulation of the currents in M1 and M2. The correct connection of the n-well in bandgap B is to the VDDA. Now the main terminals of M1 and M2 (gate, source, well) are "clean". The noise picked up by the n-well is routed towards VDDA. The resulting simulations are given in figure 6b, curve 2.

The simulations have been verified by measurements on a large mixed-signal IC. Figure 7 shows a measured reference voltage, derived from a bandgap circuit. The reference voltage is plotted as a function of the clock frequency of the IC. For the wrong n-well connection the reference shows a large deviation around 10MHz clock for 3 samples of the IC (curves 1). We modified the connection with a FIB (Focussed Ion Beam) station on the 3 samples and the result is clear! (curves 2)

7 CONCLUSIONS

Substrate noise is one of the key problems in mixed analog/digital ICs. Although measures are known to reduce substrate noise, the noise will never be completely eliminated for cost reasons. Analog circuits on digital ICs simply have to be resistant to substrate noise. A general strategy has been given which can be summarized as: the analog circuits must be referred to the substrate and the analog signals are referred to a clean analog ground. Furthermore several design constraints are given to minimize the effect of substrate noise on analog. Two

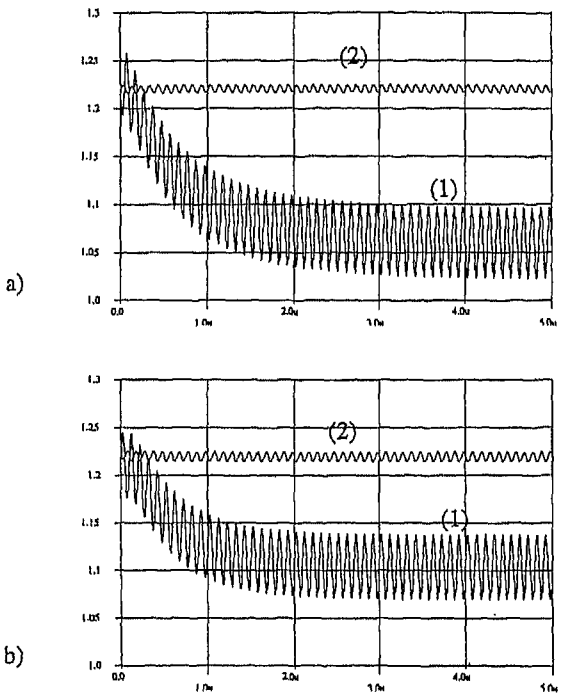

figure 6 Simulation results of the bandgap reference. a) Bandgap circuit A, with output referred to the substrate. Curve 1 with n-well to VDDA (wrong), curve 2 with n-well to common source node of differential pair (correct). b) Bandgap circuit B, with output referred to the analog ground Curve 1 with n-well to common source node of differential pair (wrong), curve 2 with n-well to VDDA (correct).

bandgap circuits have been discussed and it has been shown that apparently minor design issues, such as the connection of an n-well of a PMOS differential pair, can have large impact on the substrate sensi-

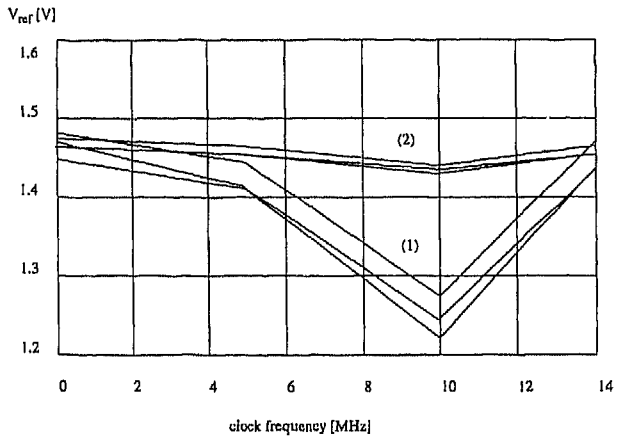

Figure 7.Measured reference voltage, derived from a bandgap circuit as a function of the clock frequency of the IC. curves (1) wrong n-well connection, curve (2) correct n-well connection.

tivity of this circuit. This has been verified with measurements.

Acknowledgment: The techniques and results described in this paper are a result of the contributions of many colleagues within Philips Research and Philips Semiconductors. We wish to thank these colleagues for their contributions. Special thanks are given to W. Relyveld for doing the bandgap simulations.

8 References

[1] H.J.M. Veendrick, "Short-Circuit Dissipation of Static CMOS Circuitry and its Impact on the Design of Buffer Circuits", IEEE Journal of Solid-State Circuits, Vol. SC-19, August 1984, pp 468-473.

[2] D.W.J. Groeneveld, "Groundbounce in CMOS", Digest of technical papers, workshop on Advances in Analog Circuit design, Leuven 1993.

[3] T.J. Schmerbeck, R.A. Richetta and L.D. Smith, "A 27MHz Mixed Analog/Digital Magnetic Recording DSP Using Partial Response Signalling with Maximum Likelihood Detection", Digest of technical papers, ISSCC 1991,, Feb 1991, pp 136-137.

[4] D.K. Su, M.J. Loinaz, S. Masui, B.A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", IEEE Journal of Solid-State Circuits, Vol. 28, No. 4, April 1993, pp420-430.

[5] K.E. Kuijk, "A reference voltage source" IEEE Journal of Solid-State Circuits, vol SC-8, pp 222-226, June 1973..