# Energy Model of Networks-on-Chip and a Bus

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***Abstract*— A Network-on-Chip (NoC) is an energy-efficient on-chip communication architecture for Multi-Processor System-on-Chip (MPSoC) architectures. In earlier papers we proposed two Network-on-Chip architectures based on packet-switching and circuit-switching. In this paper we derive an energy model for both NoC architectures to predict their energy consumption per transported bit. Both architectures are also compared with a traditional bus architecture. The energy model is primarily needed to find a near optimal run-time mapping (from an energy point of view) of inter-process communication to NoC links.**

## I. Introduction

In the Smart chipS for Smart Surroundings (4S) project [1] we propose a heterogeneous Multi-Processor System-on-Chip (MPSoC) architecture with run-time software and tools. The MPSoC architecture consists of a heterogeneous set of processing tiles interconnected by a Network-on-Chip (NoC) as depicted in Figure 1. The size of a processing tile is assumed to be less then 5 $mm^2$ in 0.13 $\mu m$ technology. By exploiting the available parallelism of the processing tiles they can run at a relatively low frequency (below 500 MHz) to achieve enough performance. The architecture including the run-time software can replace inflexible ASICs for future mobile systems.

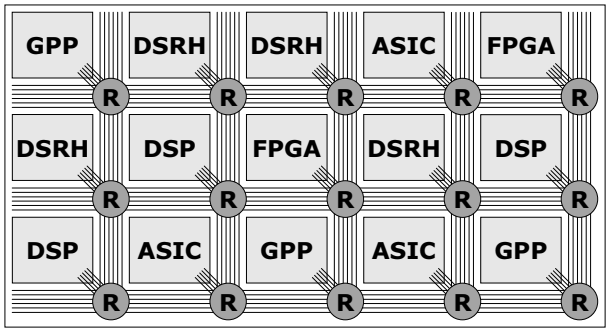


Fig. 1. An example of a heterogeneous System-on-Chip (SoC) with a Network-on-Chip (NoC). DSRH = Domain Specific Reconfigurable Hardware

Mobile systems are typically battery powered and have to support a wide range of applications so they have to be flexible as well as energy-efficient. We consider a set of streaming applications that run for a considerable period (seconds and more): e.g. wireless baseband processing (DAB, DRM, DVB), multi-media processing (MPEG-2, MPEG-4). To map these applications on a parallel architecture like a MPSoC we assume the application is represented as communicating parallel processes. One possible representation is a Kahn based process graph model [2], which is a directed graph with nodes representing sequential processes and edges representing FIFO communication between processes.

The MPSoC architecture of the 4S-project is controlled by a central operating system called OSYRES [3], that runs on one of the GPPs of the MPSoC. The main task of OSYRES is to manage the system resources. It tries to satisfy Quality of Service (QoS) requirements, to optimize the resources usage and to minimize the energy consumption.

To reduce the energy consumption of the overall application we map the processes on the processing tile that can execute it most efficiently. This spatial mapping of processes is performed at run-time by the spatial mapping tool (SMIT) [4]. OSYRES determines when the spatial mapping tool is called. Due to the mapping of processes to processing tiles on the MPSoC communication is introduced, because data has to be moved to the successive processing tiles.

Traditionally communication between processing tiles is based on a shared bus. But for larger MPSoC with many processing tiles it is expected that the bus will become a bottleneck from both a performance, scalability and energy point of view [5]. Therefore, we propose a multi-hop Network-on-Chip, where the network consists of a set of routers interconnected by links.

In this paper we will derive a simple energy model of two Network-on-Chip architectures. This is primarily needed for the spatial mapping tool. Using this model the tool can find a near-optimal mapping (from an energy point of view) of of inter-process communication to NoC links. Therefore a first-order estimation of the energy consumption is needed and sufficient. A complicated energy model would hamper the spatial mapping tool. A second motivation of deriving an energy model is that we can compare different NoC options (see also section IV). We compare the energy consumption of a solution based on a packet-switched wormhole router with virtual channels, a circuit-switched router with a separate best effort network and a traditional bus.

One of the first power modeling tool was Orion, a cycle-accurate network power-performance simulator, that was proposed in [6]. The capacitance of each network component is derived based on architectural parameters, and activities at each cycle trigger calculations of network power.

The rest of this paper is organized as follows. The evaluated network routers are briefly described in section II. The energy consumption of the logic can be determined as described

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in section III. This power estimation of the logic does not include the long wires of the links between the routers or wires required in a bus architecture. For the long wires of the communication architecture we use an analytical model of a wire. In section IV we compare the derived energy models of the Network-on-Chip architectures with a traditional bus. In section V we conclude the paper.

## II. Communication Architectures

For the NoC we defined two networks (packet-switched and circuit-switched) that can both handle guaranteed throughput (GT) traffic and best-effort (BE) traffic. The guaranteed throughput traffic is defined as data streams that have a guaranteed throughput and a bounded latency. The best-effort traffic is defined as traffic where neither throughput nor latency is guaranteed. The BE traffic handles traffic like configuration data, interrupts, status messages etc.

### A. Packet-Switched Network

The packet switching router implements wormhole switching with virtual channel flow control. The advantage of wormhole routing is the packet-size independent buffer-size. The virtual channels are used to decrease the chance of blocking and enables the routing of guaranteed throughput traffic.

The packet-switched router described by Kavaldjiev [7] has five input and five output ports and four virtual channels (VCs) per port. The flits (atomic unit) of a packet are labeled with their virtual channel number and they are buffered in four flit deep queues at the input ports. Per port four queues are available - one queue per virtual channel.

The access to the crossbar is arbitrated by 5 round-robin arbiters - one arbiter per crossbar output. This arbitration is sufficient since a conflict can only arise when more than one queue contains flits destined to a same output port. Due to the predictable round-robin arbitration the router is able to handle guaranteed throughput traffic if one single data stream is assigned to a VC.

The best-effort packets can be assigned to the same output VC. All of the packets competing for a same output VC are tagged by the sender with an unique identifier. Each router has a global counter that counts permanently and whose value is distributed to all inputs. When an output VC is freed the next packet that takes it is the one whose id equals the current counter value. The uniqueness of the id guaranties conflict free arbitration, but does not guarantee bandwidth or latency. Since, at any time, the counter value is generally random, fairness is provided.

### B. Circuit-Switched Network

The second network is a guaranteed throughput circuit-switched router [8] in combination with a separate best-effort network [9]. By using dedicated techniques for both types of traffic (BE and GT) we can reduce the total area and power consumption.

For the moment the circuit-switched router has five bidirectional ports where one port is connected to a processing tile and four ports via a bi-directional link (16 bit wide per direction) to their neighboring circuit-switched routers. The bi-directional link between two routers consists of uni-directional lanes (e.g. four lanes in each direction). Each lane can be used by a unique data-stream and more than one lane per link increases the flexibility as in time division multiplexed systems. Four lanes of four bits per link have been chosen to reduce the number of wires between routers, but it requires serialization of the 16 bit data items of the processing tiles. The serialization is handled by the data-converter that connects the (16 bit) tile interface to the small (4 bit) lanes.

To minimize energy consumption the circuit switching has fully separated data and control paths and cannot serve best-effort traffic. The best-effort traffic is handled via a separate ring network [9] that can transport packets (16 bit data, 16 bit address) to all the processing tiles and circuit-switched routers. Via the configuration interface of the circuit-switched router a single best-effort packet can configure 1 lane. On average we can transport the reconfiguration data in less than 1 ms over the BE configuration network. This is fast enough, because the configuration of the crossbar will not change frequently due to the long-life guaranteed throughput data streams between processing tiles.

## III. Power Measurements Network Routers

Benchmarking a NoC router is not a trivial task, because as far as we know no general method has been defined for on-chip networks. In this paper the power estimation of the logic is performed by modeling the design in VHDL. The synthesized VHDL-design is then annotated via a set of test-scenarios. We can estimate the power consumption per scenario using Synopsys Power Compiler [10] and the annotated design.

We expect that the power consumption of a single router is at least dependent on four parameters: 1) The average load of every data stream. This varies between 0% and 100% of the available bandwidth of a single lane/link. 2) The amount of bit-flips in the data stream. This varies from no bit-flips (ie. transmitting constant values) to continuous bit-flips. 3) The number of concurrent data streams through the router, which in our case has a maximum equal to the number of lanes or virtual channels (20). 4) The amount of control overhead in the router (e.g. buffers, arbitration)

### A. Used Traffic Patterns

To test the parameter sensitivity of our router we defined a set test-scenarios for traffic patterns. This set has three levels for the number of bit-flips:

- Best case (no bit-flips, transmitting only zeros)
- Worst case (continuous bit-flips)
- Typical case (random data with 50% bit-flips).

Furthermore, to vary the amount of traffic which concurrently traverse the router we defined ten scenarios. The scenarios have a variable number of concurrent data-streams with an variable load between 0% and 100%. The ten scenarios are listed in Table I.

| # | Number of streams | Comment |
|---|---|---|
| 1 | 0 | The router is idle |
| 2 | 1 | Stream from and to other router |
| 3 | 1 | Stream from other router to processing tile |
| 4 | 1 | Stream processing tile to other router |
| 5 | 2 | Combination of 3 and 4 |
| 6 | 3 | Combination of 2, 3 and 4 |
| 7 | 5 | Combination of 5 and three times 2 |
| 8 | 10 | Two times the number of streams of 7 |
| 9 | 15 | Three times the number of streams of 7 |
| 10 | 20 | All the lanes / virtual channels are occupied |

TABLE I
SCENARIO DEFINITIONS

The first scenario is a situation where no-data traverse the router during the time of the simulation. This will give the static offset in the dynamic power consumption. The other scenarios will simulate one or more concurrent data-streams. These scenarios are used to calculate the average energy consumption per bit [pJ/bit] to traverse one single router.

### B. Power measurements

For both network solutions all the 10 scenarios are applied. In each scenario the data-streams use the guaranteed throughput protocol of the router. The configuration information required by both routers are not send to the routers prior to the measurements. After the reservation, the power consumption of the router is measured over 20 kB of data that is offered to the router in a variable time-interval. The variable interval is used to change the average load of the link. For every scenario, load and the amount of bit-flips we measured the power consumption per MHz [$\mu W/MHz$].

The left graph of Figure 2 depicts the dynamic power consumption depending on the offered load for typical data of the packet switched network. The middle graph of Figure 2 depicts the dynamic power consumption of the circuit-switched network + best-effort router depending on the offered load for typical data. The power consumption of the extra required best-effort network is measured with a separate testbench [9]. The power consumption of this small extra router varied between 8.4 and 12.3 $\mu W/MHz$. In this paper we use the measurement of the guaranteed throughput traffic and added the worst-case power consumption of the best-effort network to find the worst-case power consumption of the combination. We noticed a relative high offset in the dynamic power consumption. This could be reduced by including clock-gating to switch-off the inactive lanes. This resulted in the right graph of Figure 2, where the remaining offset is mainly determined by the best-effort network.

## IV. COMPARING COMMUNICATION ARCHITECTURES

In this section we compare the energy consumption of a bus based system with the two described networks. For the power consumption of the wires between the components we use a simple linear model that is derived in [9] and is based on the work of Banerjee [11].

$$P_{link_{dyn}} = (0.39 + 0.12 \cdot l_{wire}) \cdot N_{wires} \cdot L_{link} \quad (1)$$

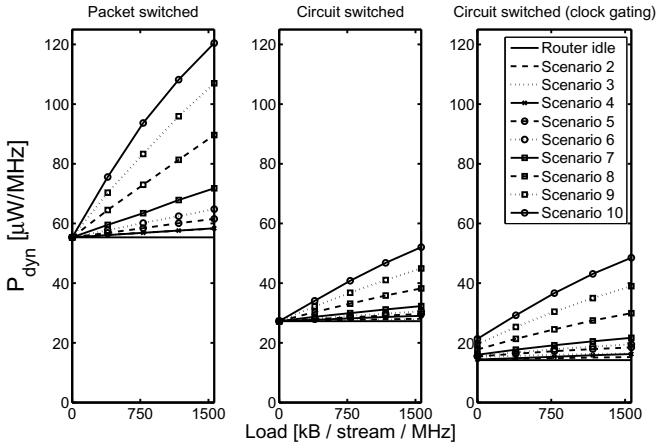


Fig. 2. Energy consumption of routers for typical data (random data with 50% bit-flips)

Where the $l_{wire}$ is the length of the wire in mm, $N_{wires}$ the number of wires and $L_{link}$ the average load of the link. In the next sections we use the energy that is required to transport a single bit over a wire. In these cases the $N_{wires}$ and $L_{link}$ are both equal to 1.

### A. Energy Consumption Model Packet-Switched Router

In Figure 2a we see a high offset in the dynamic power consumption of 55.34 $\mu W/MHz$. Above the offset an almost linear dependency between the load of the streams, number of streams and the power consumption of the router is visible. From this linear dependency (slope of the lines) we derive the amount of energy required for a single bit to pass the router. This is equal to 0.9776 pJ/bit.

The energy consumed by the router can be added to the energy consumption of the wire of equation 1. The dynamic energy ($E_{ps}$ in [pJ/bit]) required to transport a bit between two processing tiles over a distance $N_{hop}$ is equal to:

$$E_{ps} = 0.98 \cdot N_{hop} + (0.39 + 0.12 \cdot l_{wire}) \cdot (N_{hop} - 1) \quad (2)$$

### B. Performance model circuit-switched router

In Figure 2b we see a relative lower offset in the dynamic power consumption of 27.3 $\mu W/MHz$. With the same method as for the packet-switched router we derive the mount of energy required for a single bit to pass the router: 0.3722 pJ/bit, which in combination with equation 1 results the dynamic energy ($E_{cs}$ in [pJ/bit]) to transport a bit between two processing tiles with a distance of $N_{hop}$:

$$E_{cs} = 0.37 \cdot N_{hop} + (0.39 + 0.12 \cdot l_{wire}) \cdot (N_{hop} - 1) \quad (3)$$

### C. Performance model bus

To derive the communication energy required in a (non-tristate) bus we use the analysis used in [12]. It is assumed that the bus system is organized as a regular grid of NxN processing tiles. In a single master bus system it is assumed that all slave-ports have to switch, which results that the data has to be transported over all wire segments. The minimum

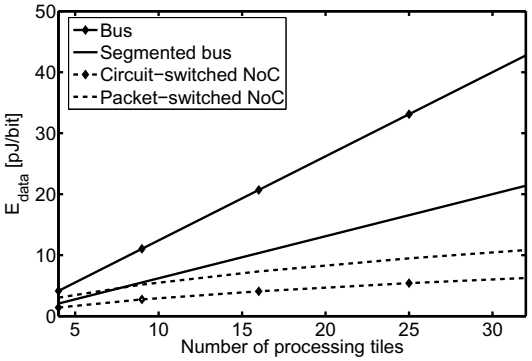


Fig. 3. Energy required for on-chip communication. ($l_{wire} = 2mm$)

number of wire segments to connect all the $N^2$ processing tiles is equal to $N^2 - 1$.

The total amount of switching energy then equals:

$$E_{bus} = (N_{wires}/N_{data}) \cdot E_{wire}(N^2 - 1) \quad (4)$$

Where $N_{wires}/N_{data}$ is the ratio between the number of data lines and the total number of wires (address, data, read, valid and accept flags) of the bus. For a 16 bit data and 16 bit address this ratio is equal to 2.19. Replacing $E_{wire}$ with the energy per bit using equation 1 it results in the energy required to transport one single data-bit:

$$E_{bus} = 2.19 \cdot (0.39 + 0.12 \cdot l_{wire}) \cdot (N^2 - 1)[pJ/bit] \quad (5)$$

### D. Comparison

In section IV-A and IV-B we derived the amount of energy to transport a single bit between processing tiles over a network-on-chip. This bit can be used as an address or data bit by the processing tiles. To make a fair comparison between the networks-on-chip and the bus we assume that 50% of the bits are used for address-bits. The energy required to transport this data bit is therefore twice the energy described by equations 2 and 3.

Using the equation 5 and the compensated equations 2 and 3 we compare the average dynamic energy required to transport a data bit between 2 processing tiles. We assume a regular grid of NxN processing tiles with a size of 4 $mm^2$ each. This will result in a wire segment length ($l_{wire}$) equal to 2 mm. The average number of hops in a network-on-chip communication architecture depends on the distribution of the traffic. For uniform distributed traffic $\overline{N}_{hop} = \frac{2}{3}N$. More local oriented traffic will decrease the average number of hops.

Figure 3 depicts the average required energy per bit depending on the number of tiles in the MPSoC. For the bus we added an extra line, which models a segmented bus structure with 2 equally sized segments. It is assumed that this will half the number of wire segments that are used in a bus-transfer. The benefit of the Network-on-Chip is clearly visible for larger number of tiles.

## V. Conclusion

In this paper we presented two Network-on-Chip architectures that are compared with a traditional bus architecture. For each architecture we derived a simple energy model that can be used for the spatial mapping tool to optimally map the on-chip communication streams. The energy model for all the architectures are relatively simple due to the derived first-order equations.

The energy models showed a lower energy consumption per bit for the Network-on-Chip architectures. Especially for larger number of processing tiles the Network-on-Chip architectures consume less energy per bit. The circuit-switched network is the most energy efficient solution due to the small amount of control and buffering.

For the circuit-switched router a clock-gated implementation was also evaluated. The clock-gated design disabled the clock for in-active (not configured) lanes. The implementation showed a relative large decrease of the offset in dynamic power consumption.

## Acknowledgement

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