Novel test structures for temperature budget determination during wafer processing

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Some process steps during wafer processing demand a carefully applied temperature budget. Novel test structures are presented for monitoring and determining this thermal budget during processing (such as sputtering or etching). Our system is based on well-defined silicidation reactions, simple to read out and enables an easy integration into existing lay-outs.

Post-processing can add many new functionalities to silicon integrated circuits. Several existing solutions and potential examples are mentioned in a review on this topic [1]. The impact of post-processing, however, on the quality and lifetime of the underlying CMOS chips should be carefully monitored and be guaranteed. Temperature is one of the key parameters to be regarded in post-processing. The maximum allowable temperature for post processing is limited to approximately 425° C [1]. For Silicon-On-Insulator (SOI) technology [2] even more care should be taken. Given the poor thermal conducting SiO₂ box layer and the relatively thin, active Si area on top there is a substantial risk for overheating during post-processing. Monitoring of temperature at device level is thus crucial to guarantee the quality of the total device.

During processes at elevated temperatures such as sputtering or etching, however, the measurement of temperature *on the process area of the wafer* is not straight forward. Active temperature measurement equipment can not always be connected to the processed front side of a wafer due to practical limitations. Furthermore, measurement of the wafer backside temperature is not always a proper measure during processing (PVD, etch) as heat capacity and thermal conductivity of Si and SiO₂ layers are involved. In this work we propose an alternative temperature monitoring module for measuring the temperature budget at device level on a wafer during post processing. The fundamental basis for this is to make use of silicidation reactions. Many metals in the periodic table react with silicon to form metal-silicides [3]. For a number of metals these reactions are described in physically and mathematically well-defined steps. By measuring the metal sheet resistance before processing and the resulting sheet resistance of the (partly) formed metal-silicide after processing one can deduce the thermal budget during this step. Van Graven and Wolters demonstrated this for the Co-Si system to monitor the maximum wafer temperature in Physical Vapor Deposition (PVD) systems [4]. The Co-Si system is an example for deducing maximum temperature in the range of approximately 400-550° C [4]. The reactions of other metals like Pd and Pt with Si are diffusion limited. The amount of silicide formed depends then on both applied temperature and time [5]. These metals can be used to deduce the thermal history of a wafer.

To illustrate the operating principle of our temperature monitoring system we will focus on the Pd-Si system. Pd and Si form Pd₂Si at elevated temperatures. This already occurs at relatively low temperatures well below 200° C [6-8]. We validated this reaction via in situ four point probe resistance measurements in a vacuum oven. The resistance of a Pd thin film on Si and the formed Pd₂Si was monitored during isothermal annealing. Subsequently, the resulting Pd₂Si thickness was derived using a simple 3-layer (Pd – Pd₂Si – Si) resistive model. Since the thickness growth of Pd₂Si is diffusion limited the square of the thickness versus time should render a linear plot. This is illustrated in Figure 1A for measurements of a 156nm Pd film on moderately doped ($N_A \sim 10^{15} \text{ cm}^{-3}$) Si for various temperatures. From this data the diffusivity D can be derived and it can be plotted in an Arrhenius curve ($\ln(D)$ versus the reciprocal temperature) as shown in Figure 1B.

Figure 1. The square of Pd₂Si thickness (d^2) vs time for three different temperatures (A) and the resulting Arrhenius plot (B). The solid line shows the best linear fit.

From Figure 1B the activation energy E_A can be derived [8] and it was found to be $1.0 \pm 0.1 \text{ eV}$, in close agreement with literature [7].

Next, this well-defined behavior of the Pd-Si system was exploited in the design of test structures. The use of SOI wafers and the fact that the silicide formation is isotropic enables us to design structures that make optimum use of the resulting silicide formation profile. An example to illustrate this effect is given in Figure 2.

Figure 2. Schematic cross-section of an SOI structure with different metal patterns before (A-1 and A-2) and after (B-1 and B-2) partial silicide formation.

In Figure 2A-1 a 50 nm Pd metal line is shown with a given width x , whereas in Figure 2A-2 this line is divided in two equal parts of width $x/2$. Before silicide formation the resistance of both line structures will be the same. During silicide formation a Pd₂Si profile will develop in vertical and lateral direction. As soon as the SOI thickness is used the reaction will continue in lateral direction only. In this case the structure in Figure 2B-1 renders two propelling silicide fronts whereas the structure in Figure 2B-2 renders four propelling silicide fronts. Starting from an initially equal resistance, a difference in the measured resistance for the two structures will occur for the same thermal budget. So, as soon as the SOI has been consumed a different diffusion path will develop and other kinetics will be measured for the two structures whereas the thermal budget seen by the two is the same. In this manner additional information and hence a more accurate determination on the thermal budget (time and temperature) is obtained.

In order to verify the above we designed various test structures. Around 50 dies of 8.7mm x 8.7 mm are patterned on a 4" test wafer. Each die contains a total of 600 test structures divided into repeating blocks of 24 - 30 individual test structures, enabling statistically verifiable measurements. Test lay-outs are divided into "lines" and "gaps" types. Examples of processed wafers with both types are depicted in Figure 3.

Figure 3. Examples of “line” structures (A) and “gap” (B) structures.

In Figure 3A some line structures are depicted. Single, double or triple line structures are both patterned horizontally and vertically with thicknesses from 2 to 60 μm . In Figure 3B an example of gap structures in the form of circular and finger structures are depicted. The gap spacing between the two sides ranges from 1 to 5 μm . When the two propelling silicide fronts during heating will touch a drastical resistance drop is expected. For increasing gap spacing the total temperature budget (temperature x time) will be longer before the two fronts will touch and hence a quick and rough estimate is obtained to check in what range the thermal budget was applied.

At present wafers have been patterned with Pd structures and measurements are in progress. Next, other metals will be tested. Since the formation of each metal silicide takes place at a given temperature window in theory one can design temperature monitors covering a large temperature window (e.g. 100° - 450° C) by selecting the proper metals.

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