A 0.45pJ/conv-step 1.2Gs/s 6b full-Nyquist non-calibrated flash ADC in 45nm CMOS and its scaling behavior

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Abstract—. **A 6-bit 1.2 Gs/s non-calibrated flash ADC in a standard 45nm CMOS process, that achieves 0.45pJ/conv-step at full Nyquist bandwidth, is presented. Power efficient operation is achieved by a full optimization of amplifier blocks, and by innovations in the comparator and encoding stage. The performance of a non-calibrated flash ADC is directly related to device properties; a scaling analysis of our ADC in and across CMOS technologies gives insight into the excellent usability of *45nm* technology for AD converter design.**

I. INTRODUCTION

Power-efficient WPAN applications push the demand for high-speed low-power wideband flash ADCs. Low resolution ADCs with off-chip calibration show efficiencies better than 0.2pJ/conv-step at sampling-rates above 1Gs/s [1]. However, the energy consumed to perform and sustain this calibration is commonly not accounted for. The non-calibrated flash ADC in standard 45nm CMOS technology reported here demonstrates an energy efficiency comparable to that of a recent on-chip calibrated flash ADC in 65nm CMOS [2]. Section II gives an overview of the architecture of the reported system. Section III links the efficiency of the preamplifier to transistor properties and comments on the efficiency improvement obtained. Section IV gives measurements results.

II. ARCHITECTURE

The architecture of the ADC, see fig. 1, is based on [3]. A resistor ladder implements the reference stage that generates 9 reference voltages. The 1st preamplifier stage amplifies the difference of the differential references and input signal. Two
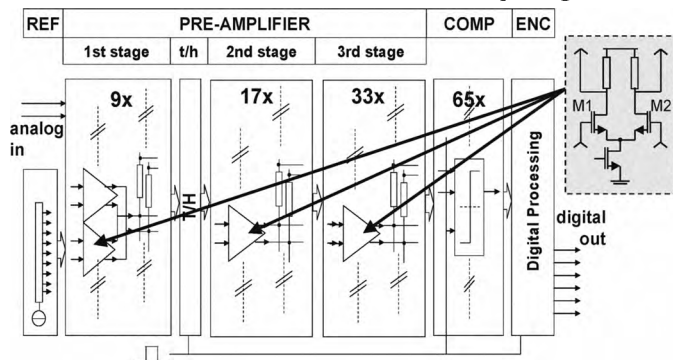

Figure 1. System view, not shown are bias circuit and clock converter. Inset: the building block amplifier.

2-input amplifiers, with there outputs combined are used to form 4-input differential amplifiers. Combining passive output-averaging and interpolation, 17 differential outputs are obtained from the 1st stage. These outputs are sampled with a distributed T/H stage.

The 2nd and 3rd preamplifier stage with passive averaging and interpolation increases the T/H outputs from 17 to 33 and 65 differential outputs respectively. These outputs are converted to 65 bits using 65 comparators. The center 63 bits are encoded into a 6-bit binary word with bubble correction and using an intermediate gray-code.

A. Preamplifier

The preamplifier has the combined function of an amplifier, track-and-hold and interpolator. The difference between the signal and reference is amplified. The track-and-hold function is implemented as a distributed T/H stage using minimum gatelength PMOS switches, dimensioned for sufficient bandwidth while keeping channel charge injection, clock and signal feed-through low. The T/H stage is preceded by the first amplifier- and interpolation-stage. This reduces the relevant voltage-swing across the switch and enables an increased CM-voltage and thus an increased overdrive voltage of the switch, which is beneficial for speed and linearity.

Without interpolation, the input-signal would have to be compared with 63 references. To keep the variations in input referred offset of each comparator small, significant area would have to be spent to compensate for mismatch. The most critical devices to be scaled are the input devices, which are the main contributors to the input capacitance of the system.

In the presented ADC, interpolation and averaging in 3 steps is used to reduce this input capacitance with a factor 19 to a relative low 200fF. This requires a voltage gain of 9dB per stage, which can be obtained with reasonable linearity within the available voltage headroom. By decreasing the width of the transistors in the second, third and comparator stage with respectively a factor 2, 4 and 8 compared to stage one, the total input capacitance per stage is approximately equal.

With the presented interpolation and averaging scheme, the preamplifier becomes the dominating factor determining the ADC bandwidth and power consumption. A full analysis

of scaling properties of the amplifier and the complete ADC in and over technology is presented in section III.

B. Comparators

The comparators are based on the sense amplifier presented in [4], see fig. 2, and replace the static latched comparators used in the [3]. This circuit consists of two integrator stages. A clock signal switches the comparator between the reset and regeneration phase. In the reset phase, as v_{CLK} is low, the intermediate nodes (v_{INT1} and v_{INT2}) are pulled to V_{DD} while the output nodes are pulled to ground. In the regeneration phase, the first stage pulls the common mode voltage at the intermediate nodes from V_{DD} to ground. An imbalance at the input results in unequal discharging currents. The resulting differential mode voltage at the intermediate nodes is amplified to the output nodes by the intermediate transistors in combination with the cross-coupled invertors. The intermediate transistors will pull the common mode voltage at the output nodes from ground to V_{DD}. While charging, the positive feedback of the inverters starts to dominate over the intermediate gain and one output node is charged further to V_{DD} while the other node is discharged to ground. This should happen before the input transistors of the first stage are forced into triode. The input transistors of the first stage are biased close to weak inversion for maximum current efficiency g_m/I_D.

The dynamic nature of this circuit yields little memory effect, high speed operation, and low power consumption: only 1mW at 1.2Gs/s for 65 comparators.

C. Encoding

The center 63 bits are encoded into a 6-bit binary word in 3 pipelined steps. After each step the intermediate digital code is clocked into flip-flops. For the first step a bubble correction is implemented which can correct single bubbles. The next step incorporates robustness against meta-stability errors of the comparators exploiting a segmented 15-bit balanced gray-code. This intermediate coding step minimizes the number of bit-transitions and homogeneously distributes transitions from LSB to MSB. In the final step the 15-bit intermediate gray code is decoded into the final 6-bit binary output code. This approach leads to efficient encoding with low power consumption of 3.2mW at 1.2Gs/s.

III. SCALING ANALYSIS

In this section, the scaling properties of non-calibrated 6-bit flash ADCs over 5 CMOS technologies from 180nm to 45nm are analyzed. In the analysis these technologies are referred
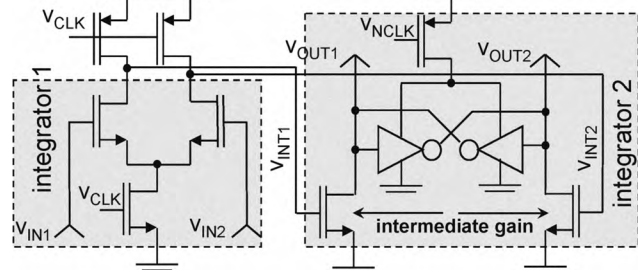

Figure 2. Dynamic comparator; the 2nd integrator provides intermediate voltage gain and positive feedback.

to as C180 to C045. In the analysis the architecture described in section II is assumed; for this architecture we have implementations in 3 CMOS technologies to support the theoretical finding. The implementations in C130 and C180 technologies were published in [8] respectively [3]. This paper presents a very efficient implementation in C045, see sections II and IV.

In our system the power consumption and bandwidth of the ADC are determined by the preamplifiers' performance. The main building block of the preamplifier is the resistor-loaded amplifier shown in the inset of fig. 1. The power consumption, bandwidth and accuracy of this amplifier are in turn determined by bias settings, aspect ratios of transistors and by various technology parameters. Clearly then the impact of porting our ADC system across technologies is ultimately dominated by transistor biasing, dimensioning and by various technology parameters.

The requirements in table I are a trade-off between linearity, gain, accuracy, input range and voltage headroom, typical for the amplifier implementation to be used in a 6-bit flash ADC. With these requirements, the only remaining degrees of freedom in the amplifier design are in the transistor gatelength (L) and supply voltage (V_{DD}). In the trend analyses in this section, the V_{DD} is set to 1.8V for C180 and 1.2V for C130-C045 respectively, leaving only the transistor length L as degree of freedom per technology. The amplifier is loaded by an equal amplifier to resemble the capacitive load described in section II. Assuming first order transistor models (e.g. square law behaviour) the relations in table 1 would result in power consumption (P) and bandwidth (BW) that both are inversely proportional to the square of the transistor length: $P \propto L^{-2}$ and $BW \propto L^{-2}$.

Differences in $P(L)$ and $BW(L)$ between various technologies can then be attributed to transistor properties. It appears that mainly differences in mobility reduction, matching properties and parasitic capacitances are dominant in differences between $P(L)$ and $BW(L)$ curves for various technologies.

To clearly show these differences, fig. 3a and fig. 3b give respectively a simulated (using MM11/PSP device models [5,6]) $P(L) \cdot L^2$ curve and a simulated $BW(L) \cdot L^2$ curve for 5 CMOS technologies. For readability reasons, these curves are normalized with respect to the value for a C180 technology when using $L=20\mu m$, yielding

TABLE I.   AMPLIFIER/SYSTEM REQUIREMENTS

Gain	$A_v = 9$ [dB]	As described in previous paragraph.
Accuracy	$3\sigma_{V_{OFFSET}} < 0.5\,\text{LSB}$	Rule of thumb to keep a monotonous ADC.
Input range	Amplifier: $V_{in} = V_{DD}/16$ [V]	Three neighbouring reference tap zero-crossings fall within the range. This enables averaging and interpolation.
	System: $0.5V_{DD}$	
Headroom	$V_{CM} = 0.75V_{DD}$ [V]	Voltage headroom needed to keep the amplifier current source in saturation.
	$\Rightarrow$	Clipping at the outer ends of the output voltage window causes distortion. *V_{WINDOW}=output voltage range=0.5V_{DD}
Linearity	$V_{out} = 0.35V_{WINDOW}^*$ [V]	

$$\underline{P} = \frac{P(technology,L)}{P(C180,L=20\mu)} \frac{L^2}{(20\mu)^2} \qquad (1)$$

$$\underline{BW} = \frac{BW(technology,L)}{BW(C180,L=20\mu)} \frac{L^2}{(20\mu)^2} \qquad (2)$$

Note that these curves would be completely flat for first order MOS transistor behaviour. Within technologies, $\underline{P}$ drops a factor 4 towards smallest L, mainly caused by mobility reduction [7]. Between technologies $\underline{P}$-reduction is mainly caused by A_{VT} reduction. The impact of mobility reduction towards short L is also apparent in $\underline{BW}$. The $\underline{BW}$ towards short L is further reduced by parasitic transistor capacitances [7].

The $P(technology,L)$ and $BW(technology,L)$ can be used to estimate the energy efficiency FoM for the complete ADC. The conventional definition of the FoM is

$$FoM = \frac{P_{ADC}}{2^{ENOB@DC} \cdot f_{sample}}$$

and its expansion for the presented analysis is

$$FoM(technology,L) = \frac{\rho \cdot P(technology,L) + P_{other}}{2^{ENOB@DC} \cdot 2 \cdot \beta \cdot BW(technology,L)} \qquad (3)$$

In (3) the factor ρ is the sum of the relative contribution to the power consumption by the amplifiers in the first, second and third preamplifier stage. For the analyzed system, see section II, $\rho=2\cdot9+17/2+33/4=34.75$ and will be kept invariant over all technologies. P_{ADC} is the power consumption of the total ADC, and P_{other} is the power consumption in the ADC outside the amplifiers. For our analyses and chip realisations $ENOB \cong 5.5$. In a single stage flash ADC the sample rate usually is twice the bandwidth of the amplifiers. For flash ADCs with averaging and interpolation the sample rate is lower, which is accounted for by the factor β.
This $FoM(technology,L)$ in (3) is plotted in fig. 4 for $\beta=1$. In fig. 4, each curve corresponds to a certain technology, while the curves are created by sweeping the amplifier transistors' length. The curves show that porting to newer CMOS
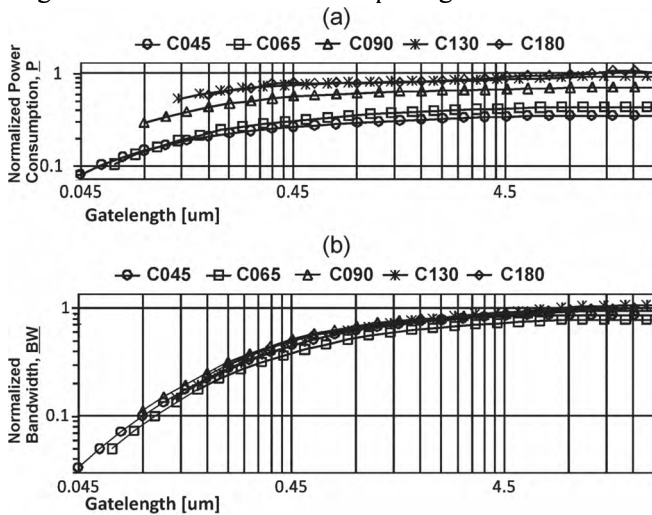
generations improves the FoM (a factor 3.5 from C180 to C045) and improves the maximum attainable sample rate. This maximum attainable sample rate is reached at minimum transistor length, which obviously can be smaller in newer CMOS generations.

In the ADC in C045 technology presented in this paper, with interpolation and averaging, the factor $\beta=\frac{1}{8}$ while non-minimum length transistors are used in our design. The arrow in fig. 4 starts at the point corresponding to $FoM(C045,L_{used})$ for $\beta=1$ and ends at the FoM for $\beta=\frac{1}{8}$. The difference between the end of the arrow and the actual (measured and simulated) FoM is due to power spent in other parts of the ADC, the term P_{other} in (3). The same reasoning can be followed for the C130 and C180 ADC using the dotted lines in fig. 4. Due to innovations in the comparator stage and in the digital encoder, see section II, for our realisation P_{other} is very small. The measured FoM of our ADC in C045 technology corresponds to the crown symbol marked C045 in fig. 4.

For benchmarking reasons, data points with published FoM and sample rate are included in fig. 4. The crown marked C045 is the system presented here including full optimization and innovations in digital and comparators. The other 2 crowns are the same system, without these optimization and innovations, in C130 and C180 [8,3]. Crosses (X) represent non-calibrated flash ADCs and plusses (+) calibrated flash ADCs in literature [1,2,9].

The ADC presented here is designed for digitization of 528MHz UWB signals and distinguishes itself from other ADCs in fig. 4 by obtaining good efficiency and a low input capacitance while not using any type of calibration. Its performance is comparable to the state-of-the-art on-chip calibrated ADC in 65nm CMOS in [2]. This demonstrates that the energy efficiency advantage of digital calibration is on par with migration to the next technology node.
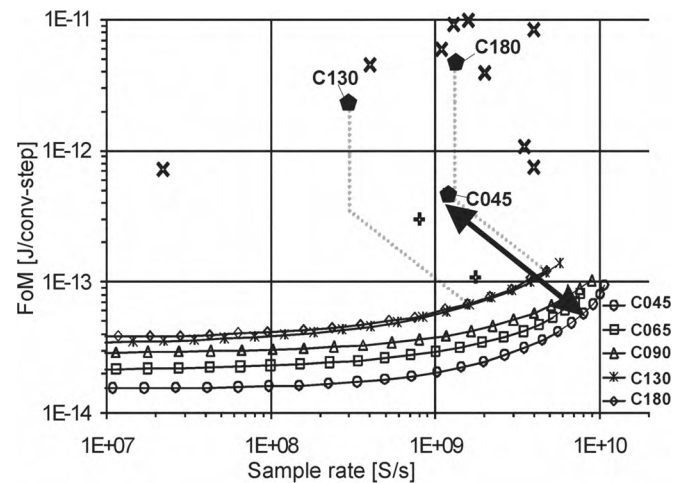
(a)

(b)

Figure 3.   a) Normalized power consumption and b) normalized bandwidth as a function of gatelength L for 5 technologies

Figure 4.   Flash ADC FoM versus sample rate. Curves are FoM according to (3) for β=1, the arrow is the shift when going to β=⅛. Crowns are the presented ADC and the C130 and C180 implementations [8,3]. Other data points are non-calibrated (X) and calibrated (+)flash ADC from [1,2,9].

IV. Measurements

The ADC is fabricated in a standard 45nm CMOS process and occupies 0.1mm^2 active area, see fig. 5 for a die photograph. INL and DNL<0.6LSB for the full input range, see fig. 6. Nonlinearity associated with averaging and interpolation towards the outer codes is effectively eliminated using a Moebius band construction [10].

Fig. 7 shows distortion, HD2 and HD3, SNR and SNDR at the output for various sample rates. The input signal frequency is at Nyquist for each sample rate. The SNDR stays flat until 1.2 Gs/s. Thereafter, it drops due to bandwidth limitations of the amplifiers.

Fig. 8 shows distortion, HD2 and HD3, SNR and SNDR at the output, sampled at 1.2Gs/s while sweeping the input frequency from 10MHz to 700MHz. The ERBW is above 600MHz and the ENOB at DC is 5.7. Power consumption of the ADC core, bias-circuit, and clock-converter excluding output buffers is 28.5mW (25.3mW analog and 3.2mW digital), with V_{DD} at 1.2V. This results in an energy efficiency of 0.45pJ/conv-step.

V. Conclusions

A non-calibrated 6-bit flash ADC with an energy efficiency of 0.45pJ/conv.step at a sample rate of 1.2GHz is presented. This low FoM was achieved by full optimization of the amplifiers, by innovations in the digital encoding and in the comparators, and by taking full advantage of the capabilities of 45nm CMOS technology. The scaling analysis combined with simulated and measured performance shows that this achieved FoM is very close to the minimum FoM possible for 45nm CMOS, at 1.2Gs/s for our interpolation/averaging architecture. Furthermore, the scaling analysis and benchmarking suggests that energy efficiency advantage of digital calibration is on par with migration to the next technology node.

Acknowledgment

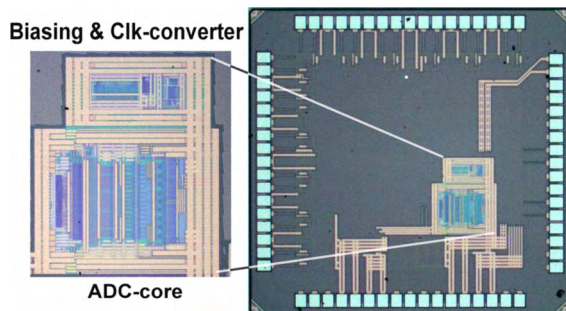The authors would like to thank Hans van de Vel for his contribution to this work.
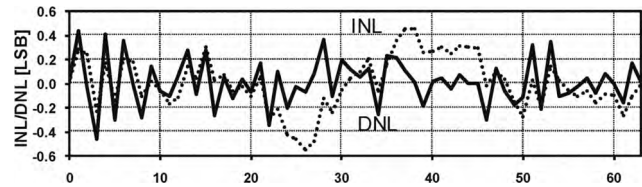

Figure 5. Die photograph.
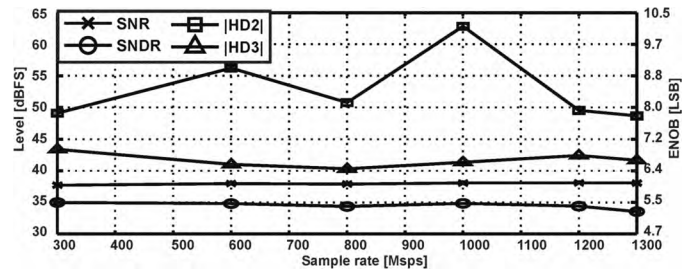

Figure 6. DNL and INL vs. output-value.

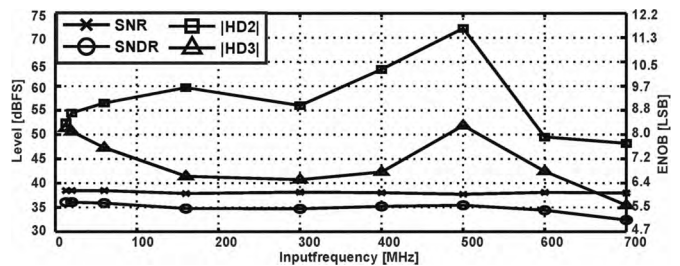Figure 7. 2nd and 3rd Harmonic, SNR and SNDR vs. f$_{sample}$, f$_{in}$=f$_{Nyquist}$.

Figure 8. 2nd and 3rd Harmonic, SNR and SNDR vs. f$_{in}$, f$_{sample}$=1.2Gs/s.

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