A Time-Interleaved Track & Hold in 0.13µm CMOS sub-sampling a 4 GHz Signal with 43dB SNDR

Simon M. Louwsma, Ed J.M. van Tuijl, Maarten Vertregt* and Bram Nauta

IC Design Group, CTIT Research Institute, University of Twente
PO Box 217, 7500 AE Enschede, The Netherlands
e-mail: s.m.louwsma@alumnus.utwente.nl
*with NXP Semiconductors, Eindhoven, The Netherlands

***Abstract*—A 16-channel time-interleaved Track and Hold is presented. Three techniques are introduced enabling a high bandwidth and linearity and good timing alignment. Integrated ADCs are used to evaluate the performance of the T/H. Single channel performance is 43 dB SNDR at an input frequency of 4 GHz. Multi-channel performance is 48 dB SNDR at 1.35 GS/s with an ERBW of 1 GHz. The power consumption of the T/H including clock-driver and buffers is 74 mW.**

I. Introduction

To sample broadband signals of e.g. satellite receivers, Track and Holds (T/Hs) are needed with a bandwidth of about 1 GHz and linearity above 50 dB. For software defined radios an even larger bandwidth is desired. To be able to embed the T/H together with an ADC in a digital IC, the power consumption of the T/H and ADC should be limited to a few hundred milliwatts. Time-interleaving is a good way of combining power efficiency with high speed. However, a time-interleaved T/H needs a signal bandwidth per channel far beyond the sample-rate of an individual channel. Moreover, it requires matching between its channels. In this paper a time-interleaved T/H is described for use in a time-interleaved ADC as shown in Fig. 1. The T/H is a successor of the one presented in [3] and has improved bandwidth, linearity and channel matching. Innovations presented here are: an improved buffer design, a bandwidth enhancement technique and a low skew-variation clock-driver. To evaluate the T/H, integrated ADCs are used which are described here only briefly, while a detailed description is given in [5].

II. Time-interleaved Track and Hold

The time-interleaved T/H consists of 16 channels, which is based on the analysis that a sample-rate of about 100 MS/s is viable for sub-ADCs with a good power-efficiency and about 50 dB SNDR. The basic schematic of one channel is shown in Fig. 2. The circuit is (pseudo) differential, and only a single-ended version is shown. The sample switch is bootstrapped by connecting a capacitor charged to V_{dd} between the source and gate of the sample switch.

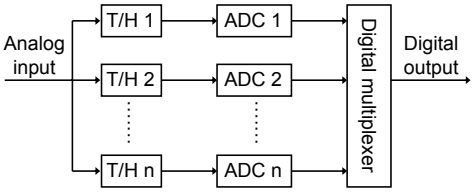

Fig. 1: time-interleaved ADC architecture

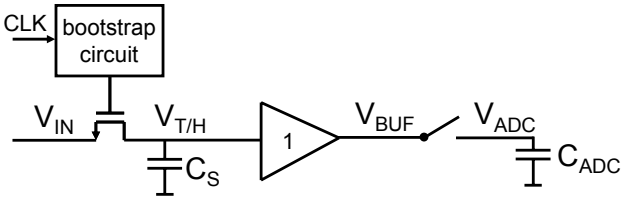

Fig. 2: Overview of 1 of the 16 T/H channels

Bootstrapping makes the on-resistance of the sample-switch more constant over varying V_{IN} and avoids signal dependent charge injection, resulting in better linearity. Also, the turn-off time is made less dependent on the momentary input voltage.

A. Buffer

The schematic of the buffer is shown in Fig. 3. It is in fact a Pmost source-follower, with an additional Nmost source-follower aiming to keep the drain-source voltage of the Pmost constant. In modern sub-micron processes the output resistance of MOSFETs has become very small and is non-linear, the first resulting in less gain, the latter resulting in distortion. By adding the second source-follower, the effective output resistance is increased and gain and linearity are improved. Compared to a conventional source-follower, the input capacitance is not increased like in a cascode source follower [6], but on the contrary it is decreased: The gate-drain (overlap) capacitance is effectively lowered since the drain terminal has roughly the same phase and amplitude as the gate terminal and the small-signal current through the capacitor is mitigated. A low and linear input capacitance is important to avoid distortion of high-frequency input signals.

B. High-bandwidth sampling technique

For a single Nyquist T/H the bandwidth requirement of the buffer for settling is: $BW > 1/(2\pi \cdot 10 \cdot f_S)$ for 5τ of settling in half the sample period. An input buffer with this bandwidth closely tracks an input signal at the Nyquist frequency. For sub-sampling and time-interleaved T/Hs however, the

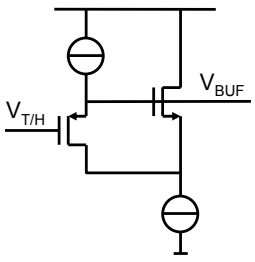

Fig. 3: High-linearity input buffer

bandwidth requirement of the input buffer for settling is relaxed by the sub-sampling or interleaving factor: the time needed for settling is long compared to the maximum input signal period. The bandwidth requirement is now $BW_{INT} > 1/(2\pi \cdot 10/ifac \cdot f_S)$, with ifac the interleaving (or sub-sampling) factor. With an interleaving factor of 16 and minimal BW (to save power) for settling, the buffer output no longer tracks input signals at the Nyquist frequency, but a large attenuation and phase-shift is present. Now the problem as shown in Fig. 4 arises: During tracking, the buffer output V_{BUF} cannot follow the input signal $V_{T/H}$ and at the sample moment (t_{SAMPLE}) the output signal is not yet fully settled. After the sample moment, output V_{BUF} will slowly settle to its final value. During this settling charge-redistribution between the non-linear parasitic capacitance between the input and output of the buffer and the sample capacitor causes distortion in the voltage on the sample capacitor $V_{T/H}$. The buffer output V_{BUF} is therefore also distorted.

To avoid distortion the buffer bandwidth can be increased, but this would increase the power consumption significantly. In this paper we introduce a switch between the buffer output and the ADC following the T/H as shown in Fig. 2. In track-mode this switch is open and the load capacitance of the buffer is now small. Hence the buffer bandwidth is increased and output V_{BUF} can now follow the input $V_{T/H}$ as shown in Fig. 5. In this case no distortion due to charge redistribution occurs. When the ADC is connected at $t=t_{SWITCH}$, the buffer output will first make a step to the previous sampled value which still was present on the ADC input capacitance, after which the buffer will charge the ADC load to the newly sampled value, see Fig 5. Charge redistribution also leads to a signal dependent step in $V_{T/H}$, however due to settling of V_{BUF}, $V_{T/H}$ returns to its initial, undistorted value. The process of connecting the ADC does therefore not cause any additional distortion.

Time-interleaving relaxes the requirements on the ADC. Just by adding the switch, the advantages now also hold for the T/H buffers. An additional advantage is the reduced input capacitance of the buffer.

III. Channel Matching

In a time-interleaved ADC differences between channels should be sufficiently small: offsets between channels cause tones at multiples of $f_S/16$, (ifac=16) while differences in gain and timing result in tones at multiples of $f_S/16 \pm f_{IN}$ [7].

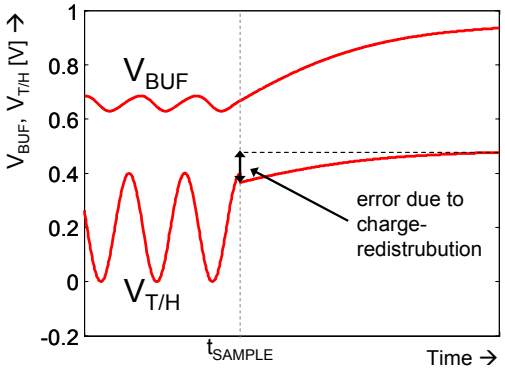

Fig. 4: Sampling a high speed input signal with limited buffer bandwidth

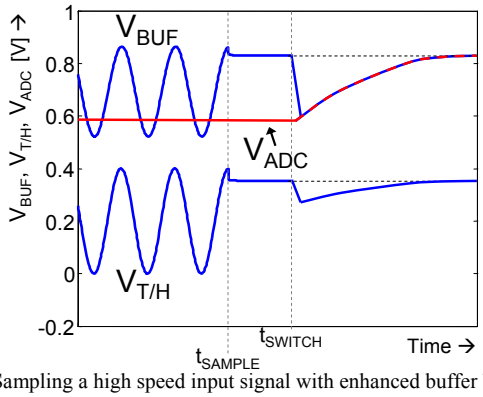

Fig. 5: Sampling a high speed input signal with enhanced buffer bandwidth

Reducing channel offsets by straightforward device sizing to reach the required accuracy conflicts with speed and power constraints [3], therefore channel offsets are made adjustable in this design. Channel gain is adjustable as well to correct for errors stemming from mismatch in the input buffer and the sample process. Both calibrations are controlled digitally by modifying analog bias settings in the input buffer via a 6/7 bits DAC. In this test-chip the digital bias settings are controlled manually. In an actual implementation, channel gain and offset can relatively easily be adjusted by a start-up calibration requiring only DC test-signals.

Calibration of timing mismatch however, requires high-frequency test-signals and complicated calibration algorithms. By careful design we try to minimize timing mismatch, avoiding the need for this calibration.

A. Timing matching

In [2] a technique to prevent timing errors in a time-interleaved T/H is presented. It uses a front-end sampling switch which is closed only half the period of the master clock. A disadvantage of this method is the decrease in bandwidth. Another technique is the use of the master clock to synchronize the different sampling instants as in [4], which achieves good timing alignment and it does not have the disadvantages of a front-end sample switch. To minimize timing offsets the following techniques are used:

- A master clock, such that the actual sample moment only depends on one common clock.
- Matched lines to distribute clock and input signals to the channels, see Fig. 9.
- Minimized skew-mismatch of the conversion between the common master-clock and the sample-switch using a new circuit-technique.

In applications where supply-noise may degrade performance, current mode logic (CML) is commonly used because it generates little supply noise. CML uses differential signaling, with signal swings of about half the supply voltage in our design. To convert the CML master clock into a full-swing signal suitable for the sample-switch, a conversion circuit is needed. With a conventional solution on a previous chip we measured a timing misalignment of 6 ps RMS, which is too high for the target specification. Therefore, a new circuit topology is used as shown in Fig. 6. To minimize skew variation and jitter, the path from the common master-clock to the different sample switches is made as short as possible.

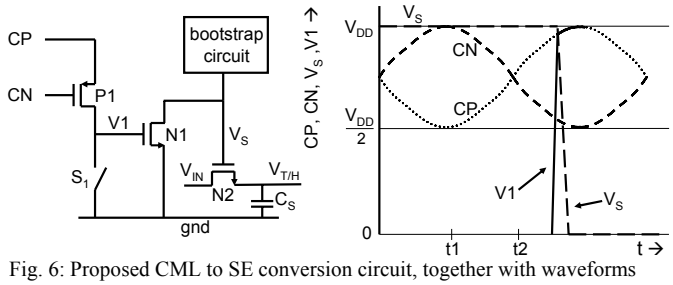

Fig. 6: Proposed CML to SE conversion circuit, together with waveforms

The operation is as follows: The T/H is put in track-mode by the bootstrap circuit, which makes the V_{GS} of N2 equal to about V_{DD}. At the end of the track-mode (t=t2), node V_S is left floating by the bootstrap circuit and for further bootstrapping we rely on parasitic capacitances. Now, to switch into hold-mode, node V_S has to be discharged to ground rapidly: transistors P1 and N1 take care of this. Assume switch S1 is closed and $V_{CP} < V_{CN}$, so node V1 is at ground potential and P1 is non-conducting. In this state switch S1 is opened, without influencing the potential of V1. When the differential voltage of the differential master clock (CP − CN) becomes larger than the threshold voltage V_T of P1, P1 will start conducting and node V1 will be charged to V_{CP} as shown in Fig. 6. This will make N1 conducting, discharging node V_S rapidly and putting the circuit into hold-mode. This is the only time-critical operation in the T/H.

In a time-interleaved T/H, the different channels should sample one after the other, with a delay of one clock-period. At the rising edge of the clock, only one of the channels should switch into hold-mode. The circuit can be extended with a transmission-gate (TM-gate) and a pull-up switch as shown in Fig. 7. When the T/H should not switch into hold-mode, the TM-gate is made non-conducting and the gate-node of P1 is pulled to V_{DD}. In this case P1 never starts conducting and node V1 stays at ground. When the circuit should switch into hold-mode, the TM-gate is made conducting when $V_{CP} < V_{CN}$ (e.g. t=t1) and the pull-up switch is made inactive. In this case the behavior is the same as without the TM-gate and the T/H switches into hold-mode when $V_{CP} - V_{CN} > V_T$.
Advantages of this solution:

- Only the mismatch of P1 and N1 influences the skew, so the complete "spread budget" can be spent in these transistors.
- Only the difference between the differential clocks CP and CN determines the sample moment; the common-mode signal is rejected.
- Both differential clocks are used and the effective slope is doubled, which halves the influence of the threshold voltage variations of P1.
- By keeping the path from input clock to sample switch short, little jitter is generated in the circuit.
- By cascading P1 and N1, which are otherwise not connected (no current sources), the gain is maximized. This results in a very steep slope at V_S and makes the sample process more ideal.

The expected timing-misalignment is 0.45 ps RMS. This value is derived from multiplying the (simulated) switching-slopes by the $\sigma(\Delta V_T)$ of the respective transistors.

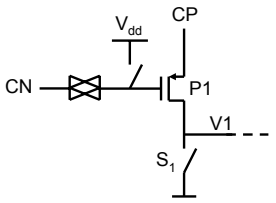

Fig. 7: Circuit enabling the use on a multi-phase clock

IV. Sub-ADC Architecture

The 16 ADCs following the 16 T/H amplifiers are built with Successive Approximation ADCs [5]. For each channel, two SA-ADCs are combined in a pipeline configuration. An overview of the sub-ADC architecture is shown in Fig. 8. It consists of an interleaved T/H section, a first SA-ADC, a DAC, an inter-stage amplifier and a second SA-ADC. Both SA-ADCs are 6 bit and with the amplifier gain of 16 the resolution becomes 10 bit. Pipelining and inter-stage gain relax the requirements of the SA-ADCs: more time is available per conversion and the required accuracy is reduced. The inter-stage amplifier uses a switched-capacitor opamp configuration with offset cancellation of the two-stage opamp. The DAC is implemented as a resistor-ladder with switches. All signaling is pseudo-differential.

The 16 times interleaved T/H and 16 connected ADCs are fabricated in 0.13 µm CMOS and a photograph of the chip is shown in Fig. 9, with a zoom-in on the interleaved T/H on the right-hand side, which has an area of 0.14 mm^2. The total active area of T/H and ADCs is 1.6 mm^2.

V. Measurement Results

First, the measurement result of a single channel is discussed. During this measurement all channels are active, however only the data from one channel is analyzed. The T/H is directly connected to a 50 Ω signal generator. In Fig. 10 the measurement result is shown at a total sample-rate of 1350 MS/s and thus 1350/16 ≈ 84.4 MS/s for a single channel. At low input frequencies the SNDR is 50 dB, simulations indicate that this is limited by ADC noise. The THD for low frequencies is -60 dB. For higher input frequencies than the Nyquist frequency per channel (>42 MHz), the ADCs are

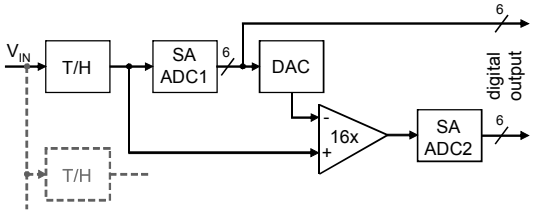

Fig. 8: Overview of the sub-ADC architecture (1/16 of total ADC)

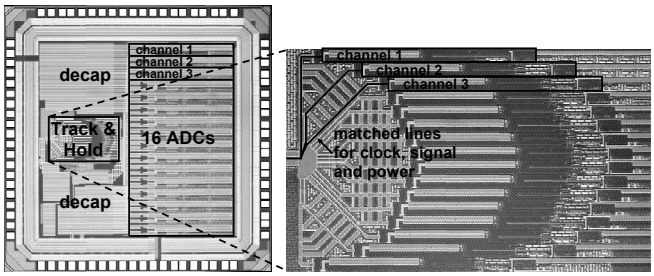

Fig. 9: Photograph of the time-interleaved ADC and zoom-in on T/H

sub-sampling and performance degradation is purely due to the T/H. The THD improvement at 8 GHz is due to a decrease in signal amplitude caused by losses in the test-bench signal path. THD at 4 GHz is -52 dB and THD at 8 GHz is -44 dB, which shows the excellent bandwidth and linearity of the T/H due to the use of the new circuit techniques applied in the T/H and the buffer. At 4 GHz input frequency the SNDR is 43 dB and at 8 GHZ the SNDR is 36 dB.

A worst-case approximation of the RMS jitter is given by: $\sigma(\Delta t) = 10^{-SNR/20}/2\pi f_{IN}$. Using this, the total jitter stemming from clock and signal generators and the circuit is only 0.2 ps RMS, which is better than any value for a T/H or ADC in CMOS found in literature. At high signal frequencies only jitter limits the SNDR.

The 16-channel interleaved performance at 1350 MS/s is shown in Fig. 11. The SNDR is 48 dB at low input frequencies and the ERBW is 1 GHz. Compared to the single channel case, the performance is only slightly degraded, showing that channel gain and offset are adjusted satisfactory and the step-size of the adjustment DACs is sufficiently small.

It is possible to extract the timing-misalignment from the measured data by determining the phase of the input signal for each channel by means of an FFT. This way jitter is averaged out and only the timing offsets remain. The result of this operation for two measurements is shown in Fig. 12. The extracted RMS timing misalignment is 0.6 ps RMS, which is close to the expected value of 0.45 ps RMS and which shows the low skew-variation technique is useful. Due to the dominance of timing-misalignment, total timing error across all channels including jitter is also 0.6 ps RMS. For ADCs with a large bandwidth (>1 GHz), this value is slightly better than the best found in literature [1] where elaborate timing calibration is used. At 2 GHz the SNDR is 41 dB and at 4 GHz the SNDR is 37 dB, limited by timing-misalignment.

The input capacitance is about 1 pF, resulting in an RC limited analog input bandwidth of 6 GHz. The T/H buffers use a supply of 1.6 V, while the rest of the circuit uses 1.2 V. Power consumption of the T/H including clock-buffer and timing generation is 34 mW, the T/H buffers consume 40 mW and the 16 ADCs consume 100 mW. The FoM of the complete ADC calculated by power/$\{2^{ENOB}\cdot\min(f_s, 2\cdot ERBW)\}$ is 0.6 pJ per conversion-step.

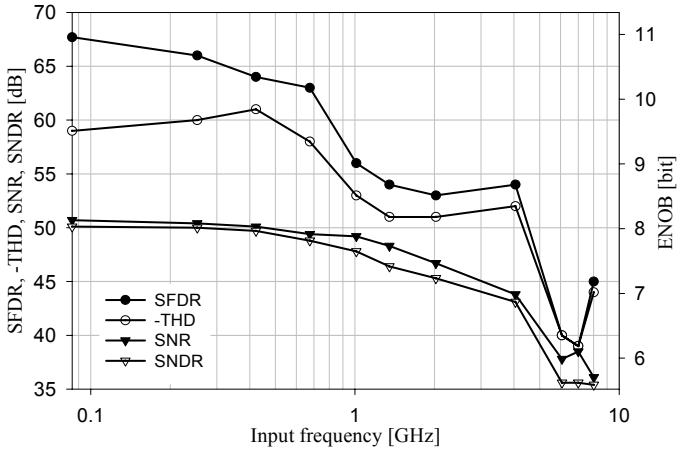

Fig. 10: Measurement result of a single channel

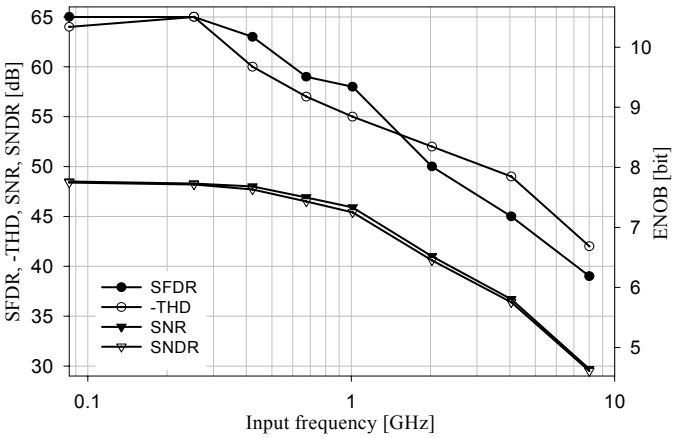

Fig. 11: Measurement result of the time-interleaved ADC at 1.35 GS/s

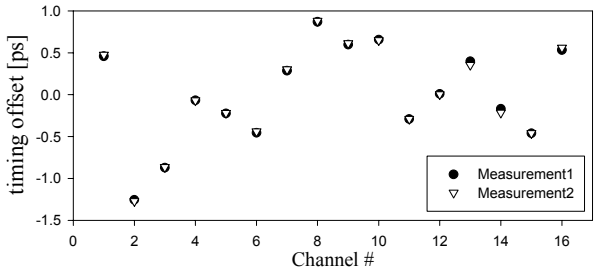

Fig. 12: Extracted timing offset (normalized)

VI. Conclusions

By using a new buffer and removing the load in track-mode, the T/H reaches a high bandwidth and good linearity. For a single channel THD is -52 dB at an input frequency of 4 GHz and SNDR is 43 dB, which is only limited by (best-in-class) jitter of 0.2 ps RMS. With a novel circuit design a good timing alignment of 0.6 ps RMS is achieved, even without timing calibration. The FoM of the complete ADC including T/H is 0.6 pJ per conversion-step. The SNDR is 48 dB for low frequencies, while the ERBW is 1 GHz, showing broadband signal handling capability.

Acknowledgments

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