Methodology for performing RF reliability experiments on a generic test structure

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Abstract— This paper discusses a new technique developed for generating well defined RF large voltage swing signals for on wafer experiments. This technique can be employed for performing a broad range of different RF Reliability experiments on one generic test structure. The frequency dependence of a gate-oxide wear out stress was investigated using this methodology for frequencies of up to 1 GHz.

Index Terms—Reliability, RF, large signal, oxide degradation.

I. INTRODUCTION

The increasing RF capabilities of CMOS have resulted in an ever growing incorporation of CMOS into RF circuits. Although the RF performance of CMOS can be very well characterized, the reliability performance under RF conditions has received very little attention in literature. The main reason for this is that all reliability models are either voltage or field based and voltage signals get strongly distorted at such high frequencies. This makes it very difficult to perform accurate reliability experiments at frequencies above ~10 MHz. Some authors have addressed this problem by designing specific test structures for one single experiment [1, 2]. In this paper we will discuss a new measurement approach that allows us to perform a broad range of different RF reliability experiments on a generic test structure.

II. TEST STRUCTURES

The goal of the work discussed in this paper is to characterize the degradation of MOS devices under RF stress conditions and compare it to degradation under stress conditions with a lower frequency. This can give very valuable insights on how accurate the current DC and AC degradation models are for predicting the lifetime of RF CMOS circuits. A useful comparison can only be made if the stress voltage signals are equivalent. This means that we need to stress the device under AC stress conditions that have equal duty cycles, but different frequencies. If the devices are stressed several orders of magnitude longer than the period of such a signal, the net voltage stress will be equal for all frequencies used.

A key issue in performing such an experiment is to generate a voltage signal that is equivalent over a broad frequency range and has a large voltage swing. For frequencies of up to 10 MHz use can be made of signal generators to generate any desired voltage signal. For higher frequencies however, this becomes very difficult as the effect of reflected voltage waves becomes noticeable. The approach that we propose in this paper is to make use of sinusoidal voltage signals for this purpose. The main advantage of using

Figure 1: Time-domain voltage waveform as it can be obtained on our test structures if the appropriate RF power is delivered. The harmonic content is also shown and the harmonic distortion is clearly negligible.

sinusoidal voltage signals is that these are relatively easy to generate without the need for complex test structures that are specifically designed for every frequency, as will be explained in this paper. Rather than designing such complex test structures we are able to perform RF reliability experiments on a generic test structure. Generic in this sense means that only one test structure needs to be designed for performing all sorts of RF reliability experiments. The test structures that are used in this work consist of transistor structures, laid out in a two-port ground-signal-ground (GSG) configuration.

The test structures consisted of several identical cells with the gates joined to each other and connected to port 1; the drains are connected to port two. The source and substrate are tied and connected to the ground plane. The GSG configuration reduces probe contact impedance, thereby increasing the accuracy of RF characterization techniques as well as that of the RF voltage generation approach that will be discussed in section IV of this paper. Furthermore all test structures are accompanied with OPEN and SHORT de-embedding structures. These can be used for small-signal RF characterization of the devices.

III. SIGNAL INTEGRITY

An important issue to realize is that the input impedance of our test structures is voltage dependent. Since we are interested in generating sinusoidal RF voltage signals with a large amplitude, it is important to verify that the voltage dependent input impedance does not distort the voltage signal too much. This can be verified by solving transmission line equations as was done in [3]. The idea of this technique is to

Figure 2: Schematic drawing of the measurement setup, including all important parts of the Vector Network Analyzer (VNA). This setup can be used to generate a sinusoidal gate voltage signal, superimposed on a DC voltage V_{bias} .

find a discrete-time domain solution for the transmission line equation given by expression (1):

$$\frac{V^+ - V^-}{Z_0} = \frac{V_{DUT}}{Z_{DUT}} \quad (1)$$

In this expression V^+ and V^- represent the incoming and reflected voltage waves at the input of the Device Under Test (DUT) respectively. Expression (1) basically says that the current flowing through the transmission line (the left hand side of equation (1)) equals the current flowing into the DUT (the right-hand side of equation (1)). This equation can be solved by realizing that [4]:

$$V_{DUT} = V^+ + V^- \quad (2)$$

A difficulty in solving expression (1) originates from the fact that Z_{DUT} is not purely resistive, but it also contains an imaginary component, resulting from capacitive and inductive elements. Since these imaginary components are also dependent on V_{DUT} , expression (1) cannot be solved in the frequency domain. This is the reason for solving expression (1) in discrete-time domain. If V_{DUT} is a steady-state sinusoidal voltage signal (the presumption we want to verify), we can model the input impedance simply with a conductance G_{DUT} in parallel with a susceptance B_{DUT} . If we want to generate a large voltage swing sinusoidal signal, the input of the DUT will consist of a bond pad capacitance in parallel with a gate capacitance. Since we are dealing with sinusoidal voltages, any inductive element will only lower the total observed capacitance. The total series inductance will not be so large that the net input impedance will be inductive. We may therefore rewrite expression (1) in time-domain as:

$$\frac{V^+(t) - V^-(t)}{Z_0} = V_{DUT}(t) \left[G_{DUT}(t) + \frac{dC_{DUT}}{dt} \right] + \frac{dV_{DUT}}{dt} C_{DUT}(t) \quad (3)$$

In this expression G_{DUT} and C_{DUT} , the input conductance and capacitance are defined as:

$$G_{DUT} = \text{Re} \left(\frac{1}{Z_{DUT}} \right) \quad (4)$$

$$C_{DUT} = \frac{1}{\omega} \text{Im} \left(\frac{1}{Z_{DUT}} \right)$$

We can measure Z_{DUT} as a function of input voltage V_{DUT}

Figure 3: Signal Flow Graph of the measurement setup of figure 2, including all seven error terms used in the calibration procedure discussed in this paper.

using small signal reflection measurements over a DC voltage sweep. Expression (3) can be solved in discrete time by defining vectors t , V^+ and V_{DUT} , representing the time, incoming voltage wave and voltage signal at DUT level. Every element in V_{DUT} can be found by an optimization routine such that expression (3) is met. For this purpose the time derivatives in this expression are replaced by their discrete time equivalents.

In figure 1 the result of such a calculation is shown. The gate voltage signal that is shown is used for the reliability experiments that will be discussed in section V of this paper. The harmonic content of the voltage signal is also shown and the harmonic distortion is clearly negligible for this example. We have also verified this for the other stress conditions discussed in section V.

IV. VOLTAGE GENERATION

In the previous section we have shown that it is possible to generate perfect sinusoidal voltage signals with a large amplitude for frequencies of up to at least 1 GHz. In this section we will discuss how we can actually control the amplitude of such an RF voltage signal. Since the test structures that we use do not have a perfect 50 Ω input impedance, it is not straightforward to generate voltage signals with a very well defined amplitude.

A. Theory

For low frequency measurements, the amplitude of a generated voltage signal can easily be determined by connecting an oscilloscope in parallel with the DUT. However at frequencies beyond 10 MHz, the wavelength of the voltage signals comes in the same order of magnitude as the length of the measurement cables. If the input impedance of the device is not exactly matched to the characteristic impedance of the measurement cables (typically 50 Ω), both traveling and standing waves will appear on the cables. This means that the amplitude of a voltage signal with a wavelength in the same order of magnitude as the length of the measurement cables, will not be the same at DUT level as it is measured by the oscilloscope. Time-domain voltage signal measurements are therefore extremely difficult to perform for RF signals with an impedance mismatch at the input of the test structure. With the advent of large signal network analyzers (LSNA) it has become possible to determine the time-domain

voltage waveform accurately [5]. As we explained in the previous section however, we are only interested in generating sinusoidal voltage signal. This makes the measurement of all the higher harmonics components and the associated complexity as it is done in such an LSNA obsolete. A Vector Network Analyzer (VNA) is very well capable of measuring the incoming and reflected voltage amplitude and phase relation of a single frequency signal. Below we will discuss how this information can be used to determine the realized voltage amplitude at DUT level and hence use a VNA as an on-wafer signal generator.

First, we show a simplified block diagram of our measurement setup, including all major components of a VNA in figure 2. The VNA is connected in a reflection measurement setup. Note that the setup as it is shown in figure 2 is used to generate sinusoidal gate voltage signals on top of a DC bias voltage V_{bias} . This is the type of stress signal that we have used in our experiments as discussed in section IV. In figure 2 we can recognize an RF power source that generates a power wave a_s . This power wave is superimposed on V_{bias} using a bias T and delivered to the DUT. A part of the power wave will be reflected due to an impedance mismatch at the DUT and a part will be transmitted. Through the use of the two couplers the incoming and reflected power waves are determined. The measured values a_m and b_m will differ from the actual incoming and reflected power waves at DUT level, due to loss terms, directivity errors of the couplers etc. In order to incorporate all these error terms, use can be made of the signal flow graph shown in figure 3. This signal flow graph is based on the commonly used three-term error model commonly used for calibrating VNA's in a reflection measurement setup (see e.g. [6]). The additional terms in the error model of figure 3 originate from the fact that we are not only interested in a relative measurement (sufficient for parameters such as s-parameters, impedance, etc), but also in absolute power levels. In order to make this possible we have split the complete measurement setup into two blocks. Block 1 (consisting of E_{DF} , E_{SF} , E_{m1} and E_{m1}) takes into account all errors that are introduced within the VNA and Block 2 models the loss and mismatch terms of the sma cable and probe needle. We assume this cable & connector network to be reciprocal, expressed in the two identical L_C terms. Now we can determine the amplitude of the sinusoidal voltage signal present at the DUT in terms of measured a_m and b_m . First, the peak-peak voltage at the DUT is given by:

$$V_{DUT,pp} = 2\sqrt{2} \cdot |V_{DUT}| \quad (5)$$

The complex voltage wave V_{DUT} can be found from basic transmission line theory (see e.g. [4]):

$$V_{DUT} = a_{DUT} \cdot (1 + \Gamma_{DUT}) \cdot \sqrt{Z_0} \quad (6)$$

In this expression Z_0 is the characteristic impedance of the measurement setup and Γ_{DUT} is the reflection coefficient of the DUT. So if we know both Γ_{DUT} and a_{DUT} we can find $V_{DUT,pp}$. Using the signal flow graph of figure 3, a_{DUT} can be expressed in terms of a_1 :

$$a_{DUT} = a_1 \cdot \frac{L_C}{1 - M_{CD} \cdot \Gamma_{DUT}} \quad (7)$$

Similarly voltage wave a_1 can be expressed in terms of a_m , a term that is measured by the VNA.

$$a_1 = a_m \cdot \frac{E_{1m}}{1 - E_{SF} \cdot \Gamma_1} \quad (8)$$

In this expression Γ_1 represents the reflection coefficient seen at Port 1. Combining expressions (6), (7), (8) we can find an expression for $|V_{DUT}|$ in terms of a_m and the different error terms and reflection coefficients.

$$|V_{DUT}| = \sqrt{Z_0} \cdot |a_m| \cdot |E_{1m}| \cdot \left| \frac{L_C \cdot (1 + \Gamma_{DUT})}{(1 - E_{SF} \Gamma_1) \cdot (1 - M_{CD} \Gamma_{DUT})} \right| \quad (9)$$

In expression (9) variables Γ_{DUT} and Γ_1 are introduced. They can be derived from the measured quantities a_m and b_m and known error terms. The output of the VNA consists of values for both complex voltage waves a_m and b_m ; from these quantities the apparent measured reflection coefficient can be found:

$$\Gamma_m = \frac{b_m}{a_m} = E_{DF} + \frac{E_{1m} \cdot E_{m1} \cdot \Gamma_1}{1 - E_{SF} \cdot \Gamma_1} \quad (10)$$

Rewriting this expression gives an expression for Γ_1 :

$$\Gamma_1 = \frac{\Gamma_m - E_{DF}}{E_{1m} \cdot E_{m1} + E_{SF} \cdot (\Gamma_m - E_{DF})} \quad (11)$$

Similarly an expression for Γ_{DUT} can be found:

$$\Gamma_{DUT} = \frac{\Gamma_1 - M_{C1}}{L_C^2 + M_{CD} \cdot (\Gamma_1 - M_{C1})} \quad (12)$$

Now with expressions (5), (9), (11) and (12) it is possible to determine $V_{DUT,pp}$ from the two measured voltage waves a_m and b_m and the 7 known error terms of figure 3.

In order to find all error terms a calibration procedure needs to be performed. The 7 error terms can be determined using a 7-step calibration procedure. The first three steps consist of a Short-Open-Load calibration at port 1. Subsequently an absolute power meter measurement is performed at port 1 using an external power meter. Finally the cable & connector network is connected and a Short-Open-Load measurement procedure is performed using a calibration substrate. These calibration measurements are performed for all frequencies used and the entire range of possible RF power values. Assuming ideal calibration standards (a valid assumption in the frequency range discussed in this paper) expressions for E_{1m} , E_{m1} , E_{SF} and E_{DF} can be found from the calibration measurements at port 1:

$$E_{DF} = \Gamma_{L,1} \quad (13)$$

$$E_{SF} = \frac{\Gamma_{O,1} + \Gamma_{S,1} - 2 \cdot \Gamma_{L,1}}{\Gamma_{O,1} - \Gamma_{S,1}} \quad (14)$$

$$E_{1m} \cdot E_{m1} = 2 \cdot \frac{(\Gamma_{O,1} - \Gamma_{L,1}) \cdot (\Gamma_{L,1} - \Gamma_{S,1})}{\Gamma_{O,1} - \Gamma_{S,1}} \quad (15)$$

In these expressions $\Gamma_{L,1}$ represents the measured reflection coefficient (b_m/a_m) when the load standard is connected to port 1. Similarly $\Gamma_{O,1}$ and $\Gamma_{S,1}$ represent the measured reflection coefficients when an OPEN respectively SHORT standard is connected to port 1. In order to find the absolute value of the voltage at the DUT we also need to know the absolute value of the power wave flowing towards the DUT. From expression (9) we know that we therefore need to

Figure 4: Illustration of the concept of the I_{DC} technique. Q_{tunnel} is obtained for different amplitudes and frequencies of a sinusoidal gate voltage signal, using a measured $I_{\text{tunnel}}-V_G$ relation. I_{DC} as it can be measured with the given $Q_{\text{tunnel}} - \text{time}$ relation is also given. I_{DC} proves to be frequency independent, but strongly dependent on the amplitude of the gate voltage.

know $|E_{1m}|$, the absolute value of E_{1m} . This value can be found from an absolute power measurement at port 1:

$$|E_{1m}| = \frac{|a_p|}{|a_{m,p}|} \cdot |1 - \Gamma_1 \cdot E_{SF}| \quad (16)$$

In this expression a_p represents the power measured by the external power (expressed as a power wave quantity) and $a_{m,p}$ is the power wave a_m as it is measured by the VNA when the external power meter is connected. Error terms M_{C1} , M_{CD} and L_C can be found using the calibration measurements at DUT level (i.e. the tip of the probe needle). Using the known values of E_{DF} , E_{SF} and E_{1m} the remaining error terms can be expressed as:

$$M_{C1} = \Gamma_{1,L,DUT} \quad (17)$$

$$M_{CD} = \frac{\Gamma_{1,O,DUT} + \Gamma_{1,S,DUT} - 2 \cdot \Gamma_{1,L,DUT}}{\Gamma_{1,O,DUT} - \Gamma_{1,S,DUT}} \quad (18)$$

$$L_C^2 = 2 \frac{(\Gamma_{1,O,DUT} - \Gamma_{1,L,DUT})(\Gamma_{1,L,DUT} - \Gamma_{1,S,DUT})}{\Gamma_{1,O,DUT} - \Gamma_{1,S,DUT}} \quad (19)$$

In expressions (17), (18), (19) quantities $\Gamma_{1,O,DUT}$, $\Gamma_{1,S,DUT}$, $\Gamma_{1,L,DUT}$ are used. They represent the apparent reflection coefficient at port 1 when an OPEN, SHORT or LOAD standard is connected at DUT level respectively. They can be found from the measured reflection coefficients using expression (11). Using expressions (13)-(19) all necessary error terms are known and the amplitude of a sinusoidal voltage signal can be determined for any DUT using expressions (9)-(12).

B. Accuracy of the voltage measurement procedure

In order to verify the accuracy of the above explained voltage measurement procedure, we have compared it with the results of the I_{DC} technique which was introduced in [6]. In the I_{DC} technique the appropriate power level for generating a sinusoidal voltage signal with a given amplitude is determined by making use of Q_{tunnel} : the total amount of

Figure 5: Comparison of obtained values of V_{pp} using the I_{DC} technique and the approach discussed in section IV A. First the RF power was set using the I_{DC} technique and subsequently V_{pp} was determined using the new technique. A very good coincidence can be seen in this figure, indicating the accuracy of the new technique.

charge that can tunnel through a thin gate oxide per unit time. Q_{tunnel} can be established by measuring it while a low frequency sinusoidal gate voltage signal is delivered to the device. The RF power can subsequently be tuned such that the desired Q_{tunnel} is reached. The I_{DC} technique makes use of the fact that the tunneling current through a thin gate oxide is strongly dependent on the gate voltage, while it is frequency independent. This is illustrated in figure 4, where Q_{tunnel} is plotted against time for three different gate voltage amplitudes and three different frequencies. This result is obtained by first measuring the gate tunneling current as a function of gate voltage and subsequently calculating the gate tunneling current as a function of time for any given gate voltage signal. Q_{tunnel} is simply the integral over time of this tunneling current. The I_{DC} technique makes use of the DC current that can be observed under an AC gate voltage; it is defined by:

$$I_{DC} = \frac{Q_{\text{tunnel}}(t_{\text{sample}})}{t_{\text{sample}}} \quad (20)$$

In this expression t_{sample} is the time over which the DC current is measured. From figure 4 it is clear that if this sampling time is much larger than the period of the applied gate voltage signal, I_{DC} is frequency independent. Figure 4 also shows that this I_{DC} is strongly dependent on the gate voltage (if the used device has a large tunneling current). This method has proven to be very useful for generating RF voltage signals in combination with RF charge pumping measurements. It can however, only be applied on test structures that have the drain and short connected. This means that we cannot use this technique for the test structures that we discussed in section II.

In order to prove the accuracy of the voltage generation approach of section IV A we therefore made use of such a test structure with the drain and source tied together. This test structure is a transistor structure laid out in a two-port ground-signal-ground configuration where the gate is

Figure 6: C-V curves obtained before and after a sinusoidal gate voltage stress with $V_{pp} = 3.2$ V, $V_{bias} = 1.6$ V and $f = 1$ GHz. The capacitance is obtained using the RF C-V technique, at a frequency of 2.5 GHz.

connected to port 1 and the drain/source to port 2. The substrate is connected to the ground plane. A Sinusoidal voltage signal of 10 MHz is applied to the gate with four different well-controlled amplitudes (as observed with an oscilloscope). I_{DC} is recorded for every amplitude used. For higher frequencies the RF power is tuned such that the recorded values of I_{DC} are reached. Subsequently the amplitude of the sinusoidal gate voltage signals is determined using the approach discussed in section IV A. The result of this is shown in figure 5. We made use of a Rohde & Schwarz ZVB 20 VNA for generating the RF power and measuring a_m and b_m . I_{DC} was measured using a HP 4156A parameter analyzer and the absolute power measurement during calibration was performed using an HP 437B power meter. We clearly see that both methods coincide very well concerning the determined amplitude of the gate voltage for all amplitudes and frequencies used. It should be noted that higher amplitudes could not be tested, as this will lead to such high peak voltages that the used gate oxides will break down. The reason for this is that we can only measure I_{DC} accurately at the drain source/port when the device is constantly biased in inversion (i.e. also at the low peak of the gate voltage signal).

V. EXPERIMENTS

Using the technique discussed in section IV A we can determine the amplitude of RF voltage signals at DUT level. We have applied this approach in combination with some reliability experiments. The idea of these experiments was to degrade devices under a sinusoidal gate voltage stress with different frequencies and monitor the degradation of the transistor performance. In order to realize this we made use of the setup as shown in figure 2, the VNA used was a Rohde & Schwarz ZVB 20 VNA and the generation of DC voltages and measurement of DC currents was performed using an HP4156 A parameter analyzer. Furthermore an HP 437 B power meter was used for performing the absolute power level measurements during the voltage calibration procedure. The equipment was linked using an IEEE-488 bus and connected to a PC. The equipment was controlled using

Figure 7: Degradation of transconductance g_m after a sinusoidal gate voltage stress with $V_{pp} = 3.2$ V, $V_{bias} = 1.6$ V and $f = 1$ GHz. The inset shows a zoomed-in portion of the graph where $g_{m,max}$ is determined.

Labview routines that are able to perform the calibration procedure as discussed in section IV, stress devices during a set amount of time and measure DC and RF characteristics of the devices. The experiments performed started with a calibration of the measurement setup for frequencies ranging from 10 MHz to 1 GHz. After this calibration, stress experiments were performed using a sinusoidal gate voltage stress with $V_{pp} = 3.2$ V and $V_{bias} = 1.6$ V, the voltage signal shown in figure 1. The test structures used were metal gate transistor structures laid out as discussed in section II. The structures consisted of 8 identical cells connected together. Each cell has 8 gate fingers with a finger width of 3 μ m, leading to a total gate width of 192 μ m. The gate length was 0.13 μ m.

Stress experiments were performed for 9 different frequencies of the gate voltage, using one test structure for every frequency. The appropriate power level for realizing the desired V_{pp} was tuned using a Labview routine that gradually increases the RF power level and measures the realized amplitude using the approach of section IVA, until the desired V_{pp} is reached. This was done for every test structure (and thus every frequency). Device characteristics were measured

Figure 8: Degradation of maximum transconductance $g_{m,max}$ as a function of stress time, under equivalent stress conditions, but with various frequencies, ranging from 10 MHz to 1 GHz. The solid line is included as a guide to the eye.

Figure 9: Degradation of maximum transconductance $g_{m,max}$ plotted against the frequency of the stress signal, for different stress times. The dotted lines are included as a guide to the eye. The degradation appears to be frequency independent.

before any stress was applied; this was followed by a sinusoidal gate voltage stress (with appropriate V_{bias} , RF power and frequency). The stress was interrupted after 10 s, 100 s and 1000 s, after which the device characteristics were measured again. Using the setup of figure 2 and having various Labview routines, we can monitor a broad range of device characteristics including both DC as well as RF characteristics. As an example we show the oxide capacitance before and after stress with a frequency of the stress voltage of 1 GHz in figure 6. The presence of the VNA in the measurement setup, makes the RF C-V technique [8] the ideal tool to measure the oxide capacitance on this (thin oxide) transistor structure. The capacitance was extracted at 2.5 GHz and was accompanied with OPEN-SHORT de-embedding. In figure 6 we see a vertical shift in the capacitance. This appears to indicate that we are dealing with some drift. The obtained C-V curves are not able to show a clear shift in the flat-band and threshold voltage after stress which would be a good indicator of any oxide degradation.

A parameter which does show a clear degradation after stress is the transconductance g_m of the device. In figure 7 we show g_m measured as a function of gate voltage and with the drain voltage set to 0.1 V before and after stress. From this figure we can clearly see the degradation of g_m after a stress has been applied to the device. This degradation increases with increasing stress time. We plotted the degradation of $g_{m,max}$ against time and frequency as shown in figures 8 and 9. This $g_{m,max}$ is defined as the maximum g_m over an entire V_G sweep, as illustrated in the inset of figure 7. From figures 8 and 9 it appears that the stress frequency does not have a serious effect on the degradation of the transconductance of the device, indicating that gate oxide wearout is frequency independent up to at least 1 GHz.

VI. CONCLUSIONS

In this work we have introduced a new approach for performing RF reliability experiments. This approach

consists of the use of sinusoidal stress signals for comparing the degradation of devices under different stress frequencies. The use of sinusoidal stress voltage signals proves to be very beneficial in the design of appropriate test structures. We have shown that sinusoidal gate voltage signals with frequencies ranging up to at least 1 GHz can be generated on one single generic test structure. This makes the design of complex test structures for every stress frequency obsolete. The calibration procedure that we have used proved to be very accurate, making it possible to use a Vector Network analyzer as a stress voltage generator with various frequencies up to at least 1 GHz. The results of the stress experiments that we have shown indicate that the degradation of the transconductance of our devices is frequency independent. This would imply that the gate oxide wearout under a gate voltage stress is also frequency independent up to 1 GHz. To the best of our knowledge this has never been shown before. The methodology as it is described in this paper can easily be adjusted to perform all sorts of different RF reliability experiments (e.g. stressing at the drain side for investigate the hot carrier effect).

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