Test Structures for Accurate UHF C-V Measurements of Nano-Scale CMOSFETs with HfSiON and TiN Metal Gate

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Abstract— Test structures for accurate UHF capacitance–voltage (C-V) measurements of high performance CMOSFETs with Hf-based high-k dielectric and TiN metal gate are analyzed. It is shown that series resistance or substrate resistance between the channel region and body contact plays a role in UHF C-V measurements. The substrate resistance beneath the gate region also impacts accurate UHF C-V measurements. Therefore, minimization of series resistance through short gate lengths with a minimum distance between the source/drain and body contact is highly desired for an accurate evaluation of gate dielectric thickness using UHF C-V measurements.

Index Terms— UHF, Capacitance-Voltage (C-V), CMOS, High-k, Series resistance

I. INTRODUCTION

Accurate measurement of capacitance-voltage (C-V) characteristics, i.e., accurate extraction of electrical thickness of gate dielectric is essential in developing CMOS technologies. Along with the rapid scale down of the minimum feature size of CMOSFETs, the thickness of gate dielectric has also been scaled down below 1.5 nm. However, it becomes increasingly more difficult to accurately evaluate the gate dielectric thickness due to the exponential increase of direct tunneling leakage current. The excessive leakage current also limits the normal operation of CMOS devices and further scaling of nano-scale CMOSFETs. Although the direct tunneling leakage current can be significantly reduced using a high-k dielectric, the leakage current level is still high enough to hinder the accurate measurement of gate capacitance. Two-frequency [1,2], RF and UHF [3-5] C-V measurements, have been proposed to overcome this measurement problem.

In this paper, UHF C-V measurements and test structure guidelines for advanced gate structure with high-k dielectric and metal gate are demonstrated. At a very high frequency, whereas the leakage current may be less important during capacitance measurement, the series resistance can become significant because of the low impedance of the capacitor

[6-8]. Because series resistance of the well region still has a substantial effect on the C-V measurement, test structures with minimum substrate resistance should be used for accurate UHF measurements.

II. EXPERIMENT AND SERIES RESISTANCE EFFECT

The key process flow for fabrication of test chips is summarized in Fig. 1. A novel CMOS technology with HfSiON and TiN metal was used for fabricating test chips or UHF capacitor structures. First, STI (Shallow Trench Isolation) isolation is followed by formation of retrograde twin well. Then, 30 Å HfSiON and 100 Å TiN were subsequently deposited, followed by deposition of a 100 nm poly-silicon capping layer. The equivalent oxide thickness (EOT) of the high-k dielectric is approximately 16 Å.

The I_D - V_G characteristics were measured with an HP 4156B and the C_g - V_g curve was measured with an Agilent 4294A Precision Parameter Analyzer in the frequency range from 1MHz to 110MHz. Figure 2 shows the I_D - V_G characteristics of NMOSFET with HfSiON and TiN metal. The gate width and length are 10 μm and 0.15 μm , respectively.

Figure 3(a) shows the conventional C-V test structure with a square active pattern overlapped by the gate region and its equivalent circuit model is shown in Fig. 3(b) where R_s is series resistance, C_{ox} is the capacitance, G_p is the parallel conductance. As a low-resistive metal gate and a silicided gate are used, the series resistance will be dominated by the substrate or well resistance.

Although the width of the active region is only 22.4 μm , the capacitance shows a strong dependence on the applied frequency as shown in Fig. 4(a). Moreover, the frequency dependence of capacitance increases as the active width increases as in Fig. 4(b), mainly due to the series resistance of the substrate. The equivalent circuit for measuring capacitance using the Agilent 4294A is shown in Fig. 3(c), where C_m and G_m are the measured capacitance and

- **Shallow Trench Isolation**
- **Retrograde Twin Well**
- **HfSiON 30 Å / TiN 100 Å**
- **Poly-Si 100 nm**
- **Gate patterning, Extension formation**
- **S/D formation N+(As) , P+(BF₂)**
- **RTA**
- **Co Silicidation , ILD process**
- **Metallization (Al process)**

Fig. 1. Flow diagram for fabrication of CMOSFETs.

Fig. 2. I-V characteristics of NMOSFET. Gate length and width are 0.15 μm and 10 μm .

Fig. 3. (a) General test structure for measuring C-V curve and (b) its equivalent circuit. (c) Capacitor modeling for C-V measurement.

conductance, respectively [9]. As the series resistance is not accounted for, the extracted capacitance cannot be used for accurate extraction of equivalent oxide thickness.

In order to prove the series resistance effect, the parasitic components of Fig. 3(b) were extracted using the measured data. Figure 5 shows the extracted capacitance with a modeling of series resistance as 110 Ω . The capacitance now shows little variation for wide frequency range. Therefore, it can be concluded that series resistance strongly affects the capacitance measurement and hence test structure which can eliminate series resistance effect is necessary. Hence, a new UHF test pattern for accurate extraction of electrical thickness via accurate measurement of capacitance is shown in this paper.

(a)

(b)

Fig. 4. Dependence of C-V characteristics on the applied frequencies, (a) active widths of 22.4 μm and (b) 31.6 μm .

Figure 6 shows the schematic diagram of the test structure with a two-dimensional array of unit NMOSFETs with a split of gate width and length. One notable point about the structure is that the p+ region for body contact is inserted in between the n+ regions of source/drain to reduce series resistance or substrate resistance between source/drain and substrate contact. Figure 7 shows the measured C-V curves using the test structure with 50 transistors ($W/L = 5 \mu\text{m} / 4 \mu\text{m}$). The series resistance is approximately 30 Ω in Fig. 7, it is strongly decreased compared with Fig. 4(a). Although there is little difference in capacitance at the accumulation side, in the inversion region the capacitance shows a slight frequency dependence, especially for the 110 MHz case.

Fig. 5. C-V characteristics with correction of series resistance using measured data.

Fig. 6. Schematic diagram of the fabricated test structure. A body contact is inserted between n+ regions to reduce series resistance in the substrate.

Fig. 7. UHF C-V characteristics as a function of frequency. Number of transistors, gate length, and active width are 50, 4 μm and 5 μm , respectively.

This frequency dependence can be attributed to the long gate length, which can induce a large channel resistance. For an exact characterization of the effect of series resistance, UHF C-V measurements were performed for test structures with various gate length and width.

Figure 8 shows C-V characteristics of NMOS arrays with gate length and width of (a) 2 μm and 10 μm , (b) 2 μm and 5 μm , (c) 1 μm and 5 μm , respectively. The C-V characteristics showed little dependence on frequency due to the reduction of series resistance because the aspect ratio of gate width and length is small.

Fig. 8. UHF C-V characteristics as a function of frequency. Number of transistors, gate length and active width are (a) 50, 2 μm and 10 μm , (b) 100, 2 μm and 5 μm and (c) 200, 1 μm and 5 μm , respectively.

Frequency-independent C-V curves are now obtained up to a measurement frequency of 110 MHz through an improved test structure layout. The substrate contact turns out to be crucial. Figure 9 shows C-V characteristics of a very similar test structure without the substrate (p+) region between n+ source and drain (see the test structure of Fig. 6). It is shown that the frequency dependence in accumulation region increases subsequently, which means that substrate resistance plays an important role in C-V measurement even for test structures with short gate length and narrow active width. Therefore, reducing the series resistance by reducing the distance between source/drain and substrate region is necessary.

Fig. 9. UHF C-V characteristics as a function of frequency without substrate contact. Number of transistors, gate length and active width are 720, 1 μm and 2.6 μm .

III. CONCLUSION

Test structures for UHF C-V measurements of novel MOSFETs with HfSiON and TiN metal gate have been analyzed. It is shown that substrate resistance strongly affects the UHF C-V characteristics. Therefore, drastically reducing the distance between the gate and the substrate contact is necessary for accurate extraction of equivalent gate oxide thickness of high-k dielectrics.

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